MG802C256

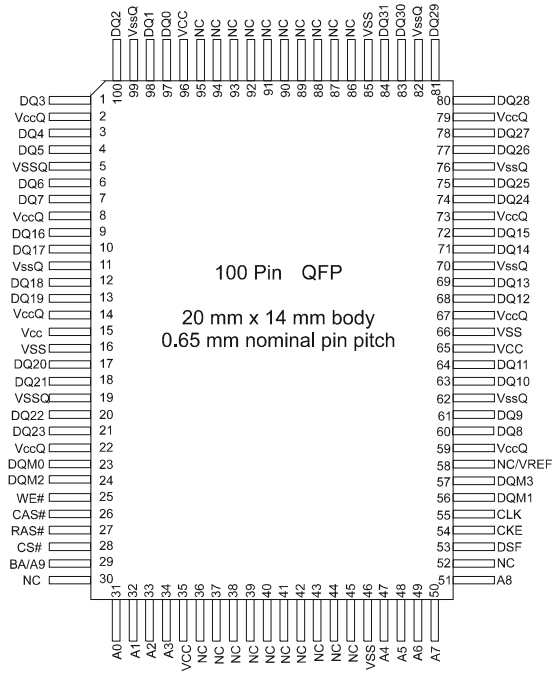
Ultra Low Latency, High Performance

256Kx32 SGRAM

Preliminary Information

Features

- SGRAM protocol
- High bandwidth 100MHz-166MHz operation
- Reduced Latency
- Improved critical timing parameter limits
- 2 Internal Banks for hiding Row Precharge
- Independent byte operation via DQM[3:0]
- Burst length - 1,2,4,8 and full page
- Burst Type: Linear, Wrap
- Capacity: 8Mb
- Organization: 256Kx32 (8Mbit)
- Refresh Interval 15.6uSec
- CBR Refresh.
- LVTTL Interface
- Supply voltages - 3.3 V ± 0.3V
- Package - 100-pin QFP



Overview

The MoSys SGRAM is a synchronous memory for graphics, multimedia, networking and other applications. It implements SGRAM commands and offers shorter Precharge (t_{RP}), faster Access Latency (t_{RC}, t_{RAS}, t_{RCD} and CL=2) and better pipelining capability. In addition to the SGRAM command set, the MoSys SGRAM implements an eight column Block Write function and a Masked Write (Write Per Bit) function to accommodate graphics applications.

Options

MoSys SGRAM supports the following device options

Option	Marking
6.0ns Cycle Time	-6
6.6ns Cycle Time	-6R6
7.5ns Cycle Time	-7R5
8ns Cycle Time	-8
10ns Cycle Time	-10

Part Number Designation
Example*: MG802C256QR -8*
Device Designation: *MG8*, Series: *02C*
Organization: *256Kx32*
Package Type: *Q*=PQFP, *L*=LQFP
Pinout: *R*=*Reverse (Mirror Image)*
Speed: *–8*=125MHz

Key Timing Parameters

Speed Grade	Clock Frequency (MHz)	Access Time (ns)	Setup Time (ns)	Hold Time (ns)	CAS Latency (CL)	RAS Access Time - tRAS (ns)	Cycle Time - tRC (ns)
-6	≤ 166	5	2	1	3	24	42
-6R6	≤ 150	5	2	1	3	26.4	46.2
-7R5	≤ 133	6	2.2	1	3	30	53
-8	≤ 125	6	2.3	1	2	24	40
-10	≤ 100	7	2.5	1	2	30	50

Functional Description

Pin Description

Pin Name	Pin Number	Pin Total	I/O	Description
CLK	55	1	I	***System Clock:*** All inputs are sampled on positive edge.
CS#	28	1	I	***Chip select:*** Disables or enables the device operation by masking or enabling all inputs except CLK, CKE and DQM.
CKE	54	1	I	***Clock Enable:*** CKE controls the Power Down Mode in MoSys SGRAM. When in Power Down Mode all input and output buffers are de-activated.
A[8:0]	51-47, 34-31	10	I	***Address Inputs:*** Row & Column address are multiplexed on the same pins.
RAS#	27	1	I	***Row Address Strobe:*** Latches Row address on the positive edge of clock with RAS# low. Enables Row access.
CAS#	26	1	I	***Column Address Strobe:*** Latches Column Address on the positive edge of clock. Enables column access.
WE#	25	1		***Write Enable:*** Enables write operation.
DSF	53	1	I	***DSF:*** Enables the Write Per Bit and Block Write function. *This pin has an internal pull-down resistor.*
DQM[3:0]	57, 24, 56, 23	4	I	***Data Input/Output Mask:*** Write data byte mask, Read output byte enables. Read latency is two cycle from DQM and zero cycle for write. The DQM masking occurs two cycles later in the Read operation and in the same cycle during Write operation. DQM is synchronous to the clock, thus the masking occurs for the whole clock.
DQ[31:0]	84, 83, 81, 80, 78, 77, 75, 74, 1, 20, 18, 17, 13, 12, 10, 9, 72, 71, 69, 68, 64, 63, 61, 60, 7, 6, 4, 3, 1, 100, 98, 97	32	I/O	***Data Input/Output:*** Bidirectional data bus.
BA	29	Input	I	***Bank Address 0:*** Bank Address defines to which Bank the Activate, Read, Write or Precharge Command is issued. BA0 is also used to program the 10th bit of the Mode Register.

Signal description for 256Kx32 MoSys SGRAM

Parameter	
Bank Address	BA
Row Address	A[8:0]
Column Address	A[7:0]
Auto Precharge	A8
Page Size	256x32

Bank, Row and Column Address mapping

CONTROL REGISTERS

MOSYS SGRAM incorporates four programmable registers, the Mode Select Register (MSR), Special Mode Register (SMR), Color Register (CR) and the Mask Register (MR). This section describes the use of these registers. In describing the functionality, the following terms are used.

WO **Write Only**. A register bit with this attribute is Write Only.
R **Reserved**. A register bit with this attribute is Reserved.

Mode Register (MSR)

MOSYS SGRAM's mode register is accessed through the Mode Register Write Command (op code '00000'). Mode Register is used to load the value of CAS Latency and Burst Length of MOSYS SGRAM.

Bit	Default	Attribute	Description
8:7	00	WO	***Reserved:*** 00 Standard operation 00 Reserved (for MOSYS Use only) 01 Reserved (for MOSYS Use only) 01 Reserved (for MOSYS Use only)
6:4	011	WO	***CAS Latency***: 000 Reserved 001 Reserved 010 2 011 3 100 4 101 Reserved 110 Reserved 111 Reserved
3	0	WO	***Burst Type:*** 0=Linear Burst Mode, 1=Wrap Mode
2:0	010	WO	***Burst Length***: 000 1 1 001 2 2 010 4 4 011 8 8 100 Reserved Reserved 101 Reserved Reserved 110 Reserved Reserved 111 Full Page Reserved

Description of Mode Register

Special Mode Register (SMR)

MOSYS SGRAM's Special Mode Register is accessed through the Mode Register Read/Write Command (op code '00001'). Special Mode Register is used to load data into the Color Register or the Mask register. During the execution of the Special Mode Register Command Bits A[6:5] are used to determine if a new value is to be loaded into the Color and Mask Registers.

Bit	Default	Attribute	Description
BA0, A[8:7]	000	WO	***Reserved:*** For Standard operation these bits should always be "000".
A[6]	0	WO	***Color Register:*** 0=Leave data unchanged for Color Register, 1=Load new data into Color Register.
A[5]	0	WO	***Mask Register:*** 0=Leave data unchanged for Mask Register, 1=Load new data into Mask Register.
A[4:0]	0000	WO	***Reserved:*** For Standard operation these bits should always be "0000".

Description of Special Mode Register

Color Register (CR)

Data is loaded into the Color Register through the Special Mode Register Write Command. During the execution of the Special Mode Register Command, bit A[6] is used to determine if a new value is to be loaded into the Mask Registers. If A[6] =1 during the Special Mode Register Command then the value on DQ[31:0] is loaded into the Color Register. The Color Register supplies data for the Block Write Command.

Bit	Default	Attribute	Description
31:0	00000000h	WO	***Color Register Data:*** Data from these bits is used for Block Write Command.

Description of Color Register

Mask Register (MR)

Data is loaded into the Mask Register through the Special Mode Register Write Command. During the execution of the Special Mode Register Command, bit A[5] is used to determine if a new value is to be loaded into the Mask Registers. If A[5] =1 during the Special Mode Register Command then the value on DQ[31:0] is loaded into the Mask Register. The Mask Register is used for Mask Per Bit functionality during the Masked Write of Masked Block Write Command. Mask Per Bit is used in conjunction with the DQM[3:0] to determine the mask for each bit.

Bit	Default	Attribute	Description
31:0	00000000h	WO	***Mask Register Data:*** Data from these bits is used for Masked Write and Block Write Command.

Description of Mask Register

DEVICE OPERATION

This section provides a description of MOSYS SGRAM device.

Device Function

The following command table lists all supported MOSYS SGRAM commands. All fixed length burst (non full page burst length) operations can be self terminated, terminated by BST, interrupted by another Read or Write operation or by a Precharge operation to the same Bank. For Auto Precharge Read or Write, the operation cannot be interrupted and has to self-terminate after the programmed burst length. Auto Precharge has no effect for a full page burst length operation. To provide backward compatibility with SDRAM command set, the MOSYS SGRAM incorporates an internal pull-down resistor for the DSF pin.

Mode Register Write

The Mode Register stores data for controlling various functions of MOSYS SGRAM. Through the mode register the CAS Latency, Burst Type, Burst Length and the PLL enable mode can be programmed for the device. The default value of the Mode Register is defined as CAS Latency of 3, Burst Type of linear and Burst Length of 4. The Mode Register is written to by driving CS#, RAS#, CAS#, WE# and DSF low.

Special Mode Register Write

The Special Mode Register controls the data written to Color or Mask Register of MOSYS SGRAM. During the Special Mode Register Command A[6:5] are used to indicate to the MOSYS SGRAM whether a new data pattern is to be written to Color or Mask Registers. The Special Mode Register is written to by driving CS#, RAS#, CAS#, WE# and DSF high.

Bank Activate

The Bank Activate Command selects a Row in a Bank. Bank is activated by driving CS# low, RAS# low, CAS# high, WE# high and DSF low with the correct Bank and Row specified on BA and A[8:0]. The Read/Write Command can follow the Activate Command after the t_{RCD} timing has been met. Every Bank Activate Command must satisfy the minimum t_{RAS} before a Precharge Command can be issued to that Bank.

Activate with WPB

The Bank Activate with WPB Command selects a random Row in an idle Bank. Bank is activated by driving CS# low, RAS# low, CAS# high, WE# high and DSF high with the correct Bank and Row specified on A[10/9:0]. The Write or Block Write Command can follow the Activate Command after the t_{RCD} timing has been met. A Write Command to the selected Bank will be masked according to the contents of the Mask Register and DQM[3:0]. A Block Write Command following the Activate with WPB Command will be masked according to the contents of the Mask Register, DQM[3:0] and the Column/Byte Mask information on the DQ[31:0] pins.

Read

The Read Command is used to access data from an active Row and Bank within the device. The Read Command is issued by driving CS# low, RAS# high, CAS# low, WE# high and A8 low (no

Auto Precharge). The Bank must have been active for at least the minimum t_{RCD} before the Read Command is issued. The first data appears on the output in CAS Latency (number of Clocks) after the Read Command is issued. Upon completion of the burst Read access (assuming that no new command is pipelined after the existing Read Command) the DQ[31:0] will go to high Z state. A fixed length Burst Read (1,2,4 or 8) can be either terminated by another Read, Write (for a Read interrupted by Write Command the DQMs should be used control to prevent data contention of the DQ pins), Precharge Command to the same Bank or a Burst Stop Command .

A Full Page Burst Read can be interrupted by a Burst Stop Command (BST) or a Precharge Command to the same Bank. A Full Page Burst is used in conjunction with the BST Command to generate an arbitrary burst length. A Full Page Burst is not self-terminating; the address wraps around after the last address in the page.

Read with Auto Precharge is issued by driving CS# low, RAS# high, CAS# low, WE# high and A8 high. The Bank must have been active for at least the minimum t_{RCD} before the Read with Auto Precharge Command is issued. The first data appears on the output in CAS Latency (number of Clocks) after the Read Command is issued. The accessed Bank is automatically Precharged after the Read Command (after providing the burst read data as specified by the burst length field in the Mode Register). For Burst Length of 1,2,4 and 8 the Precharge is carried out one clock after the Column Address is latched and is independent of the CAS latency. For a full page burst, Read with Auto Precharge has no effect (no Precharge is carried out after the full page burst read access).

Read with Auto Precharge cannot be terminated by another command. Read with Auto Precharge is self terminated after the read data is provided for the fixed length burst Read.

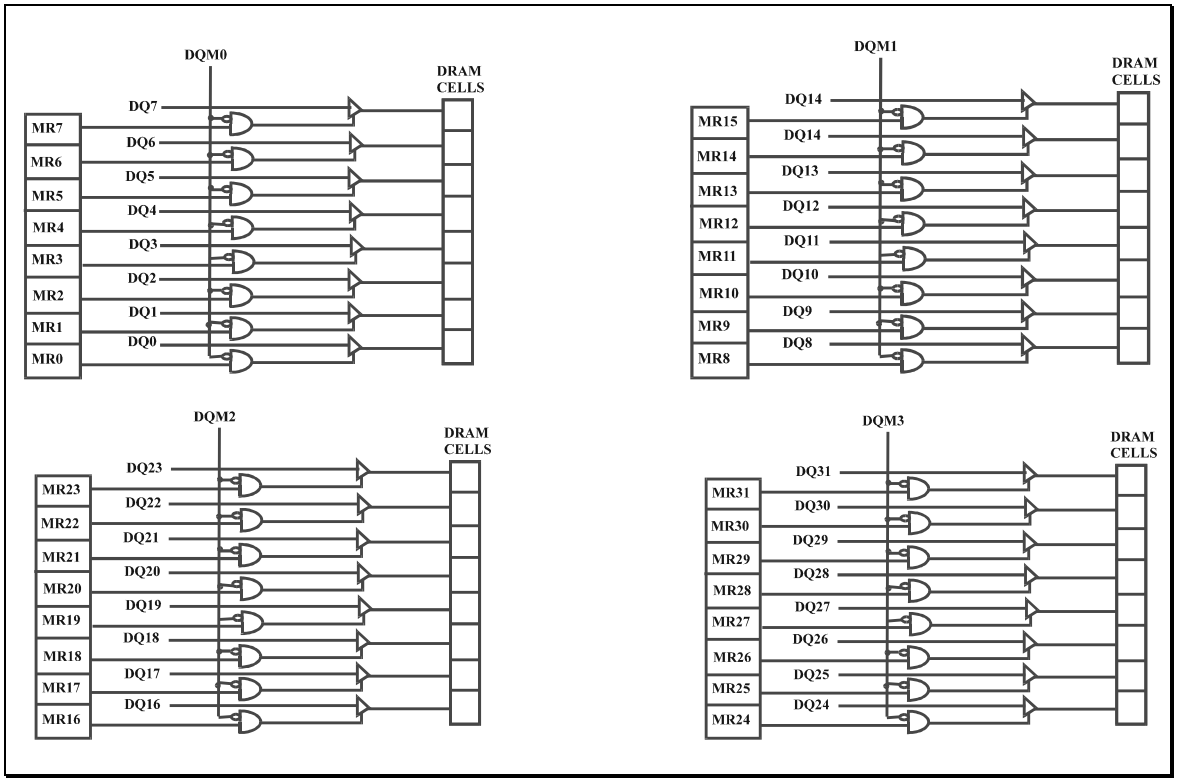
Write

The Write Command is used to write data to an active Row and Bank within the device. The Write Command is issued by driving CS# low, RAS# high, CAS# low, WE# low and A8 low. The Bank must have been active for at least the minimum t_{RCD} before the Write Command is issued. The write latency of the device is 0.

Write with Auto Precharge is issued by driving CS# low, RAS# high, CAS# low, WE# low and A8 high. The Bank must have been active for at least the minimum t_{RCD} before the Write with Auto Precharge Command is issued. The accessed Bank is automatically Precharged after the Write Command. Auto Precharge is carried out, starting two clocks (t_{WR}) after the last data is sampled. The Precharged Bank can be activated after t_{RP} has been met.

Masked Write

Any Write Command to a Row that was opened (activated) using an Activate with WPB Command is a Masked Write Command. Data is written to the Column Address subject to the Mask Write information in the Mask Register. If a particular bit in the Mask Register is '0' then the data on the corresponding DQ pin will be ignored (masked) and the existing data in that particular DRAM cell will be unchanged. If a particular bit in the Mask Register is '1' then the data on the corresponding DQ pin, based on the value of DQM[3:0] signals, will be written to the particular DRAM cell. For a Masked Write operation the overall Write Mask consists of the DQM[3:0] information (which specify the Write Mask Per Byte) and the MR[31:0] information (which specify the Write Per Bit Mask). A particular bit is written only if the corresponding DQM is low ('0') and the corresponding MR[x] is high ('1').



Block Write

The Block Write Command is used to Write a block of data to an active Row and Bank within the device. The Block Write Command is issued by driving CS# low, RAS# high, CAS# low, WE# low and DSF high. A Block Write Command is a non-burst Write Command that writes data to eight columns simultaneously. The data value contained in the Color Register (CR) is written to eight consecutive column locations addressed by A[7:3]. When the Block Write Command is executed, the value on DQ[31:0] pins is used to mask the particular column and byte within the 8 column block. For example DQ0 controls byte 0 for address '000' (within the eighth column block) , DQ8 controls byte 1 for address '000', DQ16 controls byte 2 for address '000' and DQ24 controls byte 3 for address '000'.

When a '0' is sampled on a particular DQ with the Block Write Command the corresponding column and byte combination is masked. When a '1' is sampled the Color Register data will be written to the corresponding locations (based on the value of DQM and MR[31:0] bits). The following Table specifies the column and byte combination controlled by each DQ.

DQ Input	Column Address Controlled			Address Controlled	Byte Controlled
	A2	A1	A0		
DQ0	0	0	0	0h	Byte 0
DQ1	0	0	1	1h	Byte 0
DQ2	0	1	0	2h	Byte 0
DQ3	0	1	1	3h	Byte 0
DQ4	1	0	0	4h	Byte 0
DQ5	1	0	1	5h	Byte 0
DQ6	1	1	0	6h	Byte 0
DQ7	1	1	1	7h	Byte 0
DQ8	0	0	0	0h	Byte 1
DQ9	0	0	1	1h	Byte 1
DQ10	0	1	0	2h	Byte 1
DQ11	0	1	1	3h	Byte 1
DQ12	1	0	0	4h	Byte 1
DQ13	1	0	1	5h	Byte 1
DQ14	1	1	0	6h	Byte 1
DQ15	1	1	1	7h	Byte 1
DQ16	0	0	0	0h	Byte 2
DQ17	0	0	1	1h	Byte 2
DQ18	0	1	0	2h	Byte 2
DQ19	0	1	1	3h	Byte 2
DQ20	1	0	0	4h	Byte 2
DQ21	1	0	1	5h	Byte 2
DQ22	1	1	0	6h	Byte 2
DQ23	1	1	1	7h	Byte 2
DQ24	0	0	0	0h	Byte 3
DQ25	0	0	1	1h	Byte 3
DQ26	0	1	0	2h	Byte 3
DQ27	0	1	1	3h	Byte 3
DQ28	1	0	0	4h	Byte 3
DQ29	1	0	1	5h	Byte 3
DQ30	1	1	0	6h	Byte 3
DQ31	1	1	1	7h	Byte 3

Mapping of DQ[31:0] to column and byte location within the block

The overall mask for a Block Write Command consists of DQM[3:0], MR[31:0] and the DQ[31:0] information provided with the Block Write Command.
A Block Write access requires a minimum time of t_{WBC} to execute. No new commands can be executed until t_{WBC} is met, except for the Activate and Precharge Commands to the second Bank.

DQM Operation

DQM is used to mask Read and Write operations. Read latency is two cycles from DQM and zero cycles for write. The DQM masking occurs two cycles later in the Read operation and in the same cycle during Write operation. DQM is synchronous to the clock.

Precharge

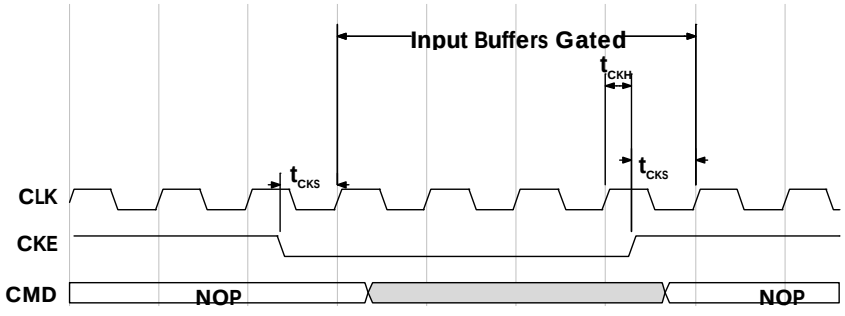
The Precharge Command is issued by driving CS# low, RAS# low, CAS# high, WE# low, Valid Bank Address and A8. If A8 is low during the assertion of the Precharge Command, then the Bank specified by the Bank address is Precharged. If A8 is high during the assertion of the Precharge Command, then both Banks are Precharged. For a Precharge Command the minimum value of t_{RP} should be satisfied before a new command is issued. After Precharge the Bank goes into the idle state.

CBR Refresh

The CBR Refresh Command is issued by driving CS# low, RAS# low, CAS# low and WE# high. Before executing the CBR Refresh Command all Banks should be Precharged. The internal counter increments internally on the CBR Refresh Command. The time required to complete the refresh cycle is specified by t_{RC} (min). The CBR Refresh should be performed at least every 15.6 usec, since the device does not do self refresh in the Power Down Mode.

Device Power Down

The device power down for MOSYS SGRAM can be entered when both Banks are in idle state (Precharged) and CKE is asserted low. In device power down all input and output buffers are de-activated (except for CKE). If the device stays in the Power Down Mode for more than 15.6 usec (refresh interval), then the MOSYS SGRAM will lose data.
The device power down can be terminated by driving CKE high again. CKE assertion and de-assertion should meet the CKE setup and hold time (t_{CKS} and t_{CKH}).



Timing Diagram for Power Down Mode

Power on Condition

The MOSYS SGRAM device generates power-on reset at power up. The internal power-on reset sets all the internal mode register values to the default state.

Command Table

Operation	Cmd	Command							BA, A[8:0]
		CS#	RAS#	CAS#	WE#	DSF	DQM	A8	
Mode Register Write	MSR Wr	0	0	0	0	0	x	V	BA, A[8:0] carry data for MSR.
Special Mode Register Write	SMR Wr	0	0	0	0	1	x	V	BA, A[8:0] carry data for SMR, DQ[31:0] carry the data for Color or Mask Register.
CBR Refresh	Ref	0	0	0	1	0	x	x	x
Activate (Single Bank)	Act	0	0	1	1	0	x	V	BA, A[8:0] carry the Bank and Row Address.
Activate with WPB (Single Bank)	Act	0	0	1	1	1	x	V	BA, A[8:0] carry the Bank and Row Address.
Write	Wr	0	1	0	0	0	v	0	BA carries the Bank Address and A[7:0] carry the Column Address.
Block Write	Blk Wr	0	1	0	0	1	v	0	BA carries the Bank Address and A[7:0] carry the Column Address.
Write with Auto Precharge	Wr AP	0	1	0	0	0	v	1	BA carries the Bank Address and A[7:0] carry the Column Address.
Read	Rd	0	1	0	1	0	v	0	BA carries the Bank Address and A[7:0] carry the Column Address.
Read with Auto Precharge	Rd AP	0	1	0	1	0	v	1	BA carries the Bank Address and A[7:0] carry the Column Address.
Burst Stop	BST	0	1	1	0	0	x	x	x
Precharge Single Bank	Pre	0	0	1	0	0	x	0	BA carry the Bank Address.
Precharge All Banks	Pre ALL	0	0	1	0	0	x	1	x
No Operation	NOP	0	1	1	1	0	x	x	x
No Operation	NOP	1	x	x	x	x	x	x	x

MoSys SGRAM Command Table

Electrical Characteristics

DC Specifications

Symbol	Parameter	Min	Max	Units	Notes
V_{CC}	Voltage on V_{CC} relative to V_{SS}	-1	4.6	V	1
V_{CCQ}	Voltage on V_{CCQ} relative to V_{SS}	-1	4.6	V	1
Pwr	Power Dissipation		1.6	W	1
Isc	Short Circuit Current		50	mA	1
Tst	Storage Temperature	-55	150	˚C	1
Ta	Operating Temperature	0	70	˚C	1

Absolute Maximum Ratings

Note 1: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating and functional operation of the device at these or any other conditions above those indicated in operational sections of this specifications is not implied.

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
V_{CCQ}	I/O Supply Voltage	3.0	3.3	3.6	V
V_{ih}	Input High Voltage	2.0		V_{CCQ} + .3	V
V_{il}	Input Low Voltage	-0.3		0.8	V
I_{il}	Input Leakage Current Any Iuput 0V≤ V_{IN} ≤V_{CC} (All other pins not under test =0V)	-2		+2	µA
I_{oz}	Output Leakage Current DQs are disabled;0V≤ V_{OUT} ≤V_{CCQ}	-10		+10	µA
V_{oh}	Output High Voltage @ I_{OUT}=8mA	2.4			V
V_{ol}	Output Low Voltage @I_{OUT}=8mA			0.4	V
C_{in}	Input Pin Capacitance	2		4	pF
$C_{I/O}$	I/O Pin Capacitance	2		5	pF
C_{OUT}	Output Pin Capacitance	2		5	pF
L_{pin}	Pin Inductance			10	nH
Ta	Ambient Temperature	0	25	70	°C

DC Operating Requirements

Parameter	Symbol	- 6 Max	- 6R6 Max	- 7R5 Max	- 8 Max	-10 Max	Units
Standby Current, Power Down Mode CKE ≤ V_{IL} (MAX), both Banks idle.	I_{CC1}	1.5	1.5	1.5	1.5	1.5	mA
Standby Current, CS# ≥ V_{IH} (MIN), t_{CK} ≥ t_{CK} (MIN), CKE ≥ V_{IH} (MIN), both Banks idle.	I_{CC2}	60	55	53	50	40	mA
Standby Current, CS# ≥ V_{IH} (MIN), t_{CK} ≥ t_{CK} (MIN), CKE ≥ V_{IH} (MIN), both Banks active after t_{RCD} is met.	I_{CC3}	70	65	63	60	50	mA
Auto Refresh Current.	I_{CC4}	160	160	145	135	110	mA
Operating Current: Active mode, burst =2 Read or Write t_{RC} ≥ t_{RC} (MIN), one Bank active.	I_{CC5}	200	190	180	160	130	mA
Operating Current: Active mode, burst =2 Read or Write t_{RC} ≥ t_{RC} (MIN), two Banks active.	I_{CC6}	300	280	260	230	190	mA
Operating Current: Burst Mode, Full Page Burst after t_{RCD} met, Read or Write, t_{CK} ≥ t_{CK} (MIN), other Bank idle.	I_{CC7}	250	235	225	195	160	mA
Operating Current: Block Write, t_{CK} ≥ t_{CK} (MIN), t_{WBC} ≥ t_{WBC} (MIN), one Bank active.	I_{CC8}	200	190	180	160	130	mA

ICC Specifications and Conditions

Timing and Measurement

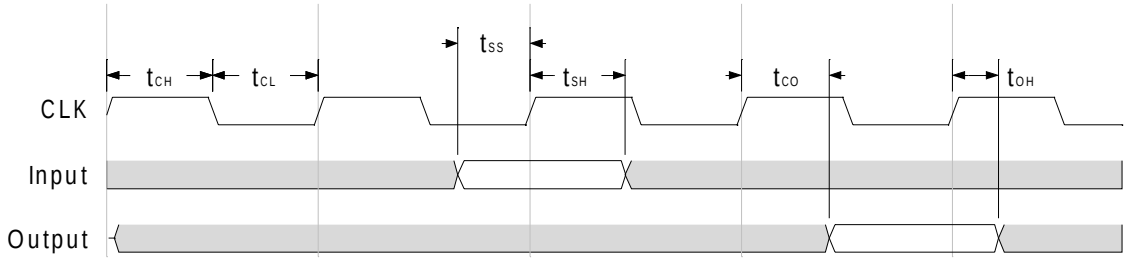
Device Timing Specification

Parameter	Symbol	- 6		- 6R6		- 7R5		- 8		-10		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
System Clock Cycle Time	t_{CK}	6		6.6		7.5		8		10		ns
CAS Latency	CL	3	3	3	3	3	3	2	3	2	3	CLK
CLK to Valid Output Delay	T_{CO}		5		5		5.5		6		7	ns
Output Data Hold Time	t_{OH}	3		3		3.3		3 .5		4		ns
CLK High Pulse Width	t_{CH}	3		3		3.3		3.6		4		ns
CLK Low Pulse Width	t_{CL}	3		3		3.3		3.6		4		ns
Input Setup Time	t_{SS}	2		2		2		2		2.5		ns
Input Hold Time	t_{SH}	1		1		1		1		1		ns
Activate to Activate Delay (Different Bank)	t_{RRD}	2		2		2		2		2		CLK
Read to Read Command Delay, Write to Write Command Delay[1]	t_{CCD}	1		1		1		1		1		CLK
Activate to Read, Write or Block Write Delay	t_{RCD}	3		3		3		2		2		CLK
Precharge to Activate Delay (single Bank Precharge)	t_{RP}	3		3		3		2		2		CLK
Activate to Precharge Delay	t_{RAS}	4		4		4		3		3		CLK
Activate to Activate Delay (Same Bank), Refresh Cycle time	t_{RC}	7		7		7		5		5		CLK
Refresh Cycle Time	t_{RFCYC}	7		7		7		6		6		CLK
Block Write to Precharge Delay	t_{BPL}	3		3		3		2		2		CLK
Block Write Cycle Time	t_{BWC}	2		2		2		2		2		CLK
Last Write Data to Precharge	t_{WR}	2		2		2		1		1		CLK
Load Register (Special or Mode) Command to Command	t_{LRC}	2		2		2		2		2		CLK
Refresh Interval	t_{Ref}	15.6		15.6		15.6		15.6		15.6		us
CKE Setup Time	t_{CKS}	2		2		2		2		3		ns
CKE Hold Time	t_{CKH}	1		1		1		1		1		ns

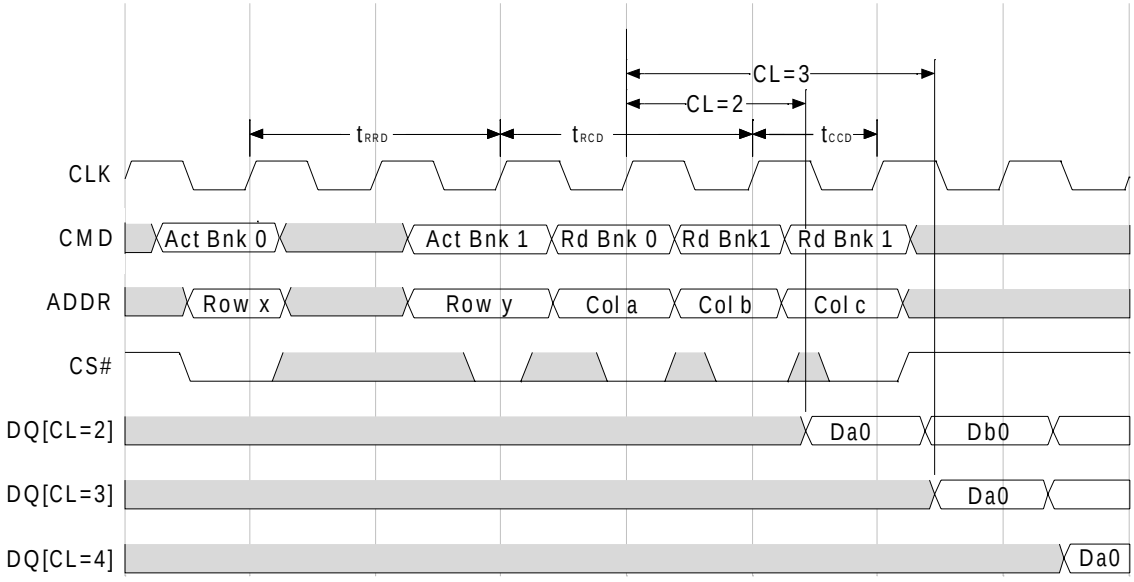
Device Timing Parameters

[1] The Write Command could be a Write or Masked Write Command.

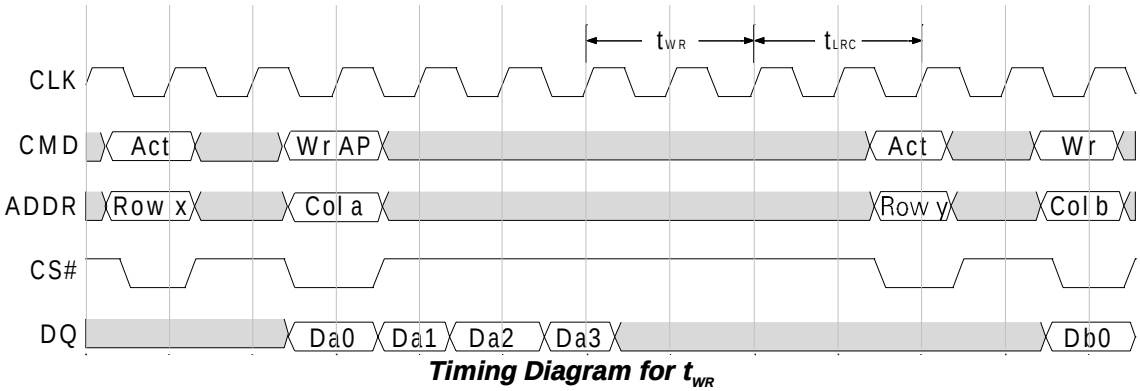
Device Timing Parameters



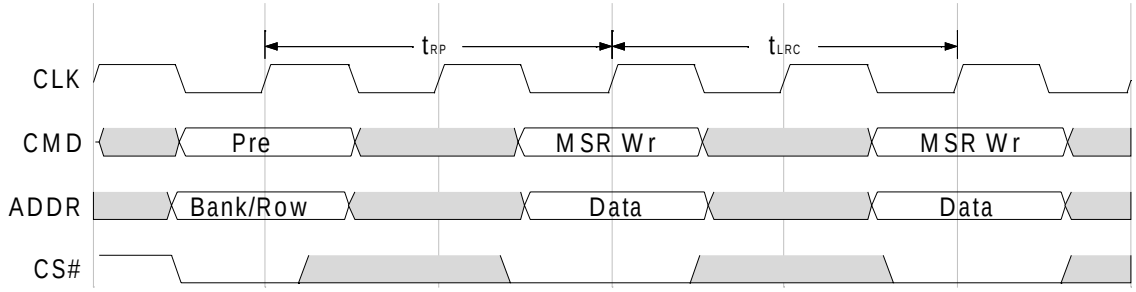
Timing Diagram for Input Setup/Hold, Clock and Output



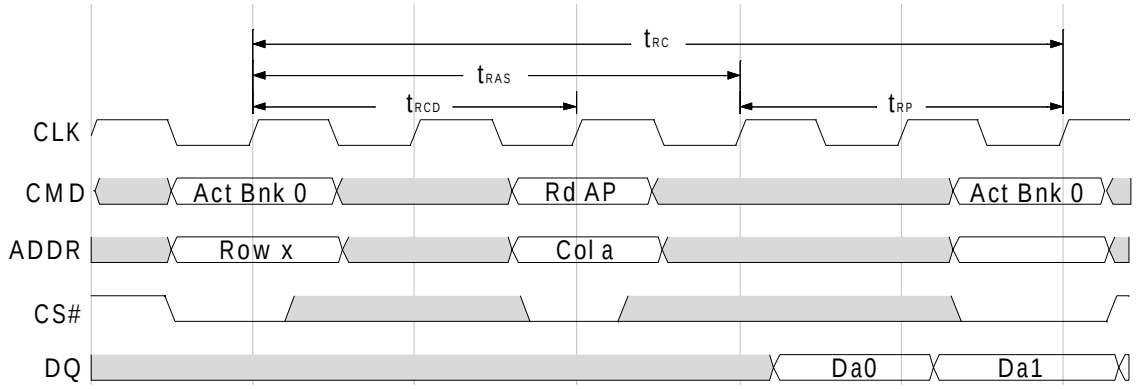
Timing Diagram for t_{RCD}, t_{CCD}, t_{RRD} and CL



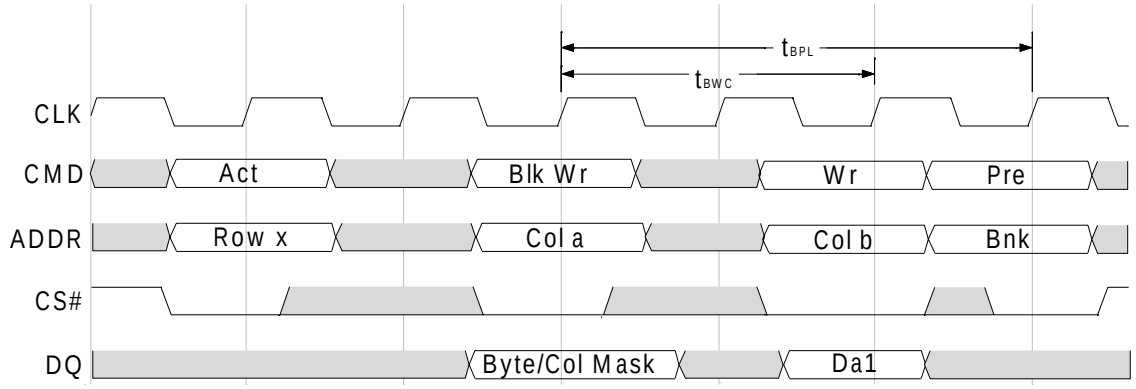
Timing Diagram for t_{WR}



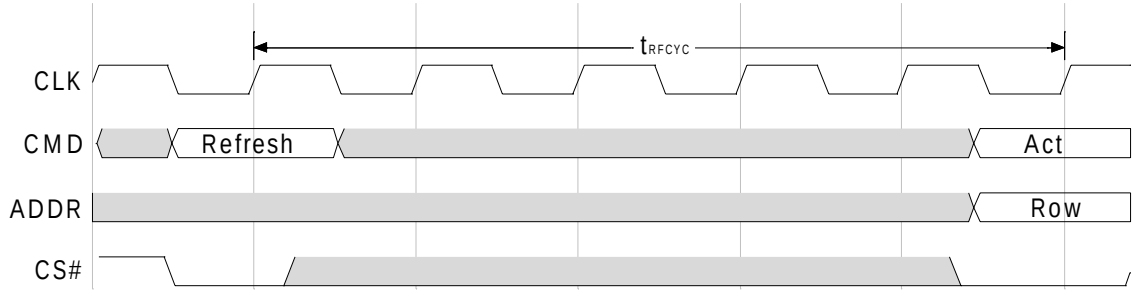
Timing Diagram for t_{LRC}



Timing Diagram for t_{RC}, t_{RAS} and t_{RP}

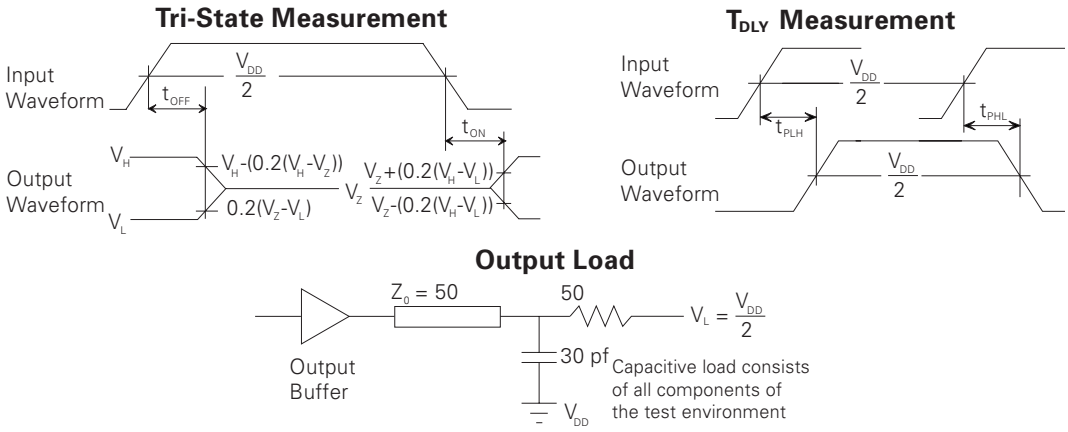


Timing Diagram for t_{BWC} and t_{BPL}



Timing Diagram for t_{RFCYC}

Test and Measurement



Test Structure and Measurement Points

Notes

1 Valid Delay Measurement is made from the VDDQ / 2 on the input waveform to the VDDQ / 2 on the output waveform. Input waveform should have a slew rate of 1V/ns.

2 Tri-state t_{off} measurement is made from the VDDQ/2 on the input waveform to the output waveform moving 20% from its initial to final value VDDQ/2.

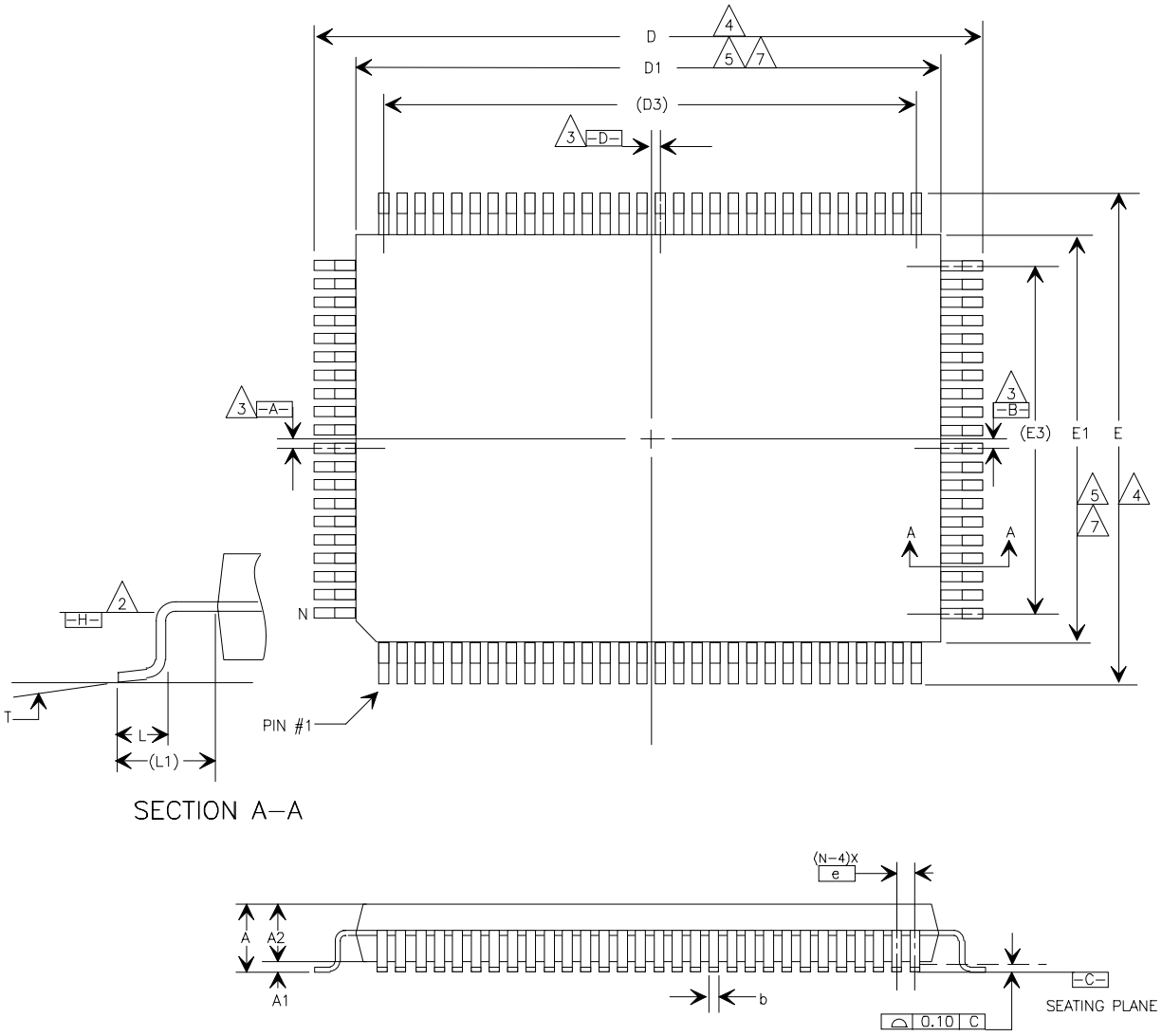
Mechanical Specifications

		Plastic Quad Flatpack (PQFP)		Thin Quad Flatpack (LQFP)	
Symbol	**Description**	**Min**	**Max**	**Min**	**Max**
Ref	Reference Standards	JEDEC MO-108-CC-1 JEDEC MO-108-CC-2 EIAJ QFP1420-065		JEDEC MO-136-DJ	
	Identification	Footprint=3.2 mm		Body Thickness=1.4 mm	
A	Overall Height		3.40		1.60
A1	Stand Off	note 9		note 9	
A2	Body Thickness	2.55	3.05	1.35	1.45
AAA	Lead True Position	0.12		0.1	
b	Lead Width	0.20	0.40	0.20	0.40
C	Lead Thickness	0.13	0.23	0.150	0.188
D	Terminal Dimension	22.95	23.45	21.90	22.10
D1	Package Body	19.90	20.10	19.90	20.10
D3	Reference	18.85 REF.		18.85 REF.	
E	Terminal Dimension	16.95	17.45	15.90	16.10
E1	Package Body	13.90	14.10	13.90	14.10
E3	Reference	12.35 REF.		12.35 REF.	
e	Lead Pitch	0.65		0.65	
L	Foot Length	0.60	1.00	0.45	0.75
L1	Lead Length	1.60 REF		1.00 REF	
T	Lead Angle	0°	10°	0°	10°
N	Lead Count	100		100	
Y	Coplanarity	0.10		0.10	

PQFP and LQFP Package Dimensions

Notes:

1 All dimensions and tolerances conform to ANSI Y14.5M-1982.
2 Datum plan --H-- located at bottom of lead and is coincident with the lead where the lead exits the plastic body at the bottom of the parting line.
3 Datums A--B and --D-- to be determined at datum plane --H-- where the center two leads exit the plastic body.
4 To be determined at seating plane --C--.
5 Dimensions D1 and E1 do not include mold protrusions. Allowable protrusion is 0.25 mm per side. D1 and E1 do include mold mismatch and are determined at datum plane -H-.
6 Details of pin 1 identifier are optional .
7 These dimensions to be determined at datum plane --H--.
8 Controlling dimension: millimeter.
9 0.1 mm stand-off requires capped vias under body with a SMT process that requires cleaning. A 0.25 mm stand-off does not require capped vias. A 0.05 mm or less stand-off is acceptable for a "no-clean" process only.



Packaging Dimensions

PCB Land Pattern

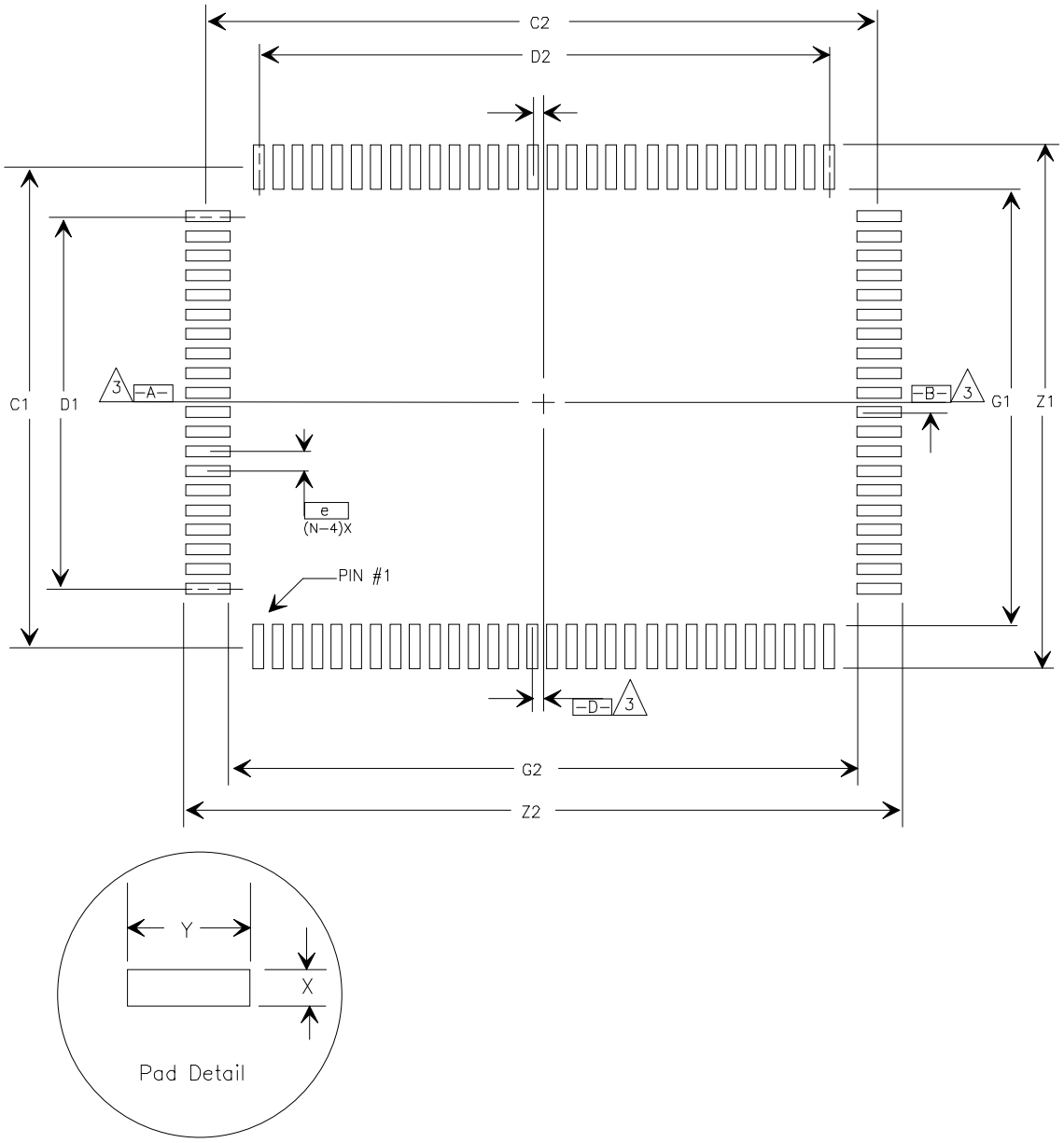
The land pattern shown in Figure 7.2.1 accommodates the QFP and LQFP packages described in 7.1.1 above. Note that the pad required to accommodate the two packages is larger than what would be required if only one package type is accommodated. SMT manufacturing capabilities vary from manufacturer to manufacturer. Check with your SMT processes to ensure that the mounting pad recommended is within your manufacturing process capability.

		QFP	
Symbol	**Description**	**Min**	**Max**
C1	Reference	15.98 REF.	
C2	Reference	21.98 REF.	
D1	Reference	12.35 REF.	
D2	Reference	18.85 REF.	
e	Pad Pitch	0.65	
G1	Pad Inner Dimension	13.69	13.79
G2	Pad inner Dimension	19.69	19.79
N	Pad Count	100	
X	Pad Width	0.35	0.38
Y	Pad Length	2.24 REF.	
Z1	Pad Outer Dimension	18.16	18.26
Z2	Pad Outer Dimension	24.16	24.26

PCB Land Pattern

Notes:

1 All dimensioning and tolerancing conforms to ANSI Y14.5M-1982.
2 Controlling dimension: millimeter.
3 Datums A--B and --D-- to be determined from the center two leads
4 Based on the Surface Mount Design and Land Pattern Standard in IPC-SM-782 revision A, Subsection 11.3, 8/93 for QFP. (IPC is the Institute for Interconnecting and Packaging Electronics Circuits, 7380 N. Lincoln Ave., Lincolnwood, Illinois 60646-1705, Tel. 708 677-2850).



PCB Land Pattern