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July 2017

FDG8850NZ

Dual N-Channel PowerTrench[®] MOSFET

30V,0.75A,0.4Ω

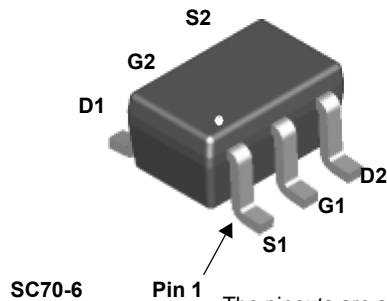
Features

- Max $r_{DS(on)}$ = 0.4Ω at $V_{GS} = 4.5V$, $I_D = 0.75A$
- Max $r_{DS(on)}$ = 0.5Ω at $V_{GS} = 2.7V$, $I_D = 0.67A$
- Very low level gate drive requirements allowing operation in 3V circuits ($V_{GS(th)} < 1.5V$)
- Very small package outline SC70-6
- RoHS Compliant



General Description

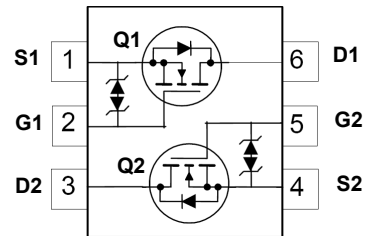
This dual N-Channel logic level enhancement mode field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. This device has been designed especially for low voltage applications as a replacement for bipolar digital transistors and small signal MOSFETs. Since bias resistors are not required, this dual digital FET can replace several different digital transistors, with different bias resistor values.



SC70-6

Pin 1

The pinouts are symmetrical; pin 1 and pin 4 are interchangeable. Units inside the carrier tape can be of either orientation (0 deg and 180 deg) and will not affect the functionality of the device.



MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

| Symbol | Parameter | Ratings | Units |
|----------------|--|-------------|------------------|
| V_{DS} | Drain to Source Voltage | 30 | V |
| V_{GS} | Gate to Source Voltage | ± 12 | V |
| I_D | Drain Current -Continuous | 0.75 | A |
| | -Pulsed | 2.2 | |
| P_D | Power Dissipation for Single Operation | (Note 1a) | W |
| | | (Note 1b) | |
| T_J, T_{STG} | Operating and Storage Junction Temperature Range | -55 to +150 | $^\circ\text{C}$ |

Thermal Characteristics

| | | | | |
|-----------------|--|-----------|-----|--------------------|
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient Single operation | (Note 1a) | 350 | $^\circ\text{C/W}$ |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient Single operation | (Note 1b) | 415 | |

Package Marking and Ordering Information

| Device Marking | Device | Reel Size | Tape Width | Quantity |
|----------------|-----------|-----------|------------|------------|
| .50 | FDG8850NZ | 7" | 8mm | 3000 units |

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|--------------------------------------|---|---|-----|-----|----------|----------------------------|
| BV_{DSS} | Drain to Source Breakdown Voltage | $I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$ | 30 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D = 250\mu\text{A}$, referenced to 25°C | | 25 | | $\text{mV}/^\circ\text{C}$ |
| I_{DSS} | Zero Gate Voltage Drain Current | $V_{DS} = 24\text{V}, V_{GS} = 0\text{V}$ | | | 1 | μA |
| I_{GSS} | Gate to Source Leakage Current | $V_{GS} = \pm 12\text{V}, V_{DS} = 0\text{V}$ | | | ± 10 | μA |

On Characteristics

| | | | | | | |
|--|--|---|------|----------------------|-------------------|----------------------------|
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $V_{GS} = V_{DS}, I_D = 250\mu\text{A}$ | 0.65 | 1.0 | 1.5 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate to Source Threshold Voltage Temperature Coefficient | $I_D = 250\mu\text{A}$, referenced to 25°C | | -3.0 | | $\text{mV}/^\circ\text{C}$ |
| $r_{DS(on)}$ | Static Drain to Source On Resistance | $V_{GS} = 4.5\text{V}, I_D = 0.75\text{A}$ $V_{GS} = 2.7\text{V}, I_D = 0.67\text{A}$ $V_{GS} = 4.5\text{V}, I_D = 0.75\text{A}, T_J = 125^\circ\text{C}$ | | 0.25 0.29 0.36 | 0.4 0.5 0.6 | Ω |
| g_{FS} | Forward Transconductance | $V_{DS} = 5\text{V}, I_D = 0.75\text{A}$ | | 3 | | S |

Dynamic Characteristics

| | | | | | | |
|-----------|------------------------------|--|--|----|-----|----|
| C_{iss} | Input Capacitance | $V_{DS} = 10\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$ | | 90 | 120 | pF |
| C_{oss} | Output Capacitance | | | 20 | 30 | pF |
| C_{rss} | Reverse Transfer Capacitance | | | 15 | 25 | pF |

Switching Characteristics (note 2)

| | | | | | | |
|--------------|-------------------------------|---|--|------|------|----|
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD} = 5\text{V}, I_D = 0.5\text{A},$ $V_{GS} = 4.5\text{V}, R_{GEN} = 6\Omega$ | | 4 | 10 | ns |
| t_r | Rise Time | | | 1 | 10 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | | 9 | 18 | ns |
| t_f | Fall Time | | | 1 | 10 | ns |
| Q_g | Total Gate Charge | | | 1.03 | 1.44 | nC |
| Q_{gs} | Gate to Source Charge | $V_{GS} = 4.5\text{V}, V_{DD} = 5\text{V}, I_D = 0.75\text{A}$ | | 0.29 | | nC |
| Q_{gd} | Gate to Drain "Miller" Charge | | | 0.17 | | nC |

Drain-Source Diode Characteristics and Maximum Ratings

| | | | | | | |
|----------|---|--|--|------|-----|---|
| I_S | Maximum Continuous Drain-Source Diode Forward Current | | | 0.3 | A | |
| V_{SD} | Source to Drain Diode Forward Voltage | $V_{GS} = 0\text{V}, I_S = 0.3\text{A}$ (Note 2) | | 0.76 | 1.2 | V |

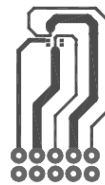
Notes:

- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



Scale 1:1 on letter size paper.

a. $350^\circ\text{C}/\text{W}$ when mounted on a 1 in^2 pad of 2 oz copper.



b. $415^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper.

- Pulse Test: Pulse Width < $300\mu\text{s}$, Duty cycle < 2.0%.

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

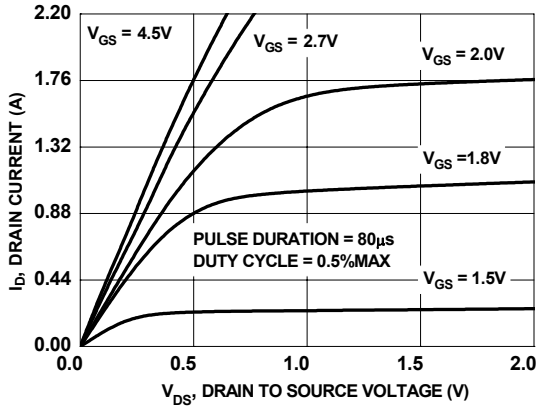


Figure 1. On-Region Characteristics

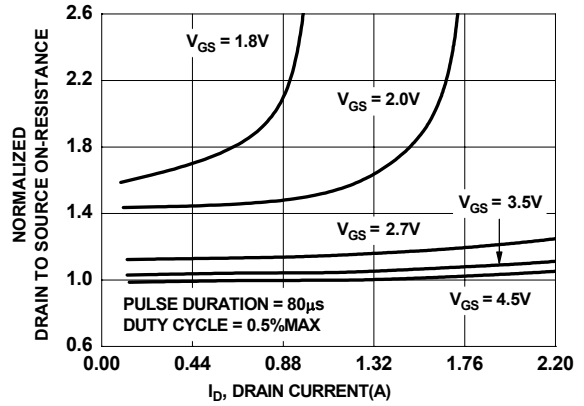


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

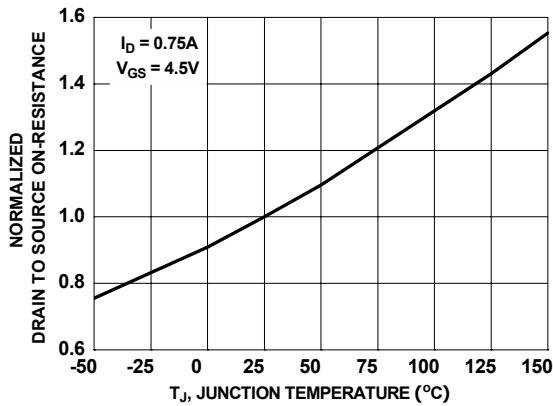


Figure 3. Normalized On-Resistance vs Junction Temperature

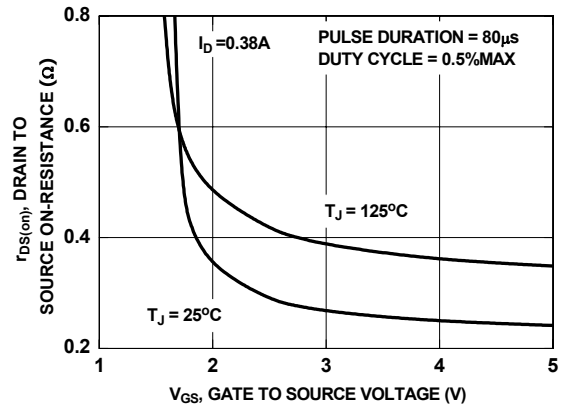


Figure 4. On-Resistance vs Gate to Source Voltage

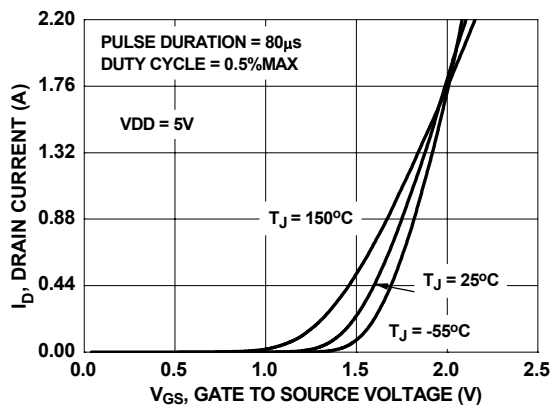


Figure 5. Transfer Characteristics

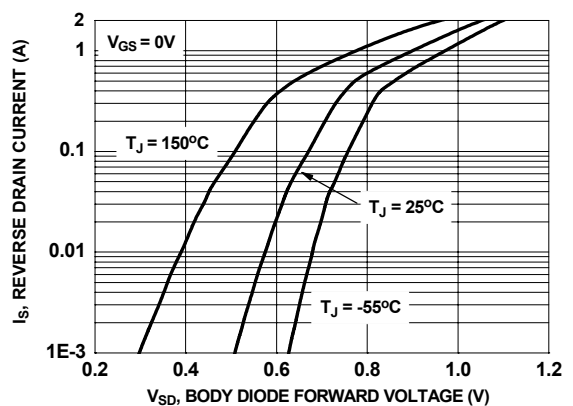


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

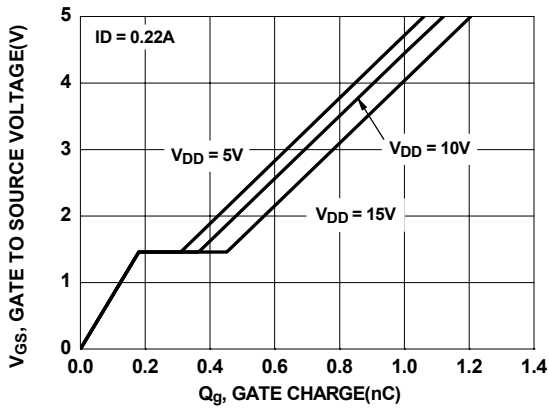


Figure 7. Gate Charge Characteristics

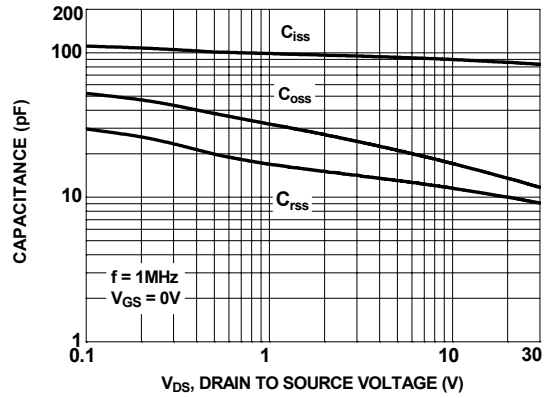


Figure 8. Capacitance vs Drain to Source Voltage

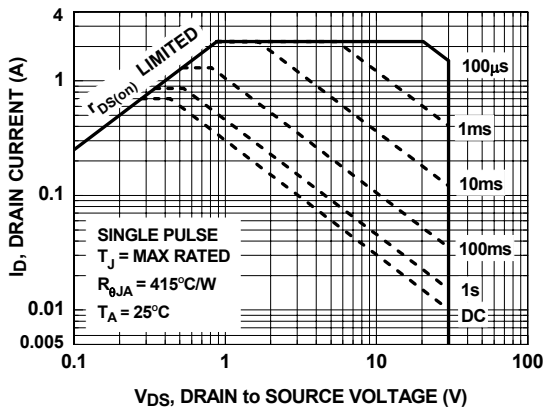


Figure 9. Forward Bias Safe Operating Area

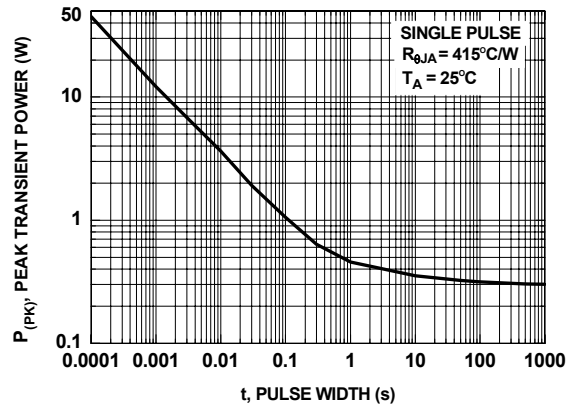


Figure 10. Single Pulse Maximum Power Dissipation

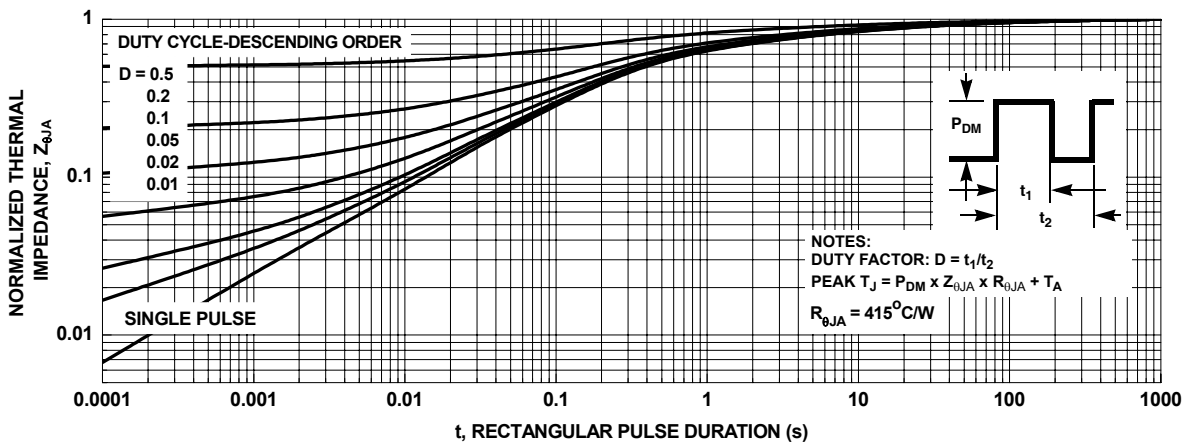
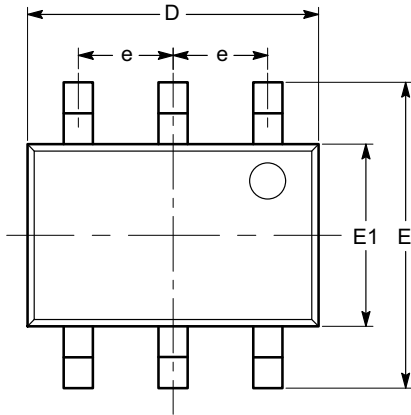


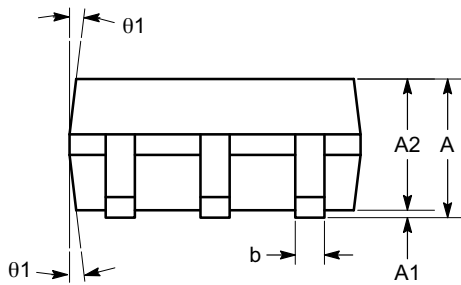
Figure 11. Transient Thermal Response Curve

SC-88 (SC-70 6 Lead), 1.25x2
CASE 419AD-01
ISSUE A

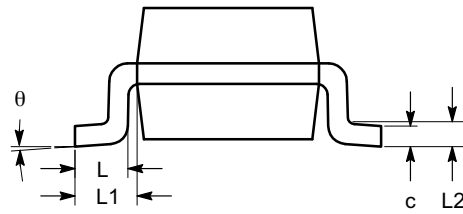


TOP VIEW

| SYMBOL | MIN | NOM | MAX |
|------------|----------|------|------|
| A | 0.80 | | 1.10 |
| A1 | 0.00 | | 0.10 |
| A2 | 0.80 | | 1.00 |
| b | 0.15 | | 0.30 |
| c | 0.10 | | 0.18 |
| D | 1.80 | 2.00 | 2.20 |
| E | 1.80 | 2.10 | 2.40 |
| E1 | 1.15 | 1.25 | 1.35 |
| e | 0.65 BSC | | |
| L | 0.26 | 0.36 | 0.46 |
| L1 | 0.42 REF | | |
| L2 | 0.15 BSC | | |
| θ | 0° | | 8° |
| $\theta 1$ | 4° | | 10° |




SIDE VIEW



END VIEW

Notes:

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MO-203.

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