TPS82130 17-V Input 3-A Step-Down Converter MicroSiP™ Module with Integrated Inductor

1 Features

- 3-mm × 2.8-mm × 1.5-mm MicroSiP™ Package
- 3-V to 17-V Input Range
- 3-A Continuous Output Current
- DCS-Control™ Topology
- Power Save Mode for Light Load Efficiency
- 20-µA Operating Quiescent Current
- 0.9-V to 6-V Adjustable Output Voltage
- 100% Duty Cycle for Lowest Dropout
- Power Good Output
- Programmable Soft Start-up with Tracking
- Thermal Shutdown Protection
- –40°C to 125°C Operating Temperature Range
- Create a Custom Design using the TPS82130 with the WEBENCH® Power Designer

2 Applications

- Industrial Applications
- Telecom and Networking Applications
- Solid State Drives

3 Description

The TPS82130 is a 17-V input 3-A step-down converter MicroSiP™ power module optimized for small solution size and high efficiency. The module integrates a synchronous step-down converter and an inductor to simplify design, reduce external components and save PCB area. The low profile and compact solution is suitable for automated assembly by standard surface mount equipment.

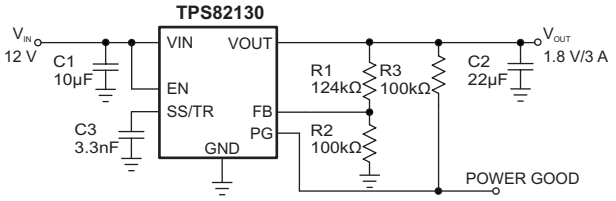
To maximize efficiency, the converter operates in PWM mode with a nominal switching frequency of 2 MHz and automatically enters power save mode operation at light load currents. In power-save mode, the device operates with typically 20-µA quiescent current. Using the DCS-Control™ topology, the device achieves excellent load transient performance and accurate output voltage regulation.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS82130	µSiL (8)	3.00 mm × 2.80 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic
1.8-V Output Application



12-V Input Voltage Efficiency

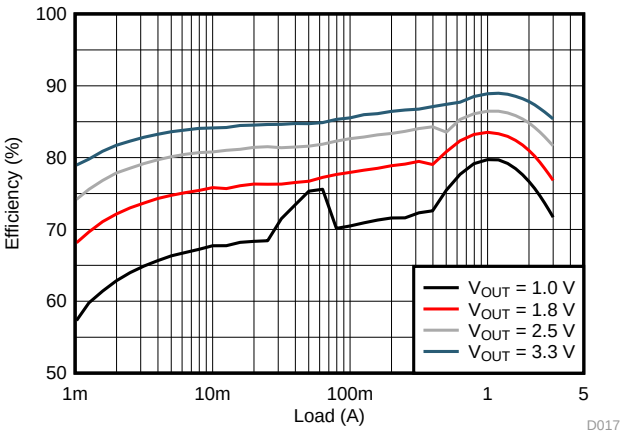


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (January 2017) to Revision D — **Page**

- Added Tape and Reel Information ... 22

Changes from Revision B (August 2016) to Revision C — **Page**

- Added WEBENCH information to the *Features*, *Detailed Design Procedure*, and *Device Support* sections ... 1
- Changed the Output voltage MAX value From: 5 V to: 6 V in the *Recommend Operating Conditions* table ... 4
- Added Table 1, Power Good Pin Logic ... 10

Changes from Revision A (February 2015) to Revision B — **Page**

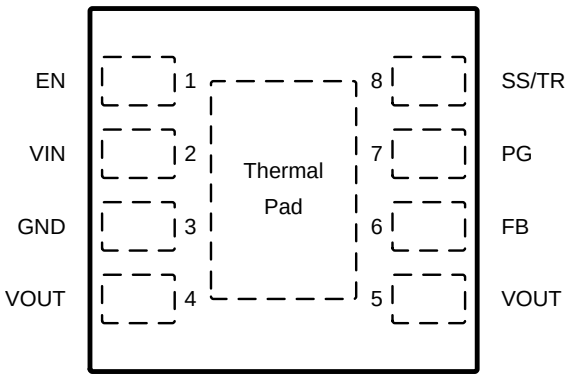
- Changed storage temperature to -55°C from -40°C ... 4
- Updated thermal information ... 4
- Added FB voltage accuracy at T_J = 0°C to 85°C condition ... 5
- Changed derating curve based on ambient temperature ... 13
- Changed derating curve based on ambient temperature ... 13
- Added derating curve for V_{OUT} = 1.0 V ... 14
- Deleted Thermal pictures ... 17
- Added "Receiving Notification of Documentation Updates" section. ... 18

Changes from Original (December 2015) to Revision A — **Page**

- Production Data release ... 1

5 Pin Configuration and Functions

8-Pin µSiL Package
(SIL0008C Top View)



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	1	I	Enable pin. Pull High to enable the device. Pull Low to disable the device. This pin has an internal pull-down resistor of typically 400 kΩ when the device is disabled.
VIN	2	PWR	Input pin.
GND	3		Ground pin.
VOUT	4, 5	PWR	Output pin.
FB	6	I	Feedback reference pin. An external resistor divider connected to this pin programs the output voltage.
PG	7	O	Power good open drain output pin. A pull-up resistor can be connected to any voltage less than 6V. Leave it open if it is not used.
SS/TR	8	I	Soft startup and voltage tracking pin. An external capacitor connected to this pin sets the internal reference voltage rising time.
Exposed Thermal Pad			The exposed thermal pad must be connected to the GND pin. Must be soldered to achieve appropriate power dissipation and mechanical reliability.

6 Specifications

6.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
Voltage at pins(2)	VIN	-0.3	20	V
	EN, SS/TR	-0.3	V_{IN} + 0.3	
	PG, FB	-0.3	7	
	VOUT	0	7	
Sink current	PG		10	mA
Module operating temperature		–40	125	°C
Storage temperature		–55	125	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground pin.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommend Operating Conditions

Over operating free-air temperature range, unless otherwise noted.

		MIN	MAX	UNIT
V_{IN}	Input voltage	3	17	V
V_{PG}	Power good pull-up resistor voltage		6	V
V_{OUT}	Output voltage	0.9	6	V
I_{OUT}	Output current	0	3	A
T_J	Module operating temperature range for 100,000 hours lifetime(1)	-40	110	°C

(1) The module operating temperature range includes module self temperature rise and IC junction temperature rise. In applications where high power dissipation is present, the maximum operating temperature or maximum output current must be derated. For applications where the module operates continuously at 125 °C temperature, the maximum lifetime is reduced to 50,000 hours.

6.4 Thermal Information

THERMAL METRIC(1)		TPS82130 (JEDEC 51-5)	TPS82130EVM-720	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	58.2	46.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	9.4	9.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14.4	14.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.9	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	14.2	14.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	21.3	21.3	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report. Theta-JA can be improved with a custom PCB design containing thermal vias where possible.

6.5 Electrical Characteristics

T_J = -40°C to 125°C and V_{IN} = 3.0V to 17V. Typical values are at T_J = 25°C and V_{IN} = 12V, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY							
I_Q	Quiescent current into VIN	No load, device not switching			20	35	µA
I_{SD}	Shutdown current into VIN	EN = Low			1.5	7.4	µA
V_{UVLO}	Under voltage lock out threshold	V_{IN} falling		2.6	2.7	2.8	V
		V_{IN} rising		2.8	2.9	3.0	V
T_{JSD}	Thermal shutdown threshold	T_J rising			160		°C
		T_J falling			140		°C
LOGIC INTERFACE (EN)							
V_{IH}	High-level input voltage			0.9	0.65		V
V_{IL}	Low-level input voltage				0.45	0.3	V
$I_{lkg(EN)}$	Input leakage current into EN pin	EN = High			0.01	1	µA
CONTROL (SS/TR, PG)							
$I_{SS/TR}$	SS/TR pin source current			2.1	2.5	2.8	µA
V_{PG}	Power good threshold	V_{OUT} rising, referenced to V_{OUT} nominal		92%	95%	99%	
		V_{OUT} falling, referenced to V_{OUT} nominal		87%	90%	94%	
$V_{PG,OL}$	Power good low-level voltage	I_{sink} = 2mA			0.1	0.3	V
$I_{lkg(PG)}$	Input leakage current into PG pin	V_{PG} = 1.8V			1	400	nA
OUTPUT							
V_{FB}	Feedback regulation voltage	PWM mode		785	800	815	mV
			T_J = 0°C to 85°C	788	800	812	
		PSM	C_{OUT} = 22 µF	785	800	823	
			C_{OUT} = 2x22 µF, T_J = 0°C to 85°C	788	800	815	
$I_{lkg(FB)}$	Feedback input leakage current	V_{FB} = 0.8V			1	100	nA
	Line regulation	I_{OUT} = 1A, V_{OUT} = 1.8V			0.002		%/V
	Load regulation	I_{OUT} = 0.5A to 3A, V_{OUT} = 1.8V			0.12		%/A
POWER SWITCH							
$R_{DS(on)}$	High-side FET on-resistance	I_{SW} = 500mA, V_{IN} ≥ 6V			90	170	mΩ
		I_{SW} = 500mA, V_{IN} = 3V			120		
	Low-side FET on-resistance	I_{SW} = 500mA, V_{IN} ≥ 6V			40	70	
		I_{SW} = 500mA, V_{IN} = 3V			50		
R_{DP}	Dropout resistance	100% mode, V_{IN} ≥ 6V			125		mΩ
		100% mode, V_{IN} = 3V			160		
I_{LIMF}	High-side FET switch current limit	V_{IN} = 6V, T_A = 25°C		3.6	4.2	4.9	A
f_{SW}	PWM switching frequency	I_{OUT} = 1A, V_{OUT} = 1.8V			2.0		MHz

6.6 Typical Characteristics

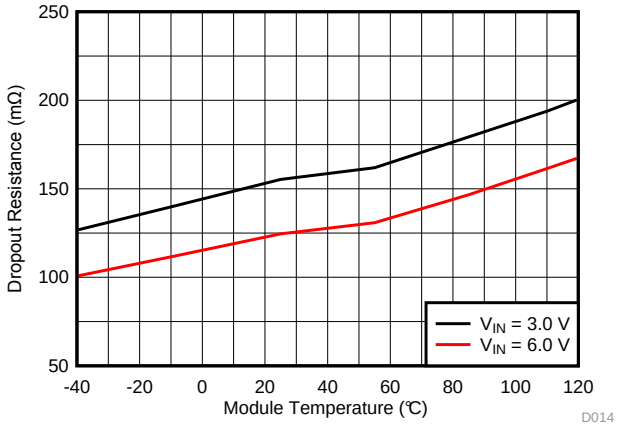


Figure 1. Dropout Resistance

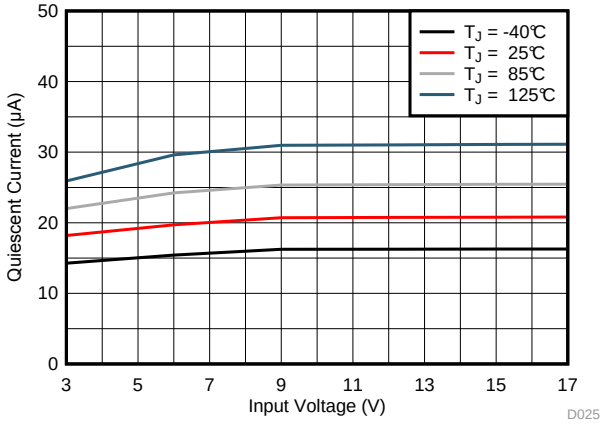


Figure 2. Quiescent Current

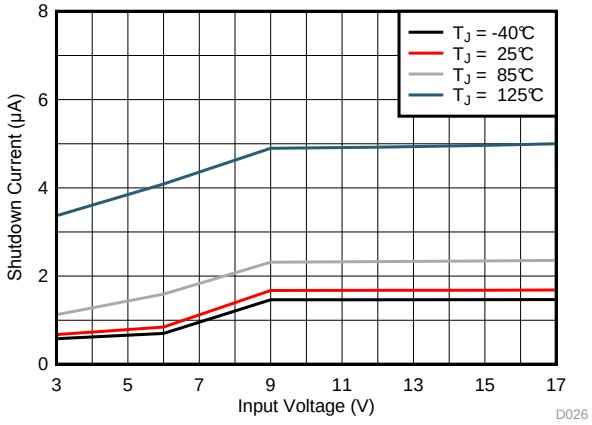


Figure 3. Shutdown Current

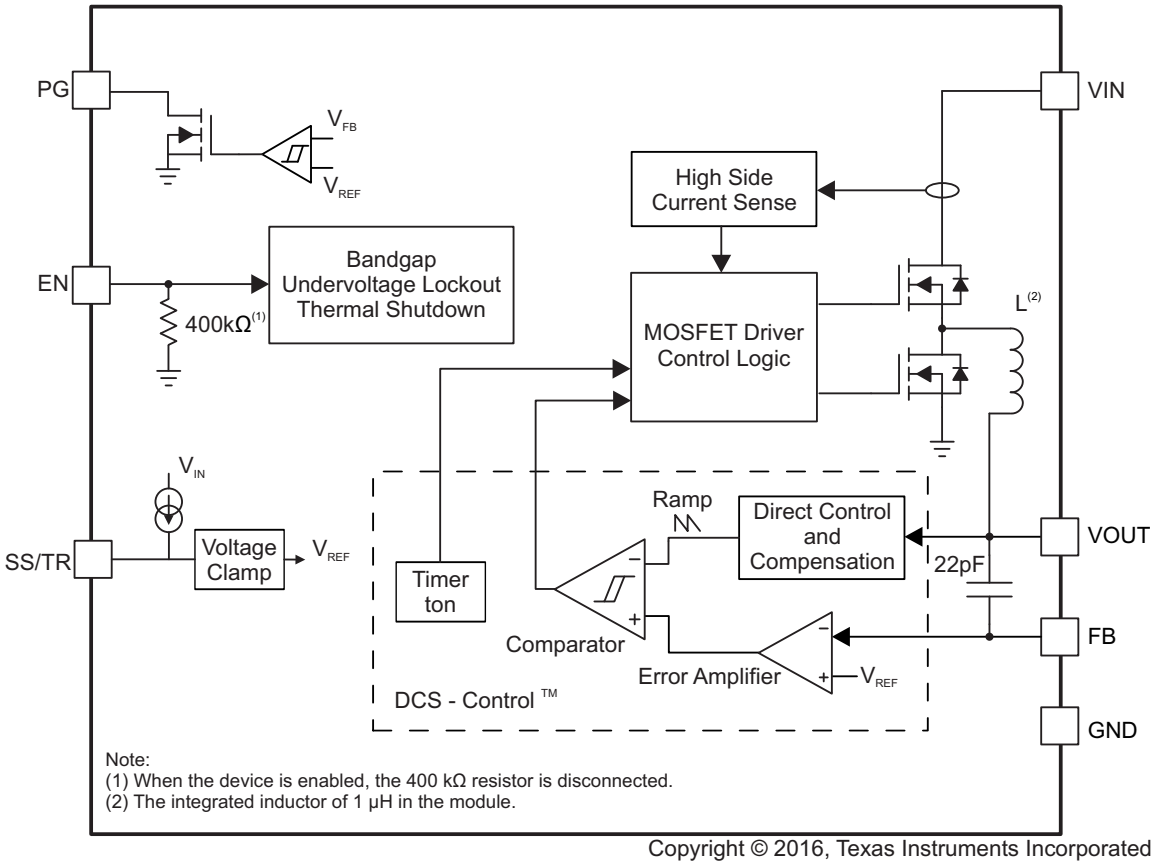
7 Detailed Description

7.1 Overview

The TPS82130 synchronous step-down converter MicroSiP™ power module is based on DCS-Control™ (Direct Control with Seamless transition into Power Save Mode). This is an advanced regulation topology that combines the advantages of hysteretic and voltage mode control.

The DCS-Control™ topology operates in PWM (Pulse Width Modulation) mode for medium to heavy load conditions and in PSM (Power Save Mode) at light load currents. In PWM mode, the converter operates with its nominal switching frequency of 2.0MHz having a controlled frequency variation over the input voltage range. As the load current decreases, the converter enters Power Save Mode, reducing the switching frequency and minimizing the IC's quiescent current to achieve high efficiency over the entire load current range. DCS-Control™ supports both operation modes using a single building block and therefore has a seamless transition from PWM to PSM without effects on the output voltage. The TPS82130 offers excellent DC voltage regulation and load transient regulation, combined with low output voltage ripple, minimizing interference with RF circuits.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 PWM and PSM Operation

The TPS82130 includes an on-time (t_{ON}) circuitry. This t_{ON}, in steady-state operation in PWM and PSM modes, is estimated as:

$$t_{ON} = 500ns \times \frac{V_{OUT}}{V_{IN}} \quad (1)$$

Feature Description (continued)

In PWM mode, the TPS82130 operates with pulse width modulation in continuous conduction mode (CCM) with a t_{ON} shown in Equation 1 at medium and heavy load currents. A PWM switching frequency of typically 2.0MHz is achieved by this t_{ON} circuitry. The device operates in PWM mode as long as the output current is higher than half the inductor's ripple current estimated by Equation 2.

$$\Delta I_L = t_{ON} \times \frac{V_{IN} - V_{OUT}}{L} \quad (2)$$

To maintain high efficiency at light loads, the device enters Power Save Mode seamlessly when the load current decreases. This happens when the load current becomes smaller than half the inductor's ripple current. In PSM, the converter operates with reduced switching frequency and with a minimum quiescent current to maintain high efficiency. PSM is also based on the t_{ON} circuitry. The switching frequency in PSM is estimated as:

$$f_{PSM} = \frac{2 \times I_{OUT}}{t_{ON}^2 \times \frac{V_{IN}}{V_{OUT}} \times \frac{V_{IN} - V_{OUT}}{L}} \quad (3)$$

In PSM, the output voltage rises slightly above the nominal output voltage in PWM mode. This effect is reduced by increasing the output capacitance. The output voltage accuracy in PSM operation is reflected in the electrical specification table and given for a 22-µF output capacitor.

For very small output voltages, an absolute minimum on-time of about 80ns is kept to limit switching losses. The operating frequency is thereby reduced from its nominal value, which keeps efficiency high. Also the off-time can reach its minimum value at high duty cycles. The output voltage remains regulated in such cases.

When V_{IN} decreases to typically 15% above V_{OUT}, the TPS82130 can't enter Power Save Mode, regardless of the load current. The device maintains output regulation in PWM mode.

7.3.2 Low Dropout Operation (100% Duty Cycle)

The TPS82130 offers a low input to output voltage differential by entering 100% duty cycle mode. In this mode, the high-side MOSFET switch is constantly turned on. This is particularly useful in battery powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range. The minimum input voltage to maintain a minimum output voltage is given by:

$$V_{IN(min)} = V_{OUT(min)} + I_{OUT} \times R_{DP} \quad (4)$$

Where

R_{DP} = Resistance from V_{IN} to V_{OUT}, including high-side FET on-resistance and DC resistance of the inductor

$V_{OUT(min)}$ = Minimum output voltage the load can accept.

7.3.3 Switch Current Limit

The switch current limit prevents the device from high inductor current and from drawing excessive current from the battery or input voltage rail. Excessive current might occur with a heavy load/shorted output circuit condition. If the inductor peak current reaches the switch current limit after a propagation delay of typically 30 ns, the high-side FET is turned off and the low-side FET is turned on to ramp down the inductor current.

7.3.4 Undervoltage Lockout

To avoid mis-operation of the device at low input voltages, an under voltage lockout is implemented, which shuts down the devices at voltages lower than V_{UVLO} with a hysteresis of 200 mV.

7.3.5 Thermal Shutdown

The device goes into thermal shutdown and stops switching once the junction temperature exceeds T_{JSD}. Once the device temperature falls below the threshold by 20°C, the device returns to normal operation automatically.

7.4 Device Functional Modes

7.4.1 Enable and Disable (EN)

The device is enabled by setting the EN pin to a logic High. Accordingly, the shutdown mode is forced if the EN pin is pulled Low with a shutdown current of typically 1.5 μA.

An internal pull-down resistor of 400kΩ is connected to the EN pin when the EN pin is Low. The pulldown resistor is disconnected when the EN pin is High.

7.4.2 Soft Startup (SS/TR)

The internal voltage clamp controls the output voltage slope during startup. This avoids excessive inrush current and ensures a controlled output voltage rise time. When the EN pin is pulled high, the device starts switching after a delay of typically 55μs and the output voltage rises with a slope controlled by an external capacitor connected to the SS/TR pin. Using a very small capacitor or leaving the SS/TR pin floating provides fastest startup time.

The TPS82130 is able to start into a pre-biased output capacitor. During the pre-biased startup, both the power MOSFETs are not allowed to turn on until the internal voltage clamp sets an output voltage above the pre-bias voltage.

When the device is in shutdown, undervoltage lockout or thermal shutdown, the capacitor connected to SS/TR pin is discharged by an internal resistor. Returning from those states causes a new startup sequence.

7.4.3 Voltage Tracking (SS/TR)

The SS/TR pin is externally driven by another voltage source to achieve output voltage tracking. The application circuit is shown in Figure 4.

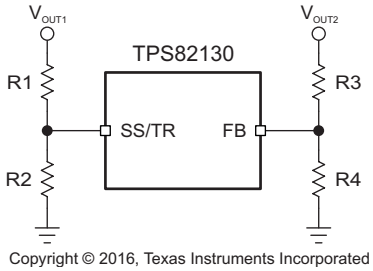


Figure 4. Output Voltage Tracking

When the SS/TR pin voltage is between 50 mV and 1.2 V, the VOUT2 tracks the VOUT1 as described in Equation 5.

$$\frac{V_{OUT2}}{V_{OUT1}} \approx 0.64 \times \frac{R2}{R1+R2} \times \frac{R3+R4}{R4} \quad (5)$$

When the SS/TR pin voltage is above 1.2 V, the voltage tracking is disabled and the FB pin voltage is regulated at 0.8 V. For decreasing SS/TR pin voltage, the device doesn't sink current from the output. So the resulting decreases of the output voltage may be slower than the SS/TR pin voltage if the load is light. When driving the SS/TR pin with an external voltage, do not exceed the voltage rating of the SS/TR pin which is VIN+0.3V.

Details about tracking and sequencing circuits are found in SLVA470.

Device Functional Modes (continued)

7.4.4 Power Good Output (PG)

The device has a power good (PG) output. The PG pin goes high impedance once the output is above 95% of the nominal voltage, and is driven low once the output voltage falls below typically 90% of the nominal voltage. The PG pin is an open drain output and is specified to sink up to 2 mA. The power good output requires a pull-up resistor connecting to any voltage rail less than 6 V.

The PG signal can be used for sequencing of multiple rails by connecting it to the EN pin of other converters. Leave the PG pin floating when it is not used. Table 1 shows the PG pin logic.

Table 1. Power Good Pin Logic

Device State		PG Logic Status	
		High Impedance	Low
Enable (EN=High)	$V_{FB} \geq V_{TH\_PG}$	√	
	$V_{FB} \leq V_{TH\_PG}$		√
Shutdown (EN=Low)			√
UVLO	$0.7\ V < V_{IN} < V_{UVLO}$		√
Thermal Shutdown	$T_J > T_{SD}$		√
Power Supply Removal	$V_{IN} < 0.7\ V$	√	

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The output voltage of the TPS82130 is adjusted by component selection. The following section discusses the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference.

8.2 Typical Applications

8.2.1 1.8-V Output Application

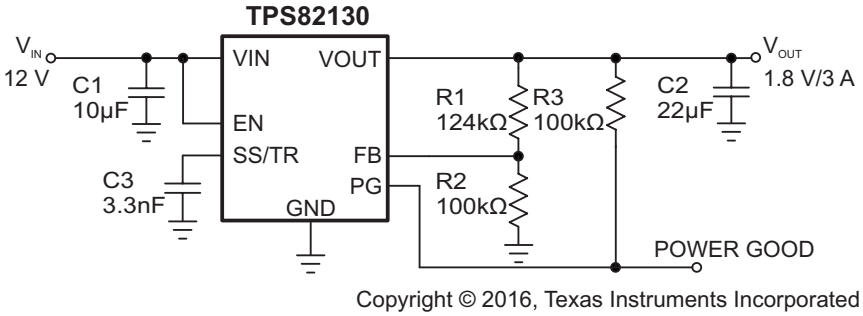


Figure 5. 1.8-V Output Application

8.2.1.1 Design Requirements

For this design example, use the following as the input parameters.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	12V
Output voltage	1.8V
Output ripple voltage	< 20mV
Output current rating	3A

The components used for measurements are given in the following table.

Table 3. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER
C1	10 µF, 25 V, X7R, ±20%, size 1206, C3216X7R1E106M160AE	TDK
C2	22 µF, 10 V, ±20%, X7S, size 0805, C2012X7S1A226M125AC	TDK
C3	3300 pF, 50 V, ±5%, C0G/NP0, size 0603, GRM1885C1H332JA01D	Murata
R1, R2, R3	Standard	

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Custom Design with WEBENCH® Tools

Click here to create a custom design using the TPS82130 device with the WEBENCH® Power Designer.

1. Start by entering your V_{IN}, V_{OUT}, and I_{OUT} requirements.
2. Optimize your design for key parameters like efficiency, footprint and cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. The WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you will also be able to:
   - Run electrical simulations to see important waveforms and circuit performance
   - Run thermal simulations to understand the thermal performance of your board
   - Export your customized schematic and layout into popular CAD formats
   - Print PDF reports for the design, and share your design with colleagues
5. Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.1.2.2 Setting the Output Voltage

The output voltage is set by an external resistor divider according to the following equations:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) = 0.8\ V \times \left(1 + \frac{R1}{R2}\right) \quad (6)$$

R2 should not be higher than 100kΩ to achieve high efficiency at light load while providing acceptable noise sensitivity. Larger currents through R2 improve noise sensitivity and output voltage accuracy. Figure 5 shows the external resistor divider value for a 1.8-V output. Choose appropriate resistor values for other outputs.

In case the FB pin gets opened, the device clamps the output voltage at the VOUT pin internally to about 7V.

8.2.1.2.3 Input and Output Capacitor Selection

For best output and input voltage filtering, low ESR ceramic capacitors are required. The input capacitor minimizes input voltage ripple, suppresses input voltage spikes and provides a stable system rail for the device. A 10-µF or larger input capacitor is required. The output capacitor value can range from 22µF up to more than 400µF. Higher values are possible as well and can be evaluated through the transient response. Larger soft start times are recommended for higher output capacitances.

High capacitance ceramic capacitors have a DC bias effect, which will have a strong influence on the final effective capacitance. Therefore the right capacitor value has to be chosen carefully. Package size and voltage rating in combination with dielectric material are responsible for differences between the rated capacitor value and the effective capacitance.

8.2.1.2.4 Soft Start-up Capacitor Selection

A capacitance connected between the SS/TR pin and the GND allows programming the startup slope of the output voltage. A constant current of 2.5 µA charges the external capacitor. The capacitance required for a given soft startup time for the output voltage is given by:

$$C_{SS/TR} = t_{SS/TR} \times \frac{I_{SS/TR}}{1.25V} \quad (7)$$

8.2.1.3 Application Performance Curves

T_A = 25°C, V_{IN} = 12 V, V_{OUT} = 1.8 V, unless otherwise noted.

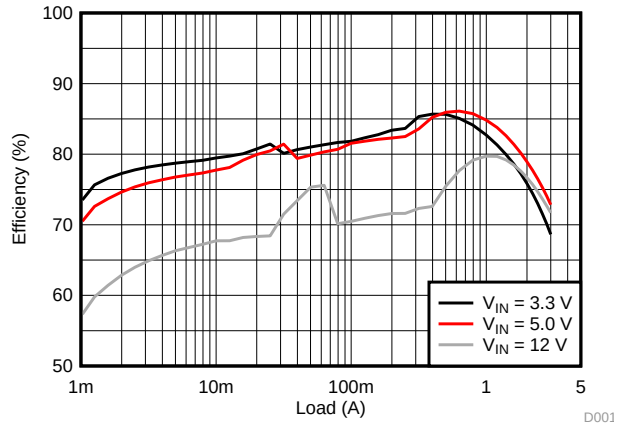


Figure 6. Efficiency, V_{OUT} = 1 V

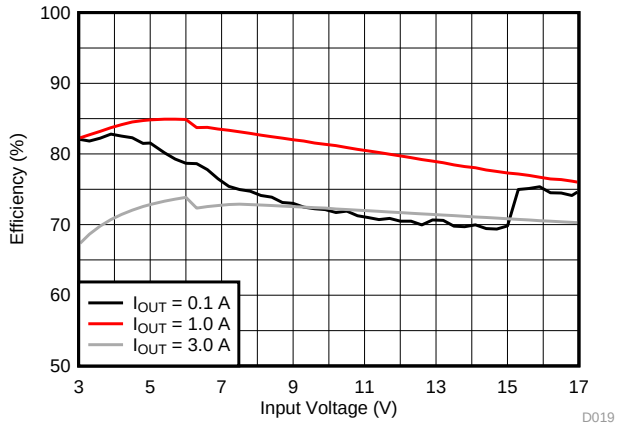


Figure 7. Efficiency, V_{OUT} = 1.0 V

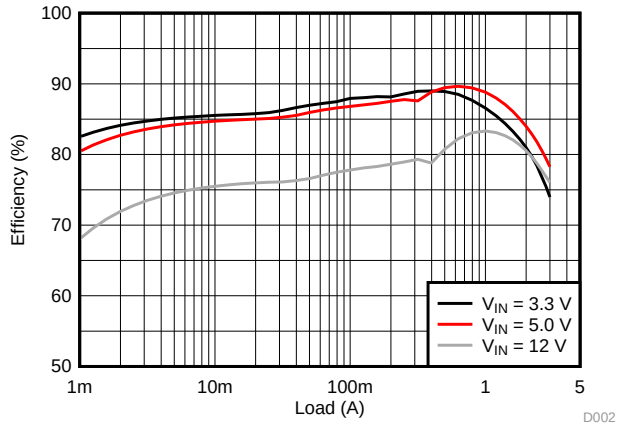


Figure 8. Efficiency, V_{OUT} = 1.8 V

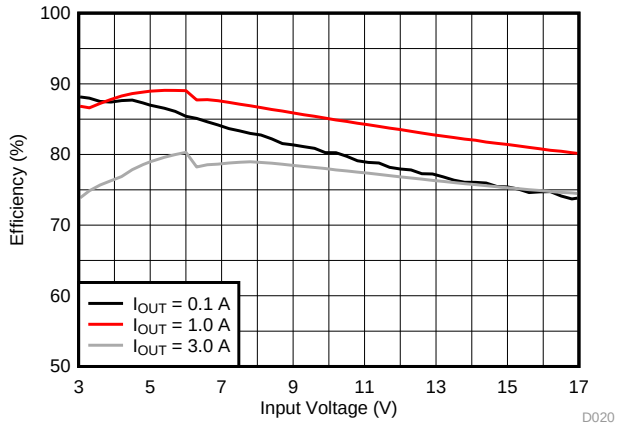


Figure 9. Efficiency, V_{OUT} = 1.8 V

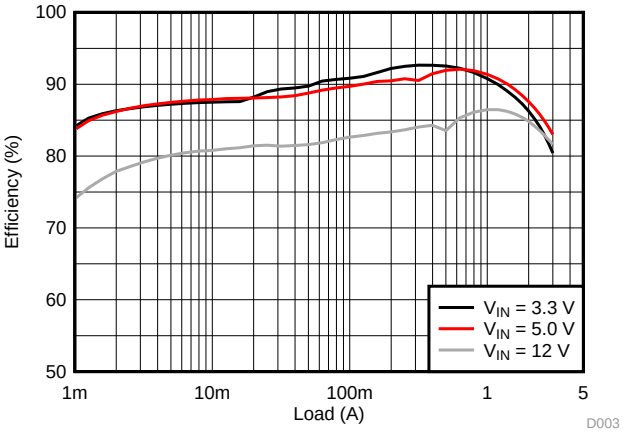


Figure 10. Efficiency, V_{OUT} = 2.5 V

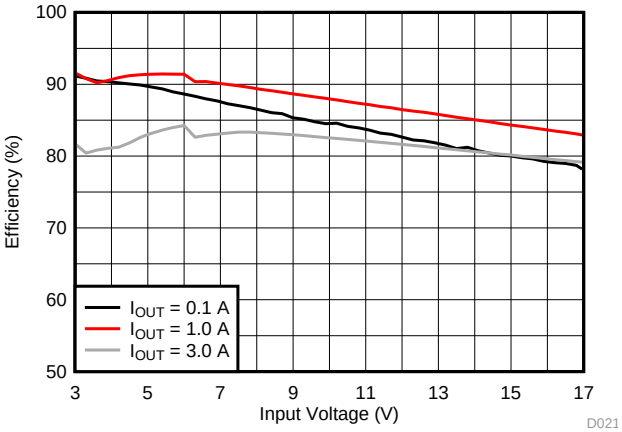


Figure 11. Efficiency, V_{OUT} = 2.5 V

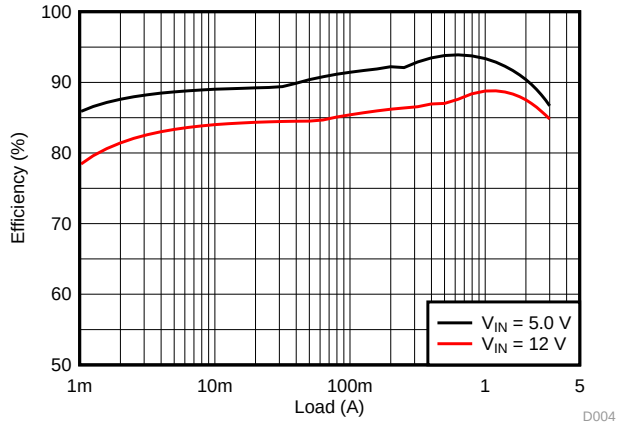


Figure 12. Efficiency, V_{OUT} = 3.3 V

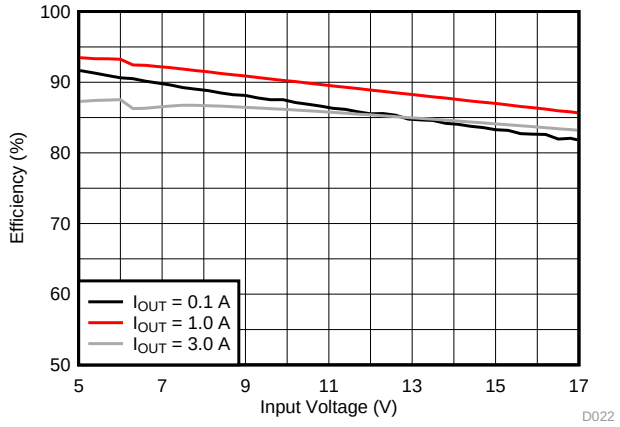


Figure 13. Efficiency, V_{OUT} = 3.3 V

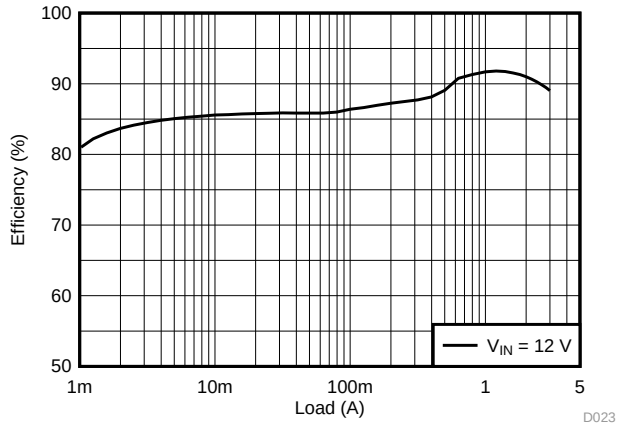


Figure 14. Efficiency, V_{OUT} = 5.0 V

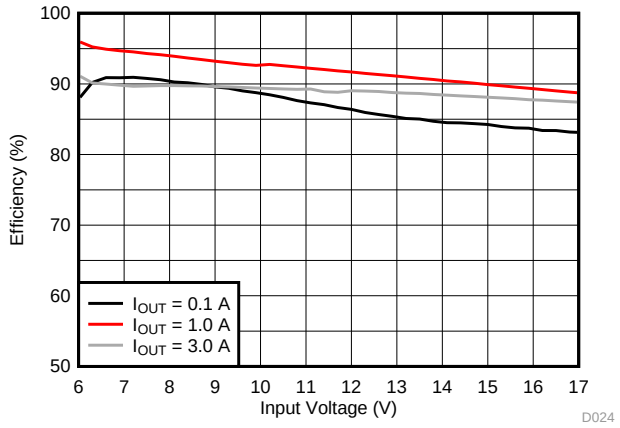
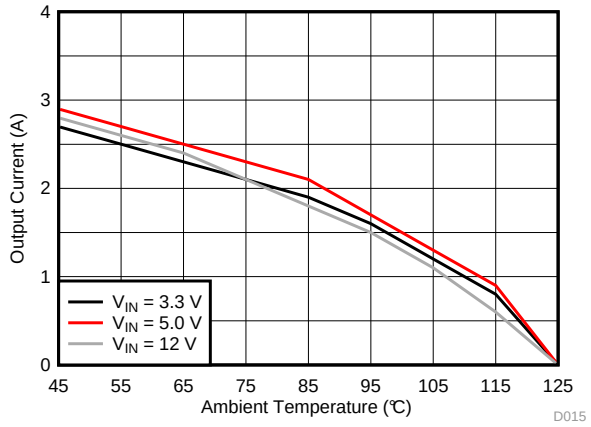
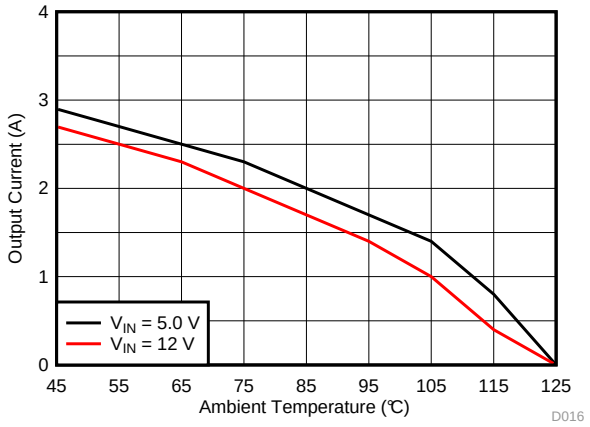


Figure 15. Efficiency, V_{OUT} = 5 V



V_{OUT} = 1.8V θ_{JA} = 46.1 °C/W

Figure 16. Thermal Derating, V_{OUT} = 1.8 V



V_{OUT} = 3.3V θ_{JA} = 46.1 °C/W

Figure 17. Thermal Derating, V_{OUT} = 3.3 V

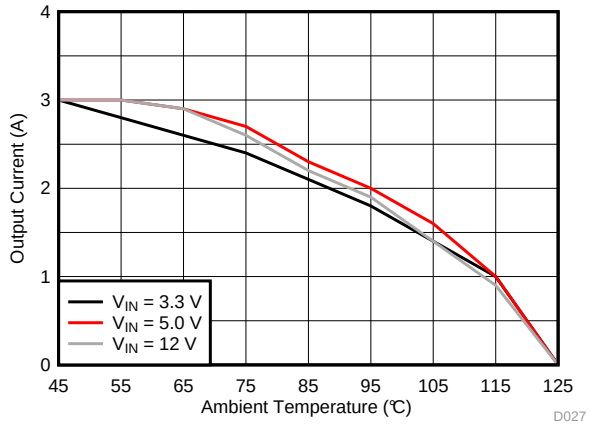
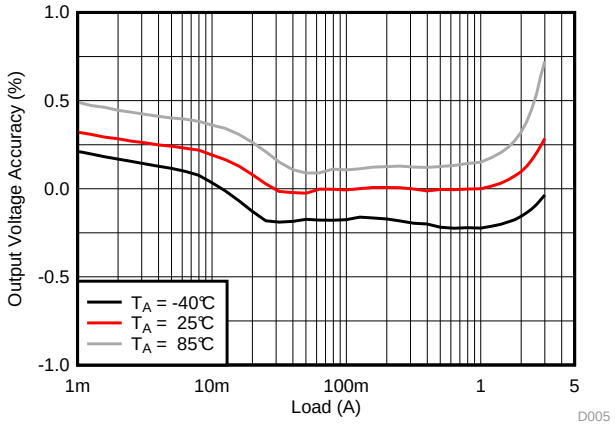
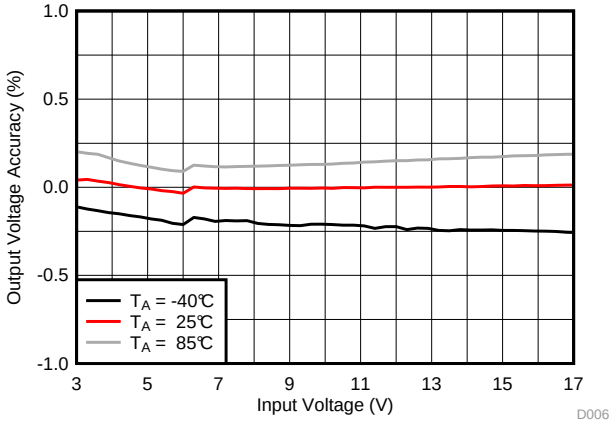


Figure 18. Thermal Derating, V_{OUT} = 1.0 V



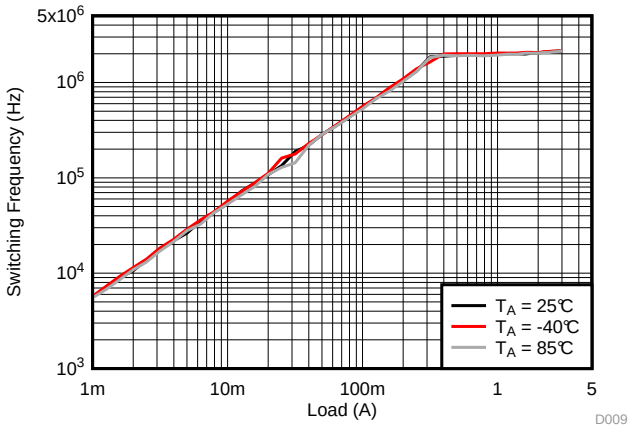
V_{IN} = 12V

Figure 19. Load Regulation



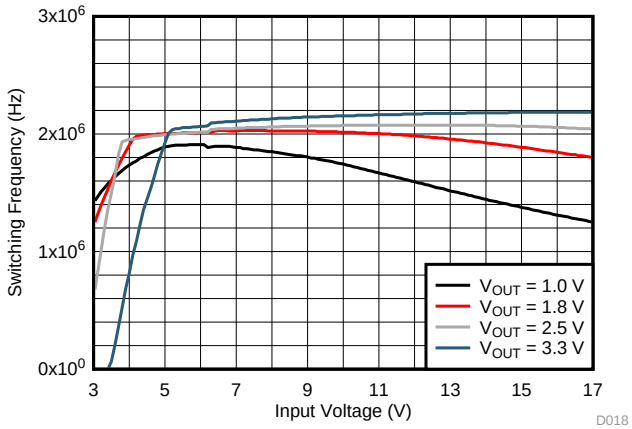
I_{OUT} = 1A

Figure 20. Line Regulation



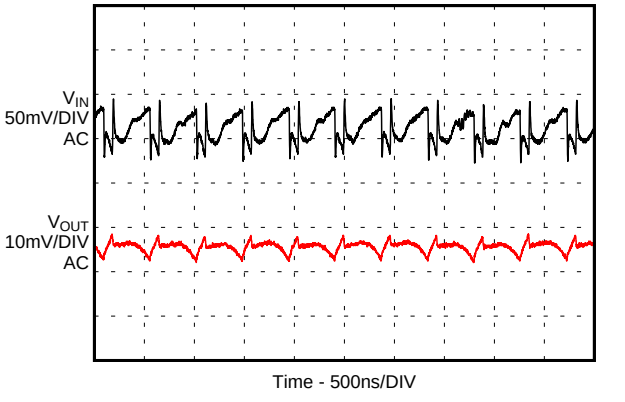
V_{OUT} = 1.8V V_{IN} = 12V

Figure 21. Switching Frequency



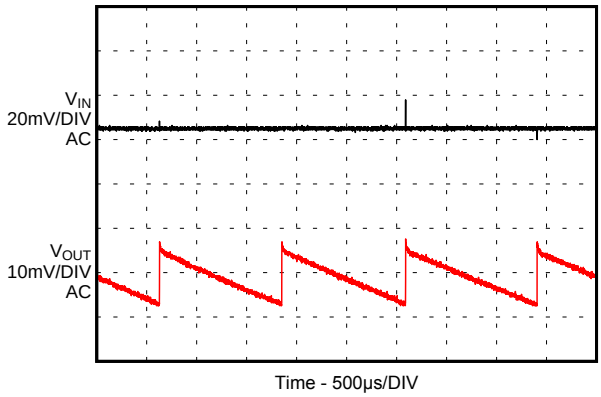
I_{OUT} = 1A

Figure 22. Switching Frequency



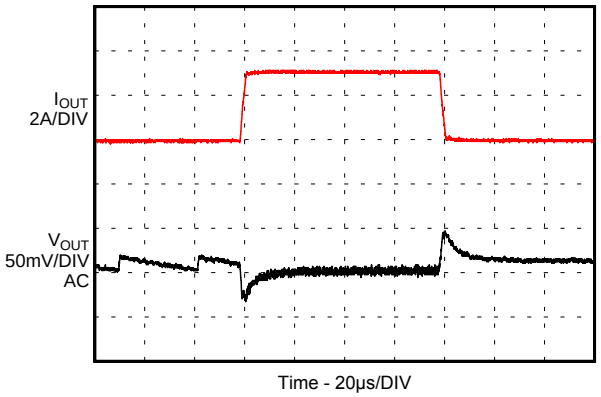
I_{OUT} = 3A

Figure 23. Input and Output Ripple in PWM Mode



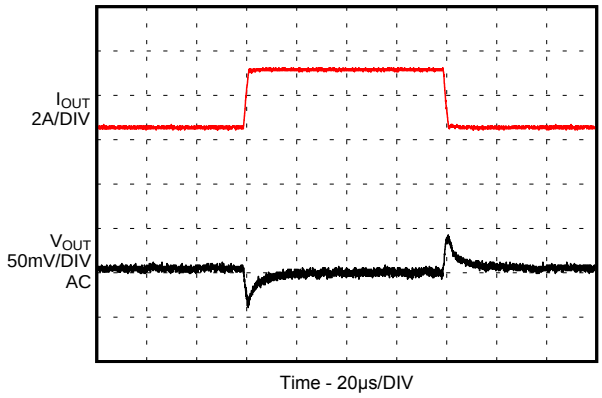
No Load

Figure 24. Input and Output Ripple in PSM Mode



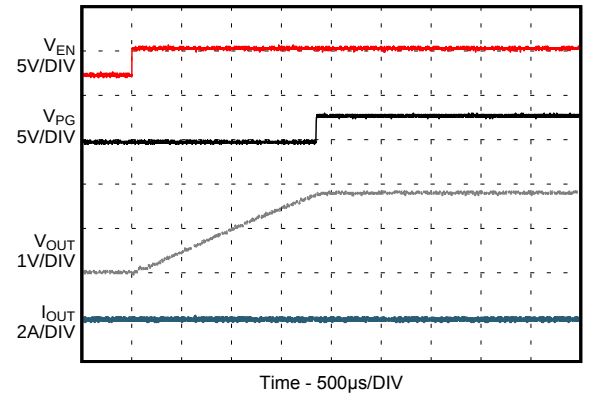
I_{OUT} = 0A to 3A, 1A/µs

Figure 25. Load Transient



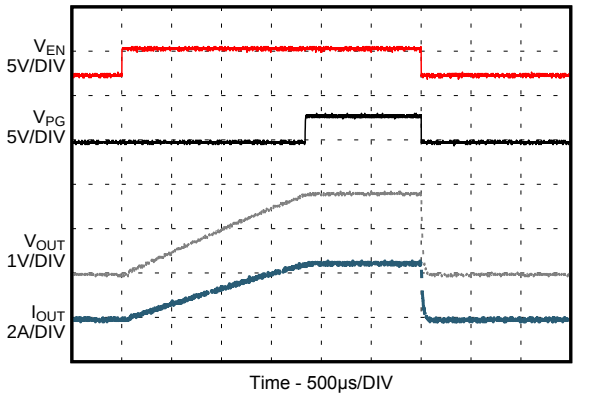
I_{OUT} = 0.5A to 3A, 1A/µs

Figure 26. Load Transient



No Load

Figure 27. Startup without Load



R_{OUT} = 0.68Ω

Figure 28. Startup / Shutdown with Resistance Load

9 Power Supply Recommendations

The devices are designed to operate from an input voltage supply range between 3V and 17V. The average input current of the TPS82130 is calculated as:

$$I_{IN} = \frac{1}{\eta} \times \frac{V_{OUT} \times I_{OUT}}{V_{IN}} \quad (8)$$

Ensure that the power supply has a sufficient current rating for the applications.

10 Layout

10.1 Layout Guidelines

- TI recommends placing all components as close as possible to the IC. The input capacitor placement specifically, must be closest to the VIN and GND pins of the device.
- Use wide and short traces for the main current paths to reduce the parasitic inductance and resistance.
- To enhance heat dissipation of the device, the exposed thermal pad should be connected to bottom or internal layer ground planes using vias.
- Refer to Figure 29 for an example of component placement, routing and thermal design.

10.2 Layout Example

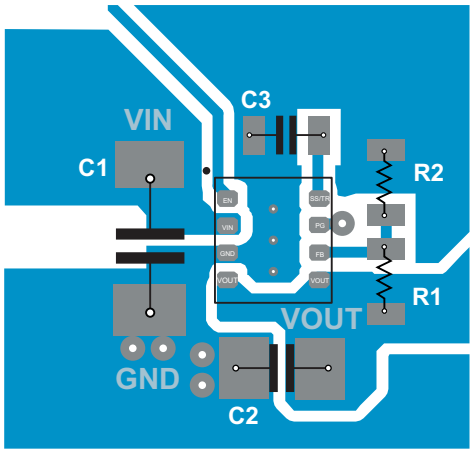


Figure 29. TPS82130 PCB Layout

10.3 Thermal Consideration

The output current of the TPS82130 needs to be derated when the device operates in a high ambient temperature or delivers high output power. The amount of current derating is dependent upon the input voltage, output power, PCB layout design and environmental thermal condition. Care should especially be taken in applications where the localized PCB temperature exceeds 65°C.

The TPS82130 module temperature must be kept less than the maximum rating of 125°C. Three basic approaches for enhancing thermal performance are below:

- Improve the power dissipation capability of the PCB design.
- Improve the thermal coupling of the TPS82130 to the PCB.
- Introduce airflow into the system.

To estimate approximate module temperature of TPS82130, apply the typical efficiency stated in this datasheet to the desired application condition to find the module's power dissipation. Then calculate the module temperature rise by multiplying the power dissipation by its thermal resistance. For more details on how to use the thermal parameters in real applications, see the application notes: SZZA017 and SPRA953.

11 Device and Documentation Support

11.1 Development Support

11.1.1 Custom Design with WEBENCH® Tools

Click here to create a custom design using the TPS82130 device with the WEBENCH® Power Designer.

1. Start by entering your V_{IN}, V_{OUT}, and I_{OUT} requirements.
2. Optimize your design for key parameters like efficiency, footprint and cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. The WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you will also be able to:
   - Run electrical simulations to see important waveforms and circuit performance
   - Run thermal simulations to understand the thermal performance of your board
   - Export your customized schematic and layout into popular CAD formats
   - Print PDF reports for the design, and share your design with colleagues
5. Get more information about WEBENCH tools at www.ti.com/WEBENCH.

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

MicroSiP, DCS-Control, E2E are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

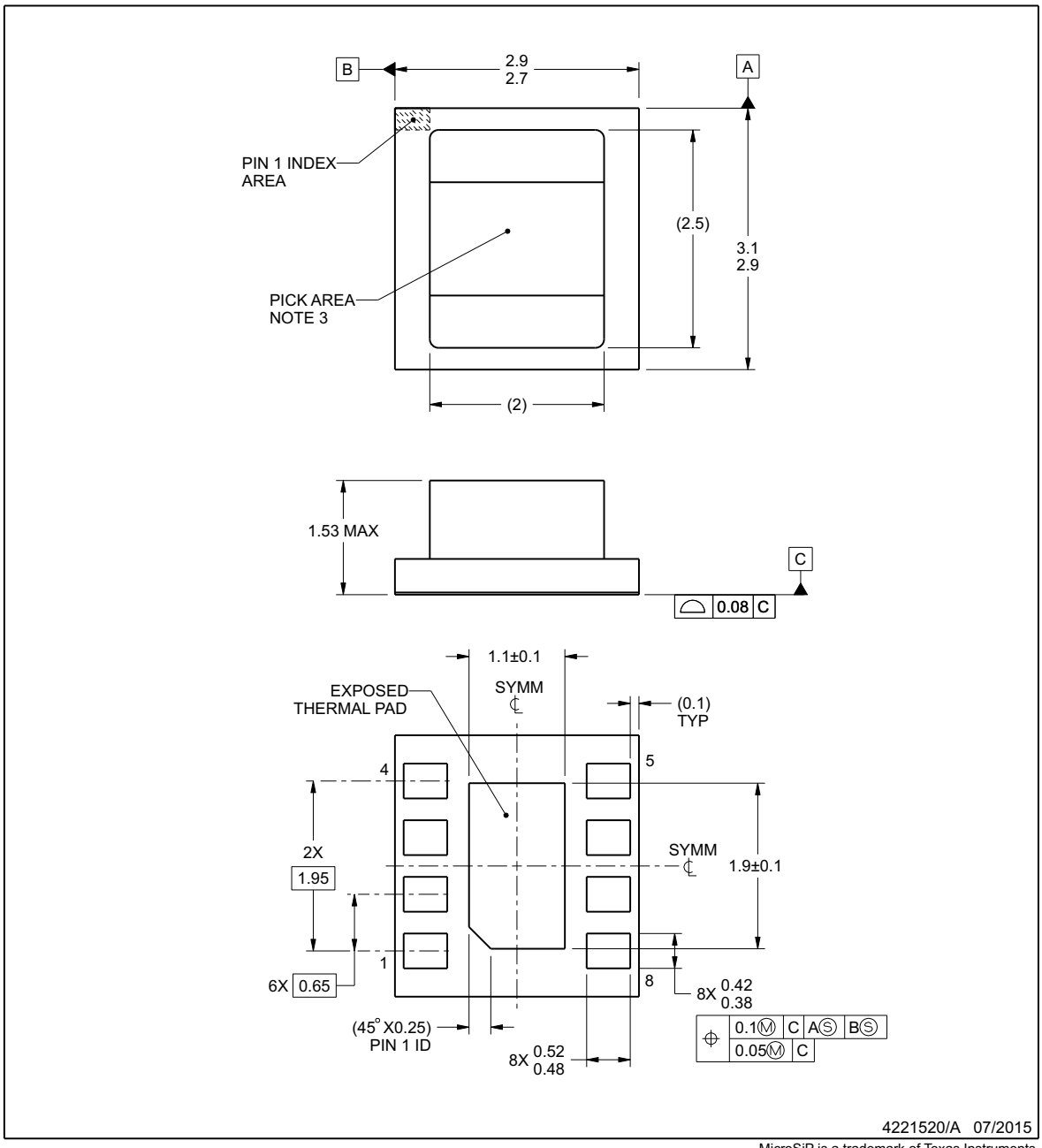
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

SIL0008D

MicroSiP™ - 1.53 mm max height

MICRO SYSTEM IN PACKAGE



MicroSiP is a trademark of Texas Instruments

NOTES:

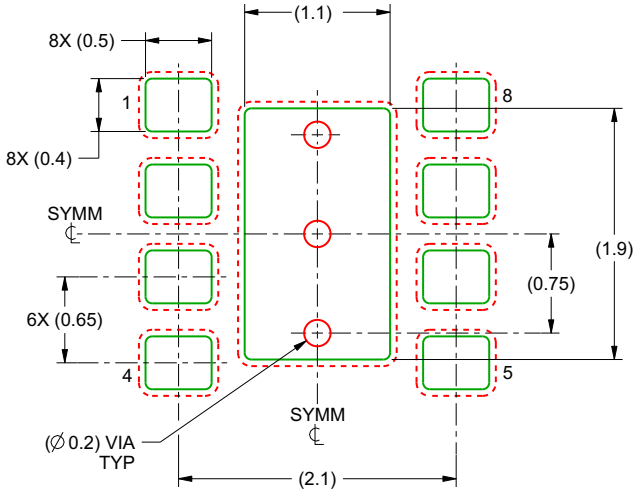
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Pick and place nozzle ∅ 1.3 mm or smaller recommended.
4. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

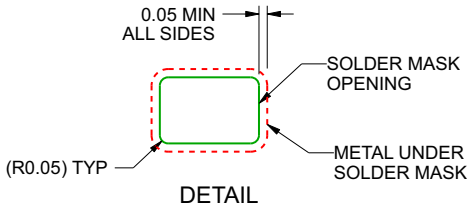
SIL0008D

MicroSiP ™ - 1.53 mm max height

MICRO SYSTEM IN PACKAGE



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:20X



DETAIL
NOT TO SCALE

4221520/A 07/2015

NOTES: (continued)

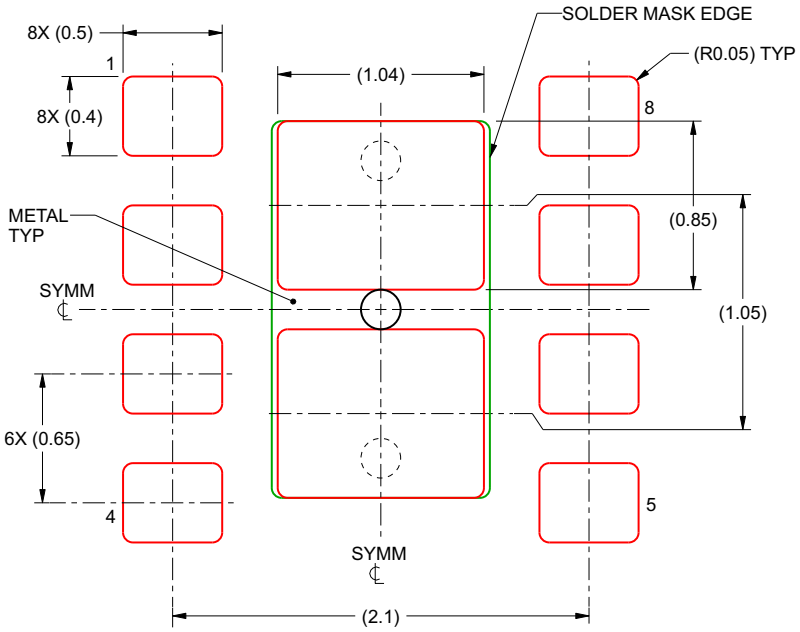
5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

SIL0008D

MicroSiP ™ - 1.53 mm max height

MICRO SYSTEM IN PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
85% PRINTED SOLDER COVERAGE BY AREA
SCALE:30X

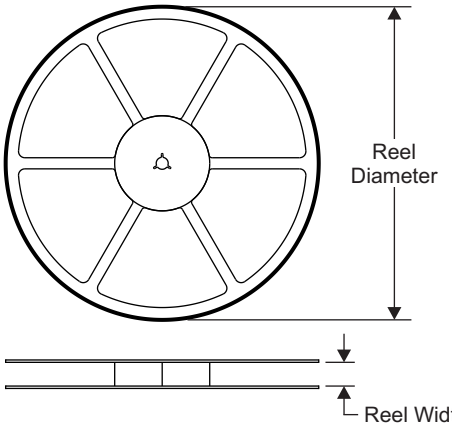
4221520/A 07/2015

NOTES: (continued)

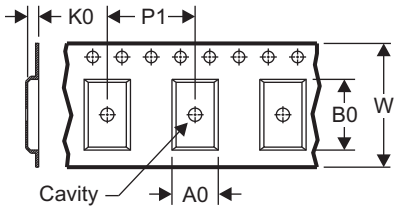
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

12.1 Tape and Reel Information

REEL DIMENSIONS

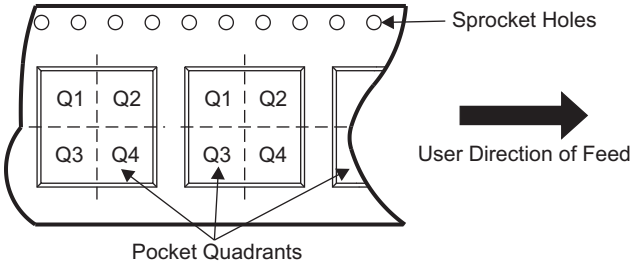


TAPE DIMENSIONS



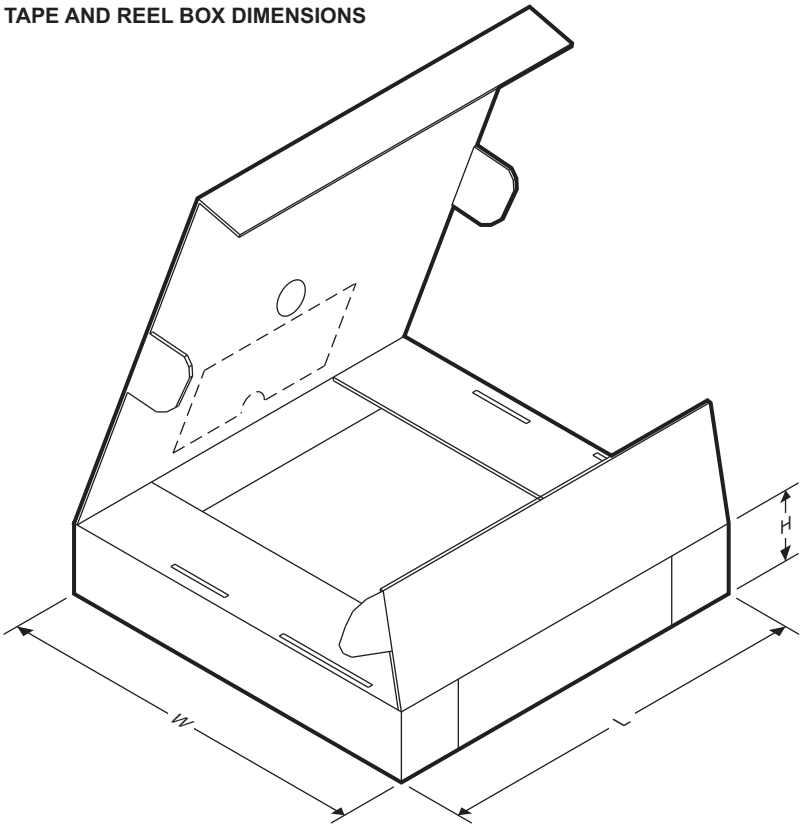
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS82130SILR	uSiP	SIL	8	3000	330.0	12.4	3.05	3.25	1.68	8.0	12.0	Q1
TPS82130SILT	uSiP	SIL	8	250	178.0	13.2	3.05	3.25	1.68	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS82130SILR	uSiP	SIL	8	3000	383.0	353.0	58.0
TPS82130SILT	uSiP	SIL	8	250	223.0	194.0	35.0

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS82130SILR	ACTIVE	uSiP	SIL	8	3000	RoHS & Green	NIAU	Level-2-260C-1 YEAR	-40 to 125	H6	Samples
TPS82130SILT	ACTIVE	uSiP	SIL	8	250	RoHS & Green	NIAU	Level-2-260C-1 YEAR	-40 to 125	H6	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265