

## SN74LVC1G175 Single D-Type Flip-Flop With Asynchronous Clear

### 1 Features

- Available in the Texas Instruments NanoFree™ Package
- Supports 5-V  $V_{CC}$  Operation
- Inputs Accept Voltages to 5.5 V
- Supports Down Translation to  $V_{CC}$
- Max  $t_{pd}$  of 4.3 ns at 3.3 V
- Low Power Consumption, 10- $\mu$ A Max  $I_{CC}$
- $\pm 24$ -mA Output Drive at 3.3 V
- $I_{off}$  Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

### 2 Applications

- TV/Set Top Box/Audio
- EPOS (Electronic Point-of-Sale)
- Motor Drives
- PC/Notebook
- Servers
- Factory Automation and Control
- Tablets
- Medical Healthcare and Fitness
- Smart Grid
- Telecom Infrastructure
- Enterprise Switching
- Projectors
- Storage

### 3 Description

This single D-type flip-flop is designed for 1.65-V to 5.5-V  $V_{CC}$  operation.

The SN74LVC1G175 device has an asynchronous clear ( $\overline{CLR}$ ) input. When  $\overline{CLR}$  is high, data from the input pin (D) is transferred to the output pin (Q) on the clock's (CLK) rising edge. When  $\overline{CLR}$  is low, Q is forced into the low state, regardless of the clock edge or data on D.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

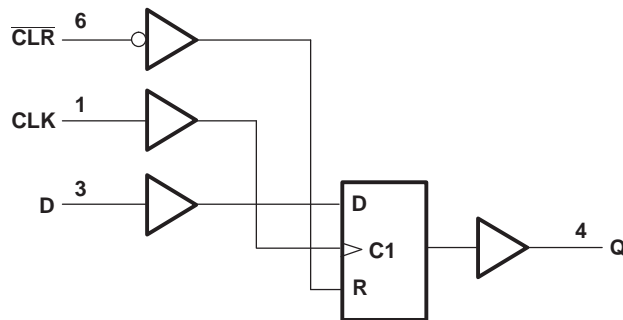
This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

#### Device Information<sup>(1)</sup>

| PART NUMBER     | PACKAGE    | BODY SIZE (NOM)   |
|-----------------|------------|-------------------|
| SN74LVC1G175DBV | SOT-23 (6) | 2.90 mm x 1.60 mm |
| SN74LVC1G175DCK | SC70 (6)   | 2.00 mm x 1.25 mm |
| SN74LVC1G175DRY | SON (6)    | 1.45 mm x 1.00 mm |
| SN74LVC1G175YZP | DSBGA (6)  | 1.41 mm x 0.91 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Logic Diagram (Positive Logic)



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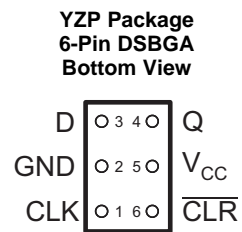
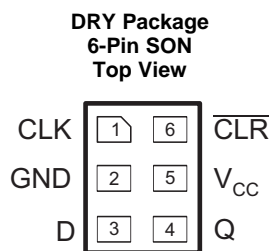
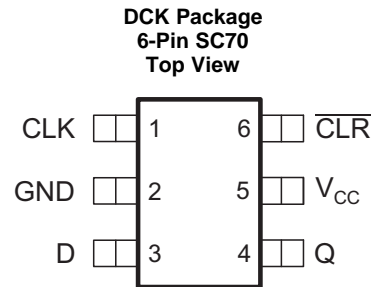
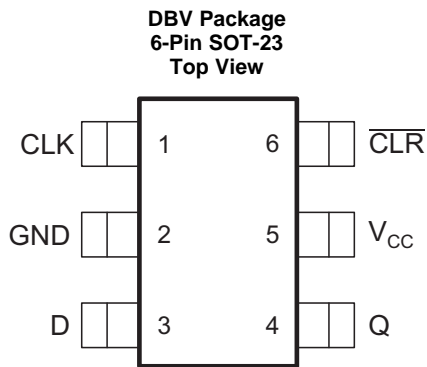
## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| <b>Changes from Revision F (December 2013) to Revision G</b> | <b>Page</b> |
|--|-------------|
| • Added <i>Applications</i> .....                            | 1           |
| • Added <i>Device Information</i> table .....                | 1           |
| • Added <i>ESD Ratingss</i> table .....                      | 4           |
| • Added <i>Thermal Information</i> table .....               | 5           |
| • Added <i>Typical Characteristics</i> .....                 | 7           |

| <b>Changes from Revision E (June 2008) to Revision F</b> | <b>Page</b> |
|--|-------------|
| • Updated document to new TI data sheet format .....     | 1           |
| • Deleted <i>Ordering Information</i> table .....        | 1           |
| • Updated Features .....                                 | 1           |

## 5 Pin Configuration and Functions



See mechanical drawings for dimensions.

### Pin Functions

| PIN                     |     | I/O | DESCRIPTION      |
|-------------------------|-----|-----|------------------|
| NAME                    | NO. |     |                  |
| CLK                     | 1   | I   | Clock Input      |
| $\overline{\text{CLR}}$ | 6   | I   | Clear Data Input |
| D                       | 3   | I   | Data Input       |
| GND                     | 2   | —   | Ground           |
| Q                       | 4   | O   | Output           |
| $V_{\text{CC}}$         | 5   | —   | Power            |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                  |   | MIN                | MAX                   | UNIT |
|------------------|---|--------------------|-----------------------|------|
| V <sub>CC</sub>  | Supply voltage  | -0.5               | 6.5                   | V    |
| V <sub>I</sub>   | Input voltage   | -0.5               | 6.5                   | V    |
| V <sub>O</sub>   | Voltage applied to any output in the high-impedance or power-off state <sup>(2)</sup> | -0.5               | 6.5                   | V    |
| V <sub>O</sub>   | Voltage applied to any output in the high or low state <sup>(2)(3)</sup>              | -0.5               | V <sub>CC</sub> + 0.5 | V    |
| I <sub>IK</sub>  | Input clamp current   | V <sub>I</sub> < 0 | -50                   | mA   |
| I <sub>OK</sub>  | Output clamp current  | V <sub>O</sub> < 0 | -50                   | mA   |
| I <sub>O</sub>   | Continuous output current   |                    | ±50                   | mA   |
|                  | Continuous current through V <sub>CC</sub> or GND                                     |                    | ±100                  | mA   |
| T <sub>stg</sub> | Storage temperature   | -65                | 150                   | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V<sub>CC</sub> is provided in the *Recommended Operating Conditions* table.

### 6.2 ESD Ratings

|                    |                         | VALUE  | UNIT |
|--------------------|-------------------------|--|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | 2000 |
|                    |                         | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | 1000 |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

 over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                 |                           | MIN                                | MAX                    | UNIT |
|-----------------|---------------------------|------------------------------------|------------------------|------|
| V <sub>CC</sub> | Supply voltage            | Operating                          | 1.65                   | 5.5  |
|                 |                           | Data retention only                | 1.5                    |      |
| V <sub>IH</sub> | High-level input voltage  | V <sub>CC</sub> = 1.65 V to 1.95 V | 0.65 × V <sub>CC</sub> | V    |
|                 |                           | V <sub>CC</sub> = 2.3 V to 2.7 V   | 1.7                    |      |
|                 |                           | V <sub>CC</sub> = 3 V to 3.6 V     | 2                      |      |
|                 |                           | V <sub>CC</sub> = 4.5 V to 5.5 V   | 0.7 × V <sub>CC</sub>  |      |
| V <sub>IL</sub> | Low-level input voltage   | V <sub>CC</sub> = 1.65 V to 1.95 V | 0.35 × V <sub>CC</sub> | V    |
|                 |                           | V <sub>CC</sub> = 2.3 V to 2.7 V   | 0.7                    |      |
|                 |                           | V <sub>CC</sub> = 3 V to 3.6 V     | 0.8                    |      |
|                 |                           | V <sub>CC</sub> = 4.5 V to 5.5 V   | 0.3 × V <sub>CC</sub>  |      |
| V <sub>I</sub>  | Input voltage             | 0                                  | 5.5                    | V    |
| V <sub>O</sub>  | Output voltage            | 0                                  | V <sub>CC</sub>        | V    |
| I <sub>OH</sub> | High-level output current | V <sub>CC</sub> = 1.65 V           | -4                     | mA   |
|                 |                           | V <sub>CC</sub> = 2.3 V            | -8                     |      |
|                 |                           | V <sub>CC</sub> = 3 V              | -16                    |      |
|                 |                           |                                    | -24                    |      |
|                 |                           | V <sub>CC</sub> = 4.5 V            | -32                    |      |

- (1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

## Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                     |                                    | MIN  | MAX | UNIT |
|---------------------|------------------------------------|--|-----|------|
| $I_{OL}$            | Low-level output current           | $V_{CC} = 1.65\text{ V}$   | 4   | mA   |
|                     |                                    | $V_{CC} = 2.3\text{ V}$  | 8   |      |
|                     |                                    | $V_{CC} = 3\text{ V}$  | 16  |      |
|                     |                                    |  | 24  |      |
|                     |                                    | $V_{CC} = 4.5\text{ V}$  | 32  |      |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}, 2.5\text{ V} \pm 0.2\text{ V}$ | 20  | ns/V |
|                     |                                    | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$                                 | 10  |      |
|                     |                                    | $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$                                   | 10  |      |
| $T_A$               | Operating free-air temperature     | -40  | 125 | °C   |

## 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> | SN74LVC1G175                           |            |           |             | UNIT |      |
|-------------------------------|--|------------|-----------|-------------|------|------|
|                               | DBV (SOT-23)                           | DCK (SC70) | DRY (SON) | YZP (DSBGA) |      |      |
|                               | 6 PINS                                 | 6 PINS     | 6 PINS    | 6 PINS      |      |      |
| $R_{\theta JA}$               | Junction-to-ambient thermal resistance | 165        | 259       | 234         | 123  | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER               | TEST CONDITIONS   | $V_{CC}$        | -40°C to 85°C  |                    |     | -40°C to 125°C |                    |     | UNIT          |
|-------------------------|---|-----------------|----------------|--------------------|-----|----------------|--------------------|-----|---------------|
|                         |   |                 | MIN            | TYP <sup>(1)</sup> | MAX | MIN            | TYP <sup>(1)</sup> | MAX |               |
| $V_{OH}$                | $I_{OH} = -100\ \mu\text{A}$  | 1.65 V to 5.5 V | $V_{CC} - 0.1$ |                    |     | $V_{CC} - 0.1$ |                    |     | V             |
|                         | $I_{OH} = -4\text{ mA}$   | 1.65 V          | 1.2            |                    |     | 1.2            |                    |     |               |
|                         | $I_{OH} = -8\text{ mA}$   | 2.3 V           | 1.9            |                    |     | 1.9            |                    |     |               |
|                         | $I_{OH} = -16\text{ mA}$  | 3 V             | 2.4            |                    |     | 2.4            |                    |     |               |
|                         |   |                 | 2.3            |                    |     | 2.3            |                    |     |               |
|                         | $I_{OH} = -32\text{ mA}$  | 4.5 V           | 3.8            |                    |     | 3.8            |                    |     |               |
| $V_{OL}$                | $I_{OL} = 100\ \mu\text{A}$   | 1.65 V to 5.5 V | 0.1            |                    |     | 0.1            |                    |     | V             |
|                         | $I_{OL} = 4\text{ mA}$  | 1.65 V          | 0.45           |                    |     | 0.45           |                    |     |               |
|                         | $I_{OL} = 8\text{ mA}$  | 2.3 V           | 0.3            |                    |     | 0.3            |                    |     |               |
|                         | $I_{OL} = 16\text{ mA}$   | 3 V             | 0.4            |                    |     | 0.4            |                    |     |               |
|                         |   |                 | 0.55           |                    |     | 0.55           |                    |     |               |
|                         | $I_{OL} = 24\text{ mA}$   | 4.5 V           | 0.55           |                    |     | 0.55           |                    |     |               |
| $I_{OL} = 32\text{ mA}$ | 0.55  |                 |                | 0.55               |     |                |                    |     |               |
| $I_I$                   | $V_I = 5.5\text{ V}$ or GND   | 0 to 5.5 V      | $\pm 1$        |                    |     | $\pm 1$        |                    |     | $\mu\text{A}$ |
| $I_{off}$               | $V_I$ or $V_O = 5.5\text{ V}$   | 0               | $\pm 10$       |                    |     | $\pm 10$       |                    |     | $\mu\text{A}$ |
| $I_{CC}$                | $V_I = 5.5\text{ V}$ or GND, $I_O = 0$                                    | 1.65 V to 5.5 V | 10             |                    |     | 10             |                    |     | $\mu\text{A}$ |
| $\Delta I_{CC}$         | One input at $V_{CC} - 0.6\text{ V}$ ,<br>Other inputs at $V_{CC}$ or GND | 3 V to 5.5 V    | 500            |                    |     | 500            |                    |     | $\mu\text{A}$ |
| $C_i$                   | $V_I = V_{CC}$ or GND   | 3.3 V           | 3              |                    |     | 3              |                    |     | pF            |

(1) All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

## 6.6 Timing Requirements, –40°C to 85°C

 over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 2](#))

|                    |                                      |                                  | –40°C to 85°C                             |     |  |     |  |     |  |     | UNIT |
|--------------------|--------------------------------------|----------------------------------|---|-----|--|-----|--|-----|--|-----|------|
|                    |                                      |                                  | $V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$ |     | $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ |     | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ |     | $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ |     |      |
|                    |                                      |                                  | MIN                                       | MAX | MIN                                      | MAX | MIN                                      | MAX | MIN                                    | MAX |      |
| $f_{\text{clock}}$ | Clock frequency                      |                                  | 100                                       |     | 125                                      |     | 150                                      |     | 175                                    |     | MHz  |
| $t_w$              | Pulse duration                       | $\overline{\text{CLR}}$          | Low                                       | 5.6 | 3  | 2.8 | 2.5                                      |     |  | ns  |      |
|                    |                                      | CLK                              | High or low                               | 3.5 | 3  | 2.8 | 2.5                                      |     |  |     |      |
| $t_{\text{su}}$    | Setup time, before CLK $\uparrow$    | Data                             |   | 3   | 2.5                                      | 2   | 1.5                                      |     |  | ns  |      |
|                    |                                      | $\overline{\text{CLR}}$ inactive |   | 0   | 0  | 0.5 | 0.5                                      |     |  |     |      |
| $t_h$              | Hold time, data after CLK $\uparrow$ |                                  | 0   | 0   | 0.5                                      | 0.5 |  |     | ns                                     |     |      |

## 6.7 Timing Requirements, –40°C to 125°C

 over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 2](#))

|                    |                                      |                                  | –40°C to 125°C                            |     |  |     |  |     |  |     | UNIT |
|--------------------|--------------------------------------|----------------------------------|---|-----|--|-----|--|-----|--|-----|------|
|                    |                                      |                                  | $V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$ |     | $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ |     | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ |     | $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ |     |      |
|                    |                                      |                                  | MIN                                       | MAX | MIN                                      | MAX | MIN                                      | MAX | MIN                                    | MAX |      |
| $f_{\text{clock}}$ | Clock frequency                      |                                  | 100                                       |     | 125                                      |     | 150                                      |     | 175                                    |     | MHz  |
| $t_w$              | Pulse duration                       | $\overline{\text{CLR}}$          | Low                                       | 5.6 | 3  | 2.8 | 2.5                                      |     |  | ns  |      |
|                    |                                      | CLK                              | High or low                               | 3.5 | 3  | 2.8 | 2.5                                      |     |  |     |      |
| $t_{\text{su}}$    | Setup time, before CLK $\uparrow$    | Data                             |   | 3   | 2.5                                      | 2   | 1.5                                      |     |  | ns  |      |
|                    |                                      | $\overline{\text{CLR}}$ inactive |   | 0.5 | 0.5                                      | 0.7 | 0.7                                      |     |  |     |      |
| $t_h$              | Hold time, data after CLK $\uparrow$ |                                  | 0.5                                       | 0.5 | 0.7                                      | 0.7 |  |     | ns                                     |     |      |

## 6.8 Switching Characteristics, –40°C to 85°C

 over recommended operating free-air temperature range,  $C_L = 15\text{ pF}$  (unless otherwise noted) (see [Figure 2](#))

| PARAMETER        | FROM (INPUT)            | TO (OUTPUT) | –40°C to 85°C                             |      |  |     |  |     |  |     | UNIT |
|------------------|-------------------------|-------------|---|------|--|-----|--|-----|--|-----|------|
|                  |                         |             | $V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$ |      | $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ |     | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ |     | $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ |     |      |
|                  |                         |             | MIN                                       | MAX  | MIN                                      | MAX | MIN                                      | MAX | MIN                                    | MAX |      |
| $f_{\text{max}}$ |                         |             | 100                                       |      | 125                                      |     | 150                                      |     | 175                                    |     | MHz  |
| $t_{\text{pd}}$  | CLK                     | Q           | 2.5                                       | 12.9 | 2  | 6.5 | 1.4                                      | 4.6 | 1                                      | 3   | ns   |
|                  | $\overline{\text{CLR}}$ |             | 2.5                                       | 12.4 | 2  | 6   | 1.2                                      | 4.3 | 1                                      | 3.2 |      |

## 6.9 Switching Characteristics, –40°C to 85°C

 over recommended operating free-air temperature range,  $C_L = 30\text{ pF}$  or  $50\text{ pF}$  (unless otherwise noted) (see [Figure 3](#))

| PARAMETER        | FROM (INPUT)            | TO (OUTPUT) | –40°C to 85°C                             |      |  |     |  |     |  |     | UNIT |
|------------------|-------------------------|-------------|---|------|--|-----|--|-----|--|-----|------|
|                  |                         |             | $V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$ |      | $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ |     | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ |     | $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ |     |      |
|                  |                         |             | MIN                                       | MAX  | MIN                                      | MAX | MIN                                      | MAX | MIN                                    | MAX |      |
| $f_{\text{max}}$ |                         |             | 100                                       |      | 125                                      |     | 150                                      |     | 175                                    |     | MHz  |
| $t_{\text{pd}}$  | CLK                     | Q           | 2.7                                       | 13.4 | 2.2                                      | 7.1 | 1.6                                      | 5.7 | 1.5                                    | 4   | ns   |
|                  | $\overline{\text{CLR}}$ |             | 2.7                                       | 12.9 | 2.2                                      | 7   | 1.5                                      | 5.8 | 1.3                                    | 4.1 |      |

### 6.10 Switching Characteristics, –40°C to 125°C

over recommended operating free-air temperature range,  $C_L = 30\text{ pF}$  or  $50\text{ pF}$  (unless otherwise noted) (see Figure 3)

| PARAMETER | FROM (INPUT)            | TO (OUTPUT) | –40°C to 125°C                            |      |  |     |  |     |  |     | UNIT |
|-----------|-------------------------|-------------|---|------|--|-----|--|-----|--|-----|------|
|           |                         |             | $V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$ |      | $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ |     | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ |     | $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ |     |      |
|           |                         |             | MIN                                       | MAX  | MIN                                      | MAX | MIN                                      | MAX | MIN                                    | MAX |      |
| $f_{max}$ |                         |             | 100                                       |      | 125                                      |     | 150                                      |     | 175                                    | MHz |      |
| $t_{pd}$  | CLK                     | Q           | 2.7                                       | 15.4 | 2.2                                      | 8.1 | 1.6                                      | 6.7 | 1.5                                    | 5   | ns   |
|           | $\overline{\text{CLR}}$ |             | 2.7                                       | 14.9 | 2.2                                      | 8   | 1.5                                      | 6.8 | 1.3                                    | 5.1 |      |

### 6.11 Operating Characteristics

$T_A = 25^\circ\text{C}$

| PARAMETER                              | TEST CONDITIONS     | $V_{CC} = 1.8\text{ V}$ | $V_{CC} = 2.5\text{ V}$ | $V_{CC} = 3.3\text{ V}$ | $V_{CC} = 5\text{ V}$ | UNIT |
|--|---------------------|-------------------------|-------------------------|-------------------------|-----------------------|------|
|  |                     | TYP                     | TYP                     | TYP                     | TYP                   |      |
| $C_{pd}$ Power dissipation capacitance | $f = 10\text{ MHz}$ | 18                      | 19                      | 19                      | 21                    | pF   |

### 6.12 Typical Characteristics

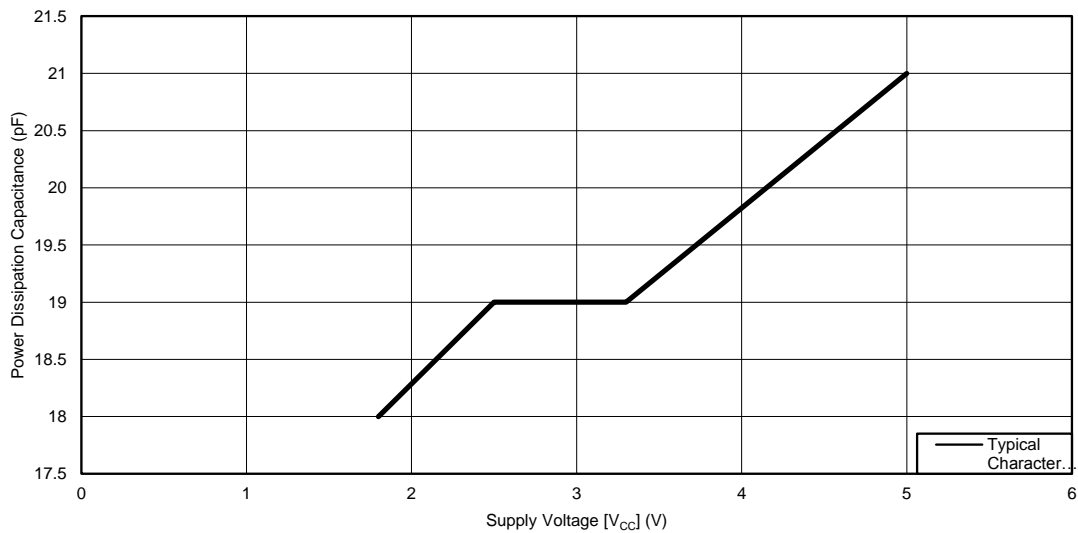
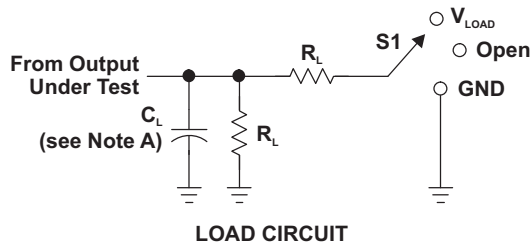


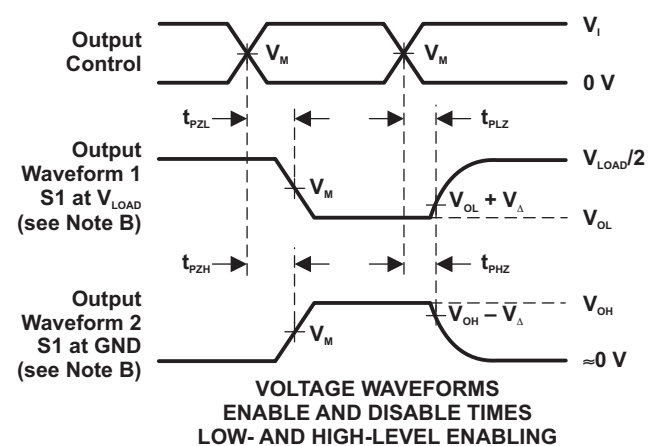
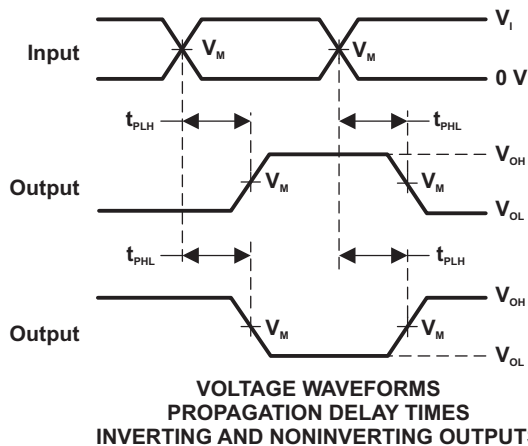
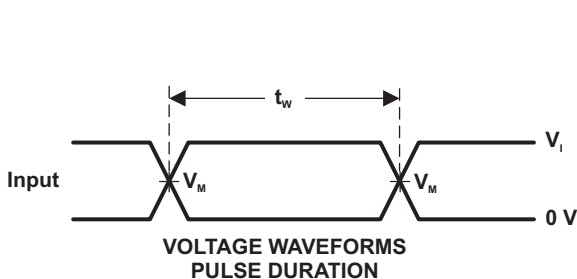
Figure 1. Voltage vs Capacitance

## 7 Parameter Measurement Information



| TEST              | S1         |
|-------------------|------------|
| $t_{PLH}/t_{PHL}$ | Open       |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}/t_{PZH}$ | GND        |

| $V_{CC}$                         | INPUTS   |                      | $V_M$      | $V_{LOAD}$        | $C_L$ | $R_L$        | $V_{\Delta}$ |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|--------------|
|                                  | $V_i$    | $t_i/t_r$            |            |                   |       |              |              |
| $1.8\text{ V} \pm 0.15\text{ V}$ | $V_{CC}$ | $\leq 2\text{ ns}$   | $V_{CC}/2$ | $2 \times V_{CC}$ | 15 pF | 1 M $\Omega$ | 0.15 V       |
| $2.5\text{ V} \pm 0.2\text{ V}$  | $V_{CC}$ | $\leq 2\text{ ns}$   | $V_{CC}/2$ | $2 \times V_{CC}$ | 15 pF | 1 M $\Omega$ | 0.15 V       |
| $3.3\text{ V} \pm 0.3\text{ V}$  | 3 V      | $\leq 2.5\text{ ns}$ | 1.5 V      | 6 V               | 15 pF | 1 M $\Omega$ | 0.3 V        |
| $5\text{ V} \pm 0.5\text{ V}$    | $V_{CC}$ | $\leq 2.5\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 15 pF | 1 M $\Omega$ | 0.3 V        |

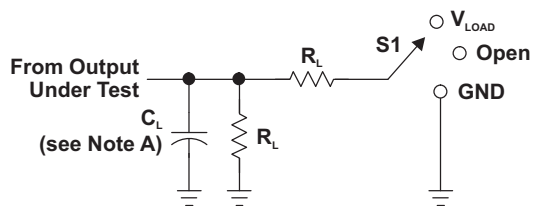


- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_o = 50\ \Omega$ .
  - The outputs are measured one at a time, with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - All parameters and waveforms are not applicable to all devices.

**Figure 2. Load Circuit and Voltage Waveforms**



Parameter Measurement Information (continued)



LOAD CIRCUIT

| TEST              | S1         |
|-------------------|------------|
| $t_{PLH}/t_{PHL}$ | Open       |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}/t_{PZH}$ | GND        |

| $V_{CC}$                         | INPUTS   |                      | $V_M$      | $V_{LOAD}$        | $C_L$ | $R_L$        | $V_{\Delta}$ |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|--------------|
|                                  | $V_I$    | $t_f/t_r$            |            |                   |       |              |              |
| $1.8\text{ V} \pm 0.15\text{ V}$ | $V_{CC}$ | $\leq 2\text{ ns}$   | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 k $\Omega$ | 0.15 V       |
| $2.5\text{ V} \pm 0.2\text{ V}$  | $V_{CC}$ | $\leq 2\text{ ns}$   | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 $\Omega$ | 0.15 V       |
| $3.3\text{ V} \pm 0.3\text{ V}$  | 3 V      | $\leq 2.5\text{ ns}$ | 1.5 V      | 6 V               | 50 pF | 500 $\Omega$ | 0.3 V        |
| $5\text{ V} \pm 0.5\text{ V}$    | $V_{CC}$ | $\leq 2.5\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 50 pF | 500 $\Omega$ | 0.3 V        |



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_o = 50\ \Omega$ .  
 D. The outputs are measured one at a time, with one transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{on}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .  
 H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

## 8 Detailed Description

### 8.1 Overview

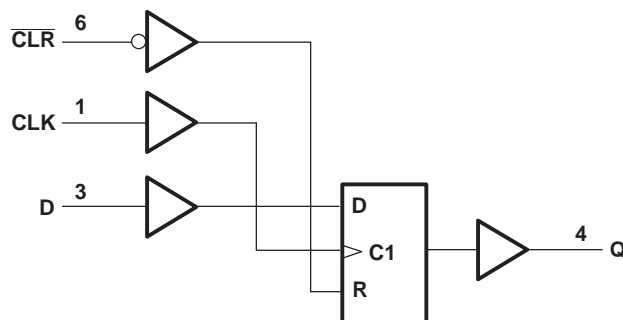
This single D-type flip-flop is designed for 1.65-V to 5.5-V  $V_{CC}$  operation.

The SN74LVC1G175 device has an asynchronous clear ( $\overline{CLR}$ ) input. When  $\overline{CLR}$  is high, data from the input pin (D) is transferred to the output pin (Q) on the clock's (CLK) rising edge. When  $\overline{CLR}$  is low, Q is forced into the low state, regardless of the clock edge or data on D.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

The SN74LVC1G175 device has a wide operating  $V_{CC}$  range of 1.65 V to 5.5 V, which allows it to be used in a broad range of systems. The 5.5-V I/Os allow down translation and also allow voltages at the inputs when  $V_{CC} = 0$ .

### 8.4 Device Functional Modes

Table 1 lists the functional modes for SN74LVC1G175.

**Table 1. Function Table**

| INPUTS           |        |   | OUTPUT<br>Q |
|------------------|--------|---|-------------|
| $\overline{CLR}$ | CLK    | D |             |
| H                | ↑      | L | L           |
| H                | ↑      | H | H           |
| H                | H or L | X | $Q_0$       |
| L                | X      | X | L           |

## 9 Application and Implementation

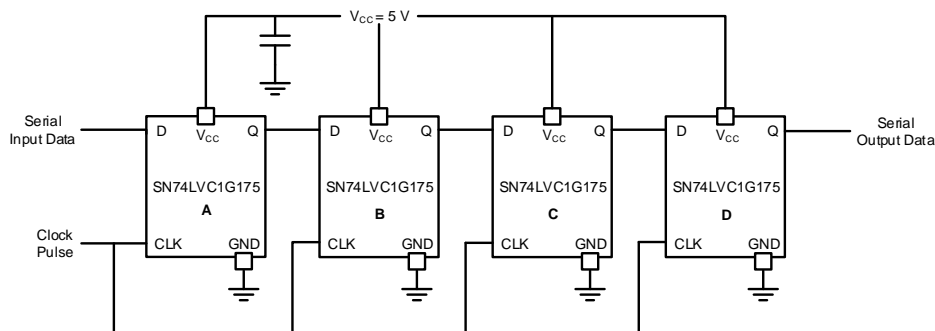
### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

Multiple SN74LVC1G175 devices can be used in tandem to create a shift register of arbitrary length. In this example, we use four SN74LVC1G175 devices to form a 4-bit serial shift register. By connecting all CLK inputs to a common clock pulse and tying each output of one device to the next, we can store and load 4-bit values on demand. We demonstrate loading the 4 bit value *1101* into memory by setting *Serial Input Data* to each desired memory bit, and by sending a clock pulse for each bit, we sequentially move all stored bits from left to right ( $A \rightarrow B \rightarrow C \rightarrow D$ )

### 9.2 Typical Application



**Figure 4. 4-Bit Serial Shift Register**

**Table 2. Stored Data Values**

| Serial Input Data | Stored A | Stored B | Stored C | Stored D |
|-------------------|----------|----------|----------|----------|
| 1                 | 0        | 0        | 0        | 0        |
| 0                 | 1        | 0        | 0        | 0        |
| 1                 | 0        | 1        | 0        | 0        |
| 1                 | 1        | 0        | 1        | 0        |
| 0                 | 1        | 1        | 0        | 1        |

#### 9.2.1 Design Requirements

The SN74LVC1G175 device uses CMOS technology and has balanced output drive. Care must be taken to avoid bus contention because it can drive currents that would exceed maximum limits.

The SN74LVC1G175 allows storing digital signals with a digital control signal. All input signals should remain as close as possible to either 0 V or  $V_{CC}$  for optimal operation.

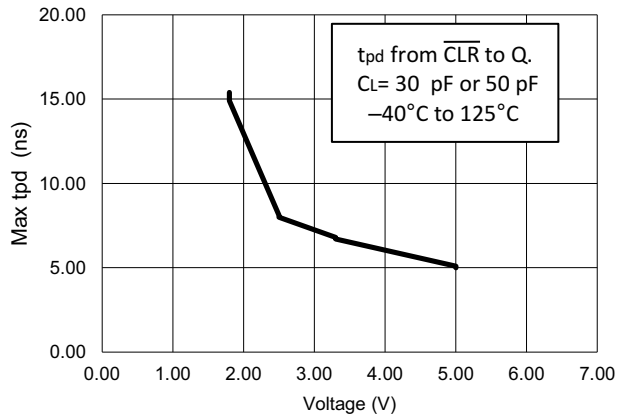
#### 9.2.2 Detailed Design Procedure

- Recommended input conditions:
  - For rise time and fall time specifications, see  $\Delta t/\Delta v$  in the table.
  - For specified high and low levels, see  $V_{IH}$  and  $V_{IL}$  in the table.
  - Inputs and outputs are overvoltage tolerant and can therefore go as high as 5.5 V at any valid  $V_{CC}$ .
- Recommended output conditions:
  - Load currents should not exceed  $\pm 50$  mA.

### 3. Frequency selection criterion:

- The effects of frequency upon the output current should be studied in Figure 5.
- Added trace resistance and capacitance can reduce maximum frequency capability; follow the layout practices listed in the [Layout](#) section.

### 9.2.3 Application Curve



**Figure 5. Max tpd vs Voltage of LVC Family**

## 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the table.

Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- $\mu$ F bypass capacitor is recommended. If multiple pins are labeled  $V_{CC}$ , then a 0.01- $\mu$ F or 0.022- $\mu$ F capacitor is recommended for each  $V_{CC}$  because the  $V_{CC}$  pins are tied together internally. For devices with dual supply pins operating at different voltages, for example  $V_{CC}$  and  $V_{DD}$ , a 0.1- $\mu$ F bypass capacitor is recommended for each supply pin. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1  $\mu$ F and 1  $\mu$ F are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 11 Layout

### 11.1 Layout Guidelines

When using multiple-bit logic devices, inputs must never float.

In many cases, functions (or parts of functions) of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or when only 3 of the 4 buffer gates are used. Such input pins must not be left unconnected, because the undefined voltages at the outside connections result in undefined operational states. [Figure 6](#) specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they are tied to GND or  $V_{CC}$ , whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it disables the output section of the part when asserted, which does not disable the input section of the I/Os. Therefore, the I/Os cannot float when disabled.

## 11.2 Layout Example

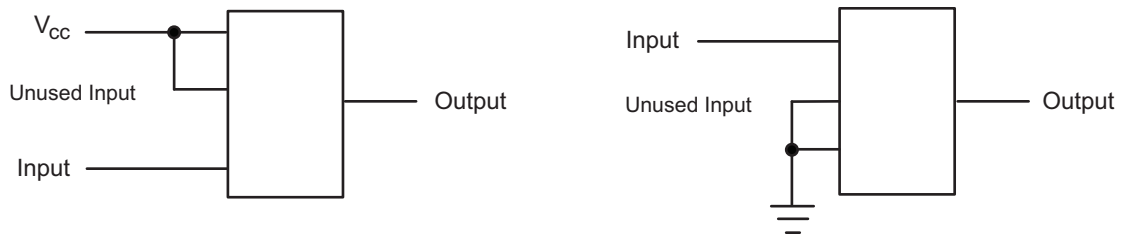


Figure 6. Layout Diagram

## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Related Documentation

For related documentation see the following:

- *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#)
- *Selecting the Right Texas Instruments Signal Switch*, [SZZA030](#)

### 12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](#), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.3 Trademarks

NanoFree, E2E are trademarks of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| 74LVC1G175DBVRE4 | ACTIVE        | SOT-23       | DBV             | 6    | 3000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | (C755, C75R)            | <a href="#">Samples</a> |
| 74LVC1G175DBVRG4 | ACTIVE        | SOT-23       | DBV             | 6    | 3000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | (C755, C75R)            | <a href="#">Samples</a> |
| 74LVC1G175DCKRG4 | ACTIVE        | SC70         | DCK             | 6    | 3000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | D65                     | <a href="#">Samples</a> |
| 74LVC1G175DCKTG4 | ACTIVE        | SC70         | DCK             | 6    | 250         | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | D65                     | <a href="#">Samples</a> |
| SN74LVC1G175DBVR | ACTIVE        | SOT-23       | DBV             | 6    | 3000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | (C755, C75R)            | <a href="#">Samples</a> |
| SN74LVC1G175DBVT | ACTIVE        | SOT-23       | DBV             | 6    | 250         | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | (C755, C75R)            | <a href="#">Samples</a> |
| SN74LVC1G175DCKR | ACTIVE        | SC70         | DCK             | 6    | 3000        | RoHS & Green    | NIPDAU   SN                          | Level-1-260C-UNLIM   | -40 to 125   | (D65, D6J, D6R)         | <a href="#">Samples</a> |
| SN74LVC1G175DCKT | ACTIVE        | SC70         | DCK             | 6    | 250         | RoHS & Green    | NIPDAU   SN                          | Level-1-260C-UNLIM   | -40 to 125   | (D65, D6J, D6R)         | <a href="#">Samples</a> |
| SN74LVC1G175DRYR | ACTIVE        | SON          | DRY             | 6    | 5000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | D6                      | <a href="#">Samples</a> |
| SN74LVC1G175YZPR | ACTIVE        | DSBGA        | YZP             | 6    | 3000        | RoHS & Green    | SNAGCU                               | Level-1-260C-UNLIM   | -40 to 85    | D6N                     | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN74LVC1G175 :**

- Enhanced Product : [SN74LVC1G175-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications



## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| 74LVC1G175DCKRG4 | SC70         | DCK             | 6    | 3000 | 178.0              | 9.2                | 2.4     | 2.4     | 1.22    | 4.0     | 8.0    | Q3            |
| 74LVC1G175DCKTG4 | SC70         | DCK             | 6    | 250  | 178.0              | 9.2                | 2.4     | 2.4     | 1.22    | 4.0     | 8.0    | Q3            |
| SN74LVC1G175DBVR | SOT-23       | DBV             | 6    | 3000 | 180.0              | 8.4                | 3.23    | 3.17    | 1.37    | 4.0     | 8.0    | Q3            |
| SN74LVC1G175DBVR | SOT-23       | DBV             | 6    | 3000 | 178.0              | 9.2                | 3.3     | 3.23    | 1.55    | 4.0     | 8.0    | Q3            |
| SN74LVC1G175DBVT | SOT-23       | DBV             | 6    | 250  | 180.0              | 8.4                | 3.23    | 3.17    | 1.37    | 4.0     | 8.0    | Q3            |
| SN74LVC1G175DBVT | SOT-23       | DBV             | 6    | 250  | 178.0              | 9.2                | 3.3     | 3.23    | 1.55    | 4.0     | 8.0    | Q3            |
| SN74LVC1G175DCKR | SC70         | DCK             | 6    | 3000 | 180.0              | 8.4                | 2.41    | 2.41    | 1.2     | 4.0     | 8.0    | Q3            |
| SN74LVC1G175DCKR | SC70         | DCK             | 6    | 3000 | 178.0              | 9.0                | 2.4     | 2.5     | 1.2     | 4.0     | 8.0    | Q3            |
| SN74LVC1G175DCKR | SC70         | DCK             | 6    | 3000 | 178.0              | 9.2                | 2.4     | 2.4     | 1.22    | 4.0     | 8.0    | Q3            |
| SN74LVC1G175DCKT | SC70         | DCK             | 6    | 250  | 180.0              | 8.4                | 2.41    | 2.41    | 1.2     | 4.0     | 8.0    | Q3            |
| SN74LVC1G175DCKT | SC70         | DCK             | 6    | 250  | 178.0              | 9.0                | 2.4     | 2.5     | 1.2     | 4.0     | 8.0    | Q3            |
| SN74LVC1G175DCKT | SC70         | DCK             | 6    | 250  | 178.0              | 9.2                | 2.4     | 2.4     | 1.22    | 4.0     | 8.0    | Q3            |
| SN74LVC1G175YZPR | DSBGA        | YZP             | 6    | 3000 | 178.0              | 9.2                | 1.02    | 1.52    | 0.63    | 4.0     | 8.0    | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| 74LVC1G175DCKRG4 | SC70         | DCK             | 6    | 3000 | 180.0       | 180.0      | 18.0        |
| 74LVC1G175DCKTG4 | SC70         | DCK             | 6    | 250  | 180.0       | 180.0      | 18.0        |
| SN74LVC1G175DBVR | SOT-23       | DBV             | 6    | 3000 | 202.0       | 201.0      | 28.0        |
| SN74LVC1G175DBVR | SOT-23       | DBV             | 6    | 3000 | 180.0       | 180.0      | 18.0        |
| SN74LVC1G175DBVT | SOT-23       | DBV             | 6    | 250  | 202.0       | 201.0      | 28.0        |
| SN74LVC1G175DBVT | SOT-23       | DBV             | 6    | 250  | 180.0       | 180.0      | 18.0        |
| SN74LVC1G175DCKR | SC70         | DCK             | 6    | 3000 | 202.0       | 201.0      | 28.0        |
| SN74LVC1G175DCKR | SC70         | DCK             | 6    | 3000 | 180.0       | 180.0      | 18.0        |
| SN74LVC1G175DCKR | SC70         | DCK             | 6    | 3000 | 180.0       | 180.0      | 18.0        |
| SN74LVC1G175DCKT | SC70         | DCK             | 6    | 250  | 202.0       | 201.0      | 28.0        |
| SN74LVC1G175DCKT | SC70         | DCK             | 6    | 250  | 180.0       | 180.0      | 18.0        |
| SN74LVC1G175DCKT | SC70         | DCK             | 6    | 250  | 180.0       | 180.0      | 18.0        |
| SN74LVC1G175YZPR | DSBGA        | YZP             | 6    | 3000 | 220.0       | 220.0      | 35.0        |

DCK (R-PDSO-G6)

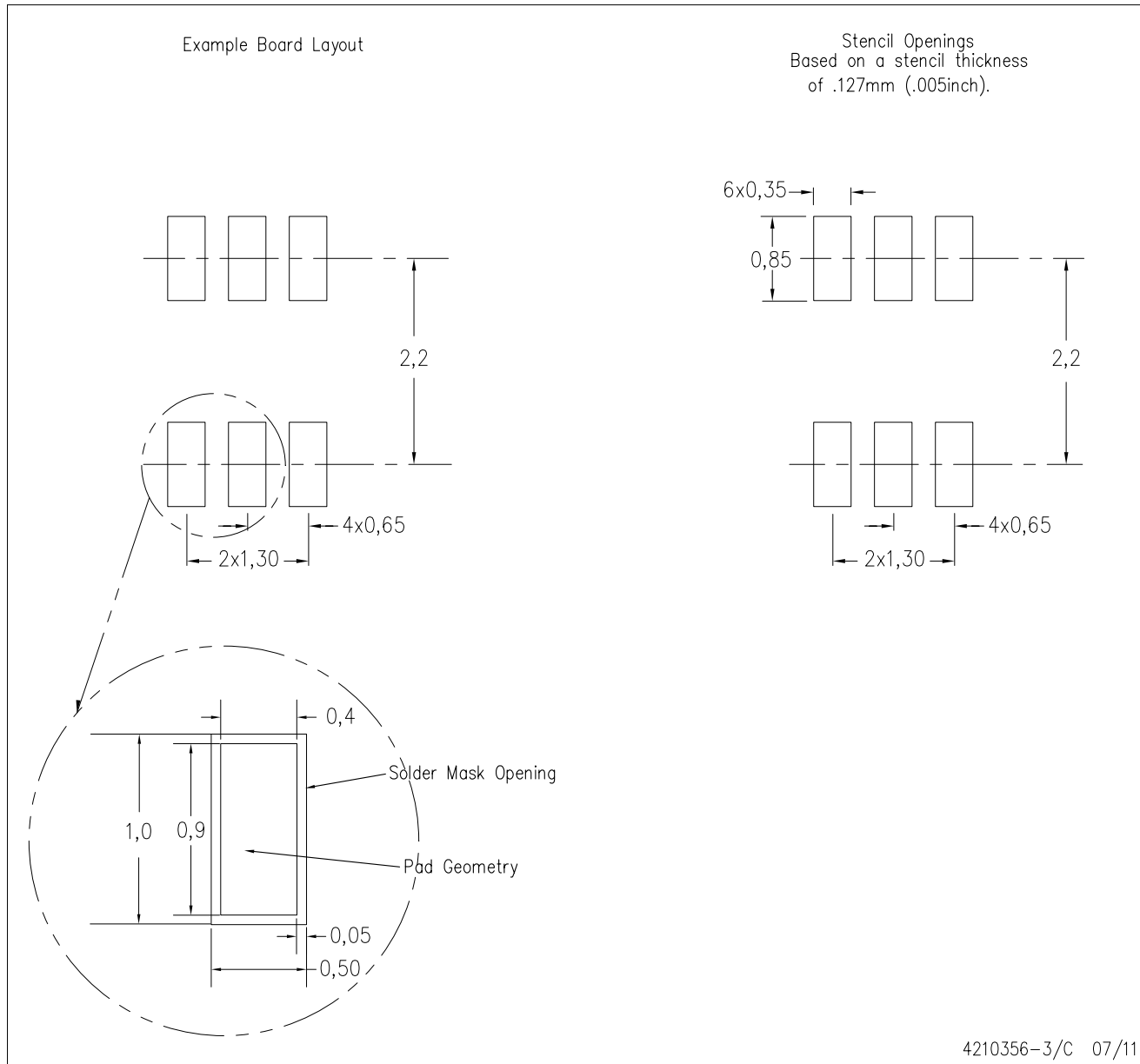
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-203 variation AB.

DCK (R-PDSO-G6)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



# EXAMPLE BOARD LAYOUT

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214840/C 06/2021

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



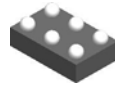
SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214840/C 06/2021

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

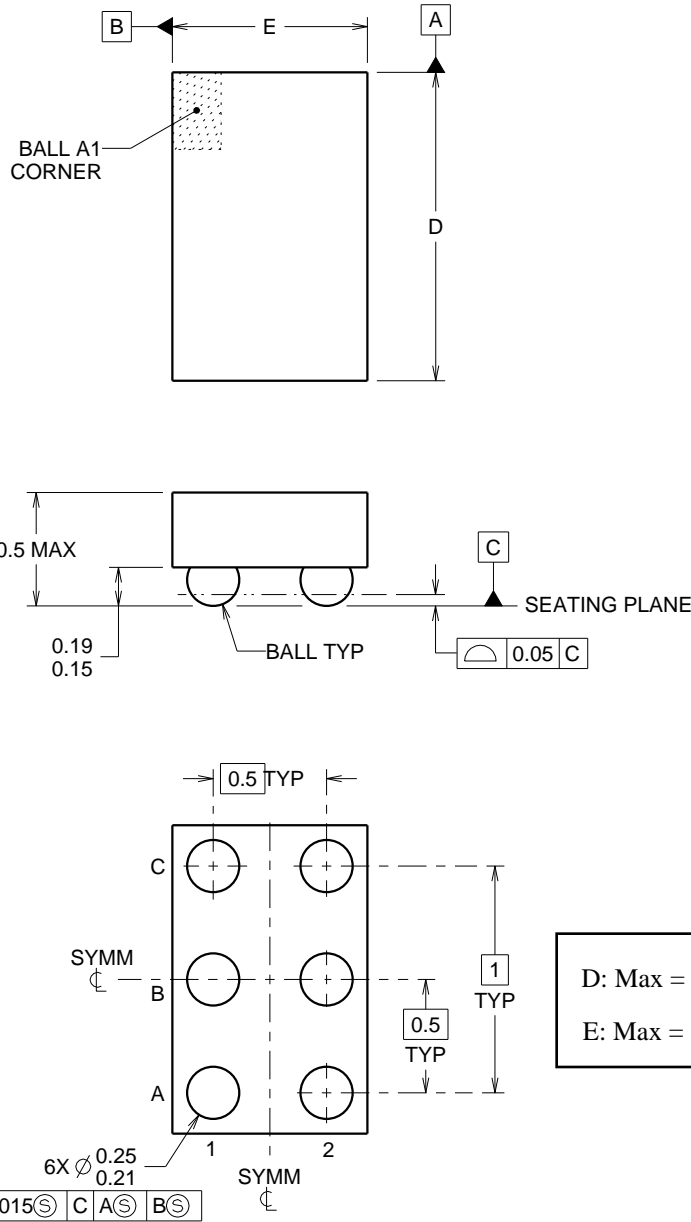
YZP0006



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



4219524/A 06/2014

NOTES:

NanoFree Is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.



# EXAMPLE BOARD LAYOUT

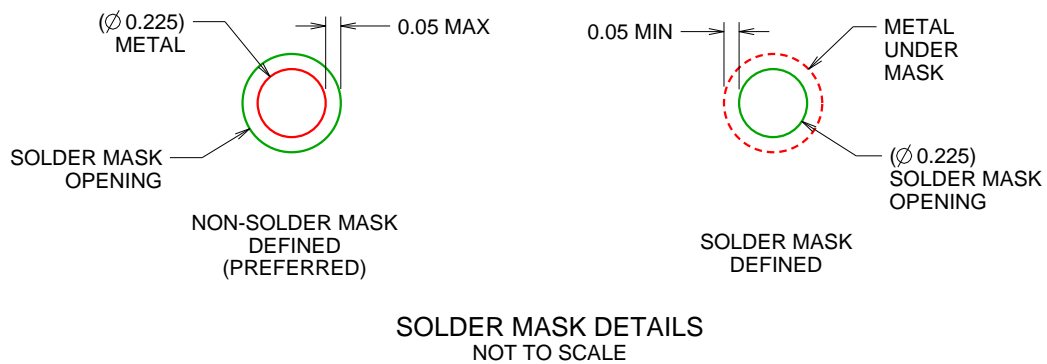
YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE  
SCALE:40X



4219524/A 06/2014

NOTES: (continued)

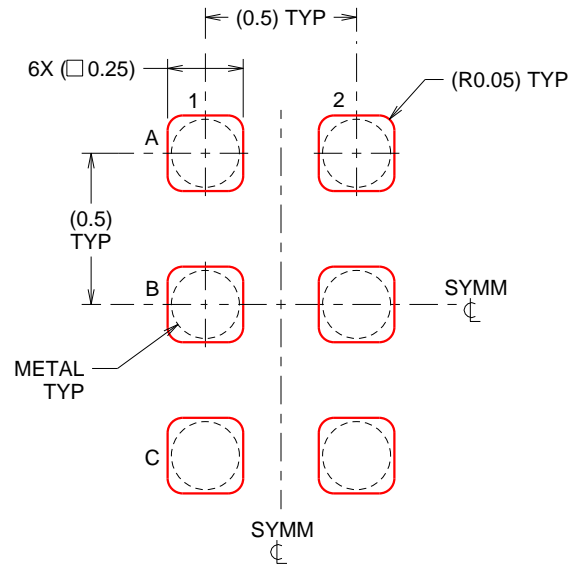
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SBVA017 ([www.ti.com/lit/sbva017](http://www.ti.com/lit/sbva017)).

# EXAMPLE STENCIL DESIGN

YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:40X

4219524/A 06/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

## GENERIC PACKAGE VIEW

**DRY 6**

**USON - 0.6 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4207181/G

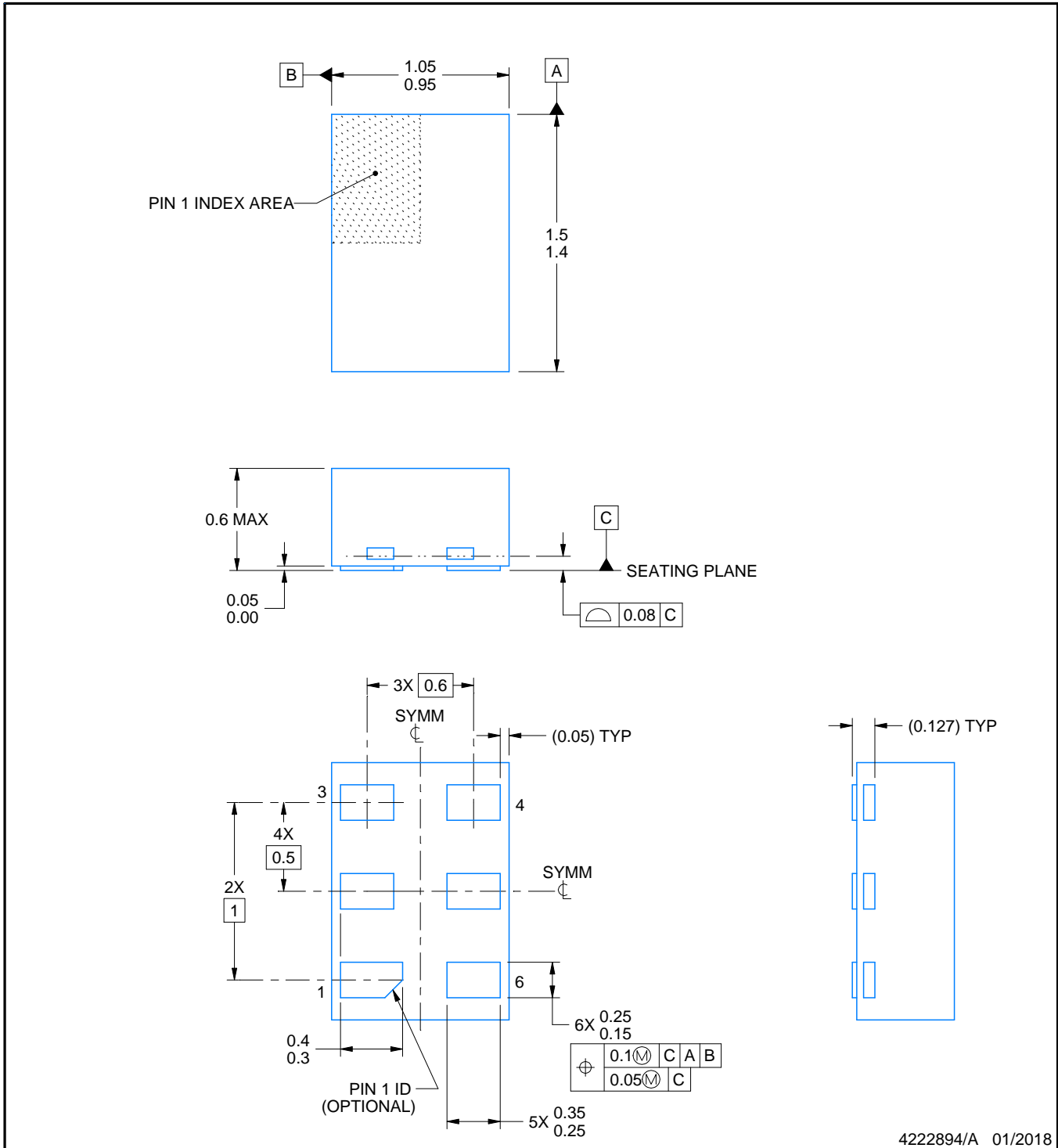
DRY0006A



# PACKAGE OUTLINE

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4222894/A 01/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



**LAND PATTERN EXAMPLE**  
1:1 RATIO WITH PKG SOLDER PADS  
EXPOSED METAL SHOWN  
SCALE:40X



**SOLDER MASK DETAILS**

4222894/A 01/2018

NOTES: (continued)

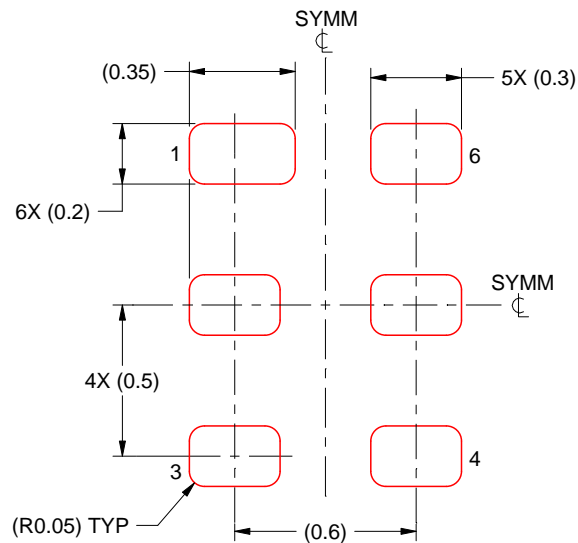
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

# EXAMPLE STENCIL DESIGN

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.075 - 0.1 mm THICK STENCIL  
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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