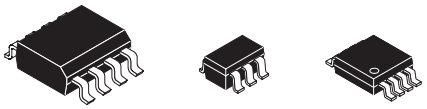


SLOS377A – SEPTEMBER 2001– REVISED JULY 2003

# FAMILY OF MICROPOWER RAIL-TO-RAIL INPUT AND OUTPUT OPERATIONAL AMPLIFIERS

## FEATURES

- **BiMOS Rail-to-Rail Input/Output**
- **Input Bias Current . . . 1 pA**
- **High Wide Bandwidth . . . 160 kHz**
- **High Slew Rate . . . 0.1 V/μs**
- **Supply Current . . . 7 μA (per channel)**
- **Input Noise Voltage . . . 90 nV/√Hz**
- **Supply Voltage Range . . . 2.7 V to 16 V**
- **Specified Temperature Range**
  - **–40°C to 125°C . . . Industrial Grade**
- **Ultra-Small Packaging**
  - **5 Pin SOT-23 (TLV2381)**

## APPLICATIONS

- **Portable Medical**
- **Power Monitoring**
- **Low Power Security Detection Systems**
- **Smoke Detectors**

## DESCRIPTION

The TLV238x single supply operational amplifiers provide rail-to-rail input and output capability. The TLV238x takes the minimum operating supply voltage down to 2.7 V over the extended industrial temperature range, while adding the rail-to-rail output swing feature. The TLV238x also provides 160-kHz bandwidth from only 7 μA. The maximum recommended supply voltage is 16 V, which allows the devices to be operated from (±8 V supplies down to ±1.35 V) two rechargeable cells.

The combination of rail-to-rail inputs and outputs make them good upgrades for the TLC27Lx family—offering more bandwidth at a lower quiescent current. The offset voltage is lower than the TLC27LxA variant.

To maintain cost effectiveness the TLV2381/2 are only available in the extended industrial temperature range. This means that one device can be used in a wide range of applications that include PDAs as well as automotive sensor interface.

All members are available in SOIC, with the singles in the small SOT-23 package, duals in the MSOP.

**SELECTION GUIDE**

| DEVICE | $V_S$ [V] | $I_Q$/ch [μA] | $V_{ICR}$ [V] | $V_{IO}$ [mV] | $I_{IB}$ [pA] | GBW [MHz] | SLEW RATE [V/μs] | $V_n$, 1 kHz [nV/√Hz] |
|---|---|---|---|---|---|---|---|---|
| TLV238x | 2.7 to 16 | 10 | –0.2 to $V_S$ + 0.2 | 4.5 | 60 | 0.16 | 0.06 | 100 |
| TLV27Lx | 2.7 to 16 | 11 | –0.2 to $V_S$ – 1.2 | 5 | 60 | 0.16 | 0.06 | 100 |
| TLC27Lx | 4 to 16 | 17 | –0.2 to $V_S$ – 1.5 | 10/5/2 | 60 | 0.085 | 0.03 | 68 |
| OPAx349 | 1.8 to 5.5 | 2 | –0.2 to $V_S$ + 0.2 | 10 | 10 | 0.070 | 0.02 | 300 |
| OPAx347 | 2.3 to 5.5 | 34 | –0.2 to $V_S$ + 0.2 | 6 | 10 | 0.35 | 0.01 | 60 |
| TLC225x | 2.7 to 16 | 62.5 | 0 to $V_S$ – 1.5 | 1.5/0.85 | 60 | 0.200 | 0.02 | 19 |

NOTE: All dc specs are maximums while ac specs are typicals.

**PACKAGE/ORDERING INFORMATION**

| PRODUCT | PACKAGE | PACKAGE CODE | SYMBOL | SPECIFIED TEMPERATURE RANGE | ORDER NUMBER | TRANSPORT MEDIA |
|---|---|---|---|---|---|---|
| TLV2381ID | SOIC-8 | D | 2381I | –40°C to 125°C | TLV2381ID | Tube |
| | | | | | TLV2381IDR | Tape and Reel |
| TLV2381IDBV | SOT-23 | DBV | VBKI | | TLV2381IDBVR | Tape and Reel |
| | | | | | TLV2381IDBVT | |
| TLV2382ID | SOIC-8 | D | 2382I | | TLV2382ID | Tube |
| | | | | | TLV2382IDR | Tape and Reel |

## absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, $V_S$ . . . . . 16.5 V
Input voltage, $V_I$ (see Notes 1 and 2) . . . . . $V_S$ + 0.2 V
Output current, $I_O$ . . . . . 100 mA
Differential input voltage, $V_{ID}$ . . . . . $V_S$
Continuous total power dissipation . . . . . See Dissipation Rating Table
Maximum junction temperature, $T_J$ . . . . . 150°C
Operating free-air temperature range, $T_A$: I suffix . . . . . –40°C to 125°C
Storage temperature range, $T_{stg}$ . . . . . –65°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Relative to GND pin.
2. Maximum is 16.5 V or $V_S$+0.2 V whichever is the lesser value.

**DISSIPATION RATING TABLE**

| PACKAGE | $\theta_{JC}$ (°C/W) | $\theta_{JA}$ (°C/W) | $T_A \le 25°C$ POWER RATING | $T_A = 85°C$ POWER RATING |
|---|---|---|---|---|
| D (8) | 38.3 | 176 | 710 mW | 370 mW |
| DBV (5) | 55 | 324.1 | 385 mW | 201 mW |
| DBV (6) | 55 | 294.3 | 425 mW | 221 mW |

## recommended operating conditions

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage, ($V_S$) | Dual supply | ±1.35 | ±8 | V |
| | Single supply | 2.7 | 16 | |
| Input common-mode voltage range | | –0.2 | $V_S$+0.2 | V |
| Operating free air temperature, $T_A$ | I-suffix | –40 | 125 | °C |

## electrical characteristics at recommended operating conditions, $V_S$ = 2.7 V, 5 V, and 15 V (unless otherwise noted)

### dc performance

| PARAMETER | | TEST CONDITIONS | | $T_A$† | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{IO}$ | Input offset voltage | $V_{IC}$ = $V_S$/2, $R_L$ = 100 kΩ | $V_O$ = $V_S$/2 $R_S$ = 50 Ω | 25°C | | 0.5 | 4.5 | mV |
| | | | | Full range | | | 6.5 | |
| $\alpha_{VIO}$ | Offset voltage drift | | | 25°C | | 1.1 | | µV/°C |
| CMRR | Common-mode rejection ratio | $V_{IC}$ = 0 V to $V_S$, $R_S$ = 50 Ω | $V_S$ = 2.7 V | 25°C | 54 | 69 | | dB |
| | | | | Full range | 53 | | | |
| | | $V_{IC}$ = 0 V to $V_S$–1.3 V, $R_S$ = 50 Ω | | 25°C | 71 | 86 | | |
| | | | | Full range | 70 | | | |
| | | $V_{IC}$ = 0 V to $V_S$, $R_S$ = 50 Ω | $V_S$ = 5 V | 25°C | 58 | 74 | | dB |
| | | | | Full range | 57 | | | |
| | | $V_{IC}$ = 0 V to $V_S$–1.3 V, $R_S$ = 50 Ω | | 25°C | 72 | 88 | | |
| | | | | Full range | 70 | | | |
| | | $V_{IC}$ = 0 V to $V_S$, $R_S$ = 50 Ω | $V_S$ = 15 V | 25°C | 65 | 80 | | dB |
| | | | | Full range | 64 | | | |
| | | $V_{IC}$ = 0 V to $V_S$–1.3 V, $R_S$ = 50 Ω | | 25°C | 72 | 90 | | |
| | | | | Full range | 70 | | | |
| $A_{VD}$ | Large-signal differential voltage amplification | $V_{O(PP)}$=$V_S$/2, $R_L$ = 100 kΩ | $V_S$ = 2.7 V | 25°C | 80 | 100 | | dB |
| | | | | Full range | 77 | | | |
| | | | $V_S$ = 5 V | 25°C | 80 | 100 | | |
| | | | | Full range | 77 | | | |
| | | | $V_S$ = 15 V | 25°C | 77 | 83 | | |
| | | | | Full range | 74 | | | |

† Full range is –40°C to 125°C.

### input characteristics

| PARAMETER | | TEST CONDITIONS | | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $I_{IO}$ | Input offset current | $V_{IC}$ = $V_S$/2, $R_L$ = 100 kΩ , | $V_O$ = $V_S$/2, $R_S$ = 50 Ω | ≤25°C | | 1 | 60 | pA |
| | | | | ≤70°C | | | 100 | |
| | | | | ≤125°C | | | 1000 | |
| $I_{IB}$ | Input bias current | | | ≤25°C | | 1 | 60 | pA |
| | | | | ≤70°C | | | 200 | |
| | | | | ≤125°C | | | 1000 | |
| $r_{i(d)}$ | Differential input resistance | | | 25°C | | 1000 | | GΩ |
| $C_{IC}$ | Common-mode input capacitance | f = 1 kHz | | 25°C | | 8 | | pF |

## electrical characteristics at recommended operating conditions, $V_S$ = 2.7 V, 5 V, and 15 V (unless otherwise noted) (continued)

### power supply

| PARAMETER | | TEST CONDITIONS | $T_A$† | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{DD}$ | Supply current (per channel) | $V_O = V_S/2$ | 25°C | | 7 | 10 | µA |
| | | | Full range | | | 15 | |
| PSRR | Power supply rejection ratio ($\Delta V_S/\Delta V_{IO}$) | $V_S$ = 2.7 V to 16V, No load, $V_{IC} = V_S/2$ V | 25°C | 74 | 82 | | dB |
| | | | Full range | 70 | | | |

† Full range is –40°C to 125°C for I suffix.

### output characteristics

| PARAMETER | | TEST CONDITIONS | | $T_A$† | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_O$ | Output voltage swing from rail | $V_{IC} = V_S/2$, $I_O$ = 100 µA | $V_S$ = 2.7 V | 25°C | 200 | 160 | | mV |
| | | | | Full range | 220 | | | |
| | | | $V_S$ = 5 V | 25°C | 120 | 85 | | |
| | | | | Full range | 200 | | | |
| | | | $V_S$ = 15 V | 25°C | 120 | 50 | | |
| | | | | Full range | 150 | | | |
| | | $V_{IC} = V_S/2$, $I_O$ = 500 µA | $V_S$ = 5 V | 25°C | 800 | 420 | | mV |
| | | | | Full range | 900 | | | |
| | | | $V_S$ = 15 V | 25°C | 400 | 200 | | |
| | | | | Full range | 500 | | | |
| $I_O$ | Output current | $V_O$ = 0.5 V from rail | $V_S$ = 2.7 V | 25°C | | 400 | | µA |

† Full range is –40°C to 125°C for I suffix.

### dynamic performance

| PARAMETER | | TEST CONDITIONS | | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| GBP | Gain bandwidth product | $R_L$ = 100 kΩ , $C_L$ = 10 pF, f = 1 kHz | | 25°C | | 160 | | kHz |
| SR | Slew rate at unity gain | $V_{O(pp)}$ = 2 V, $R_L$ = 100 kΩ, $C_L$ = 10 pF | | 25°C | | 0.06 | | V/µs |
| | | | | –40°C | | 0.05 | | |
| | | | | 125°C | | 0.08 | | |
| $\phi_M$ | Phase margin | $R_L$ = 100 kΩ, $C_L$ = 50 pF | | 25°C | | 62 | | ° |
| | Gain margin | | | 25°C | | 6.7 | | dB |
| $t_s$ | Settling time (0.1%) | $V_{(STEP)pp}$ = 1 V, $A_V$ = –1, $C_L$ = 10 pF, $R_L$ = 100 kΩ | Rise | 25°C | | 31 | | µs |
| | | | Fall | | | 61 | | |

### noise/distortion performance

| PARAMETER | | TEST CONDITIONS | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_n$ | Equivalent input noise voltage | f = 1 kHz | 25°C | | 90 | | nV/√Hz |

## TYPICAL CHARACTERISTICS

### Table of Graphs

| | | | FIGURE |
|---|---|---|---|
| $V_{IO}$ | Input offset voltage | vs Common-mode input voltage | 1, 2, 3 |
| $I_{IB}/I_{IO}$ | Input bias and offset current | vs Free-air temperature | 4 |
| $V_{OH}$ | High-level output voltage | vs High-level output current | 5, 7, 9 |
| $V_{OL}$ | Low-level output voltage | vs Low-level output current | 6, 8, 10 |
| $I_Q$ | Quiescent current | vs Supply voltage | 11 |
| | | vs Free-air temperature | 12 |
| | Supply voltage and supply current ramp up | | 13 |
| $A_{VD}$ | Differential voltage gain and phase shift | vs Frequency | 14 |
| GBP | Gain-bandwidth product | vs Free-air temperature | 15 |
| $\phi_m$ | Phase margin | vs Load capacitance | 16 |
| CMRR | Common-mode rejection ratio | vs Frequency | 17 |
| PSRR | Power supply rejection ratio | vs Frequency | 18 |
| | Input referred noise voltage | vs Frequency | 19 |
| SR | Slew rate | vs Free-air temperature | 20 |
| $V_{O(PP)}$ | Peak-to-peak output voltage | vs Frequency | 21 |
| | Inverting small-signal response | | 22 |
| | Inverting large-signal response | | 23 |
| | Crosstalk | vs Frequency | 24 |

**INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE**

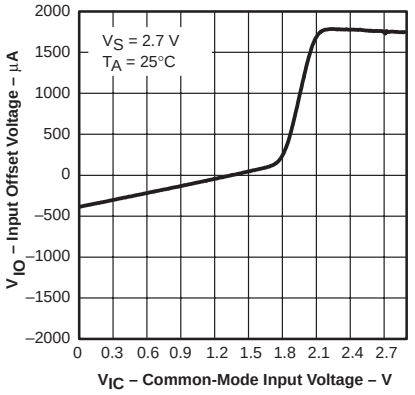



**Figure 1**

**INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE**

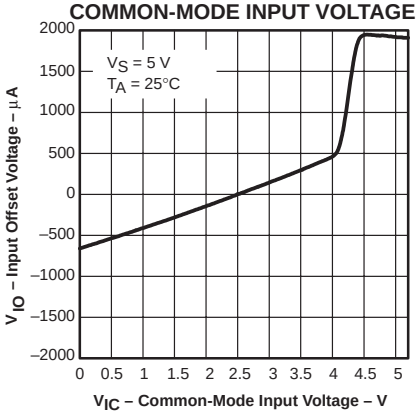



**Figure 2**

**INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE**

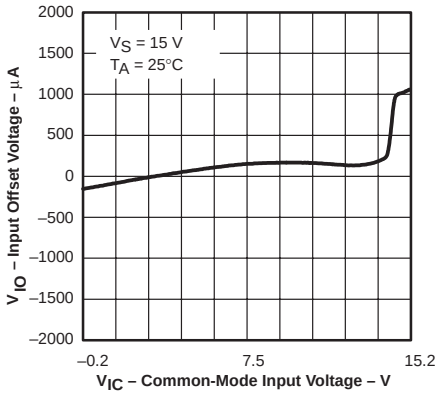



**Figure 3**

## TYPICAL CHARACTERISTICS

**INPUT BIAS AND INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE**

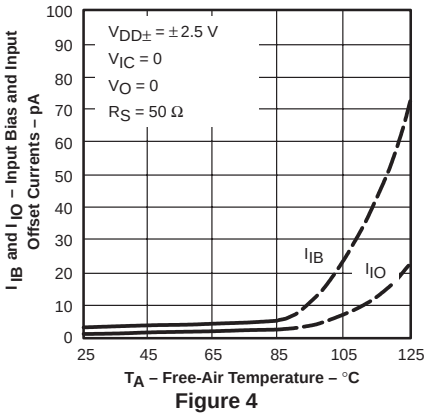



Figure 4

**HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT**

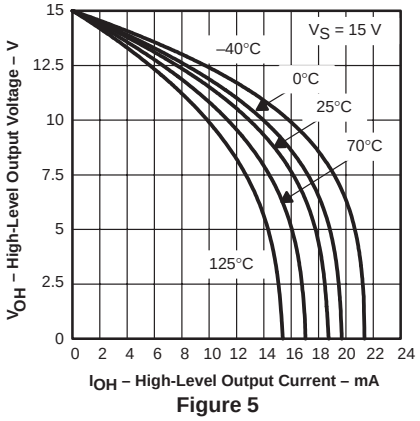



Figure 5

**LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT**

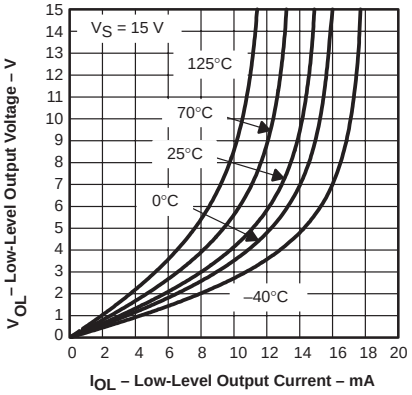



Figure 6

**HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT**

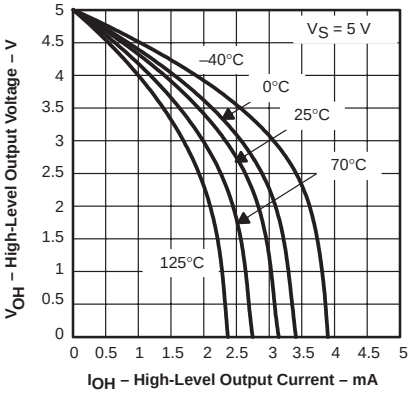



Figure 7

**LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT**

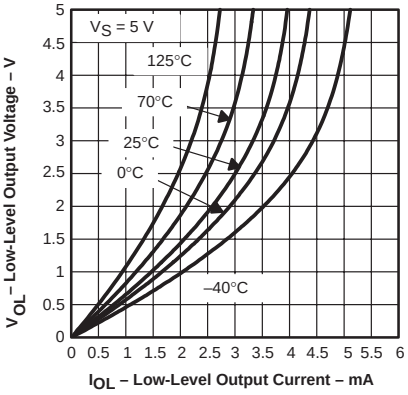



Figure 8

**HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT**

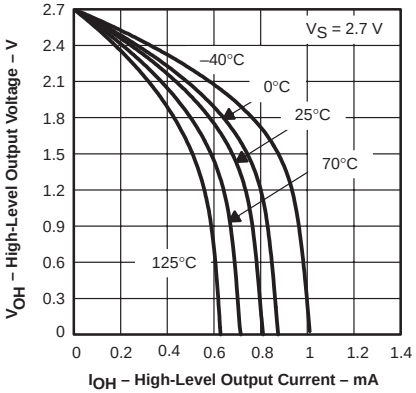



Figure 9

**LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT**

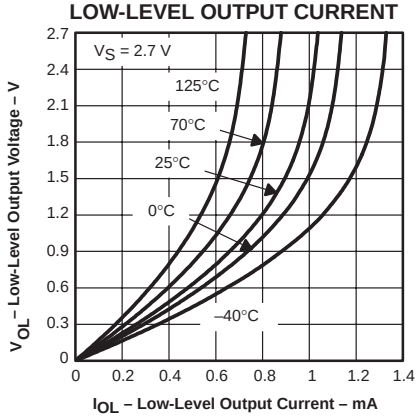



Figure 10

**QUIESCENT CURRENT vs SUPPLY VOLTAGE**

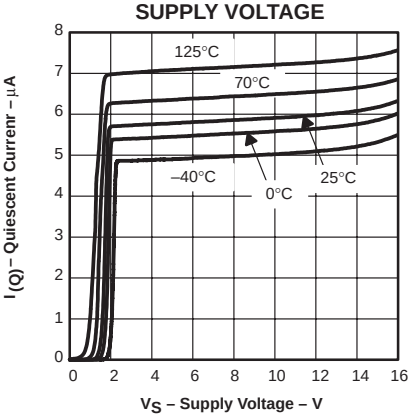



Figure 11

**QUIESCENT CURRENT vs FREE-AIR TEMPERATURE**

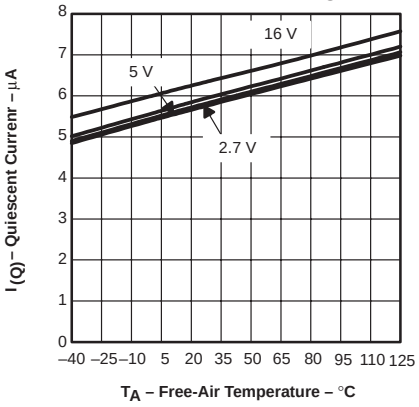



Figure 12

## TYPICAL CHARACTERISTICS

**SUPPLY VOLTAGE AND SUPPLY CURRENT RAMP UP**

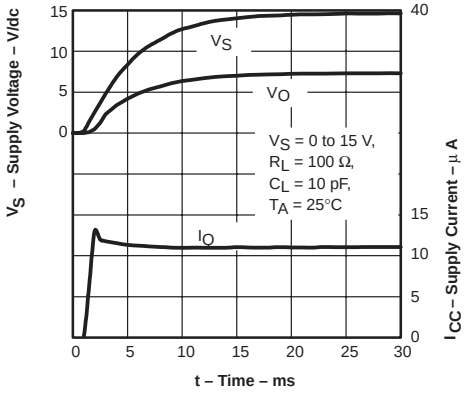



Figure 13

**DIFFERENTIAL VOLTAGE GAIN AND PHASE SHIFT vs FREQUENCY**

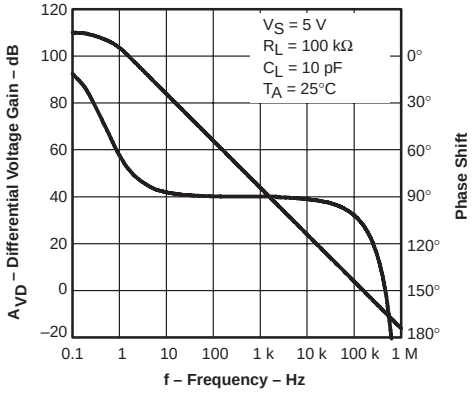



Figure 14

**GAIN-BANDWIDTH PRODUCT vs FREE-AIR TEMPERATURE**

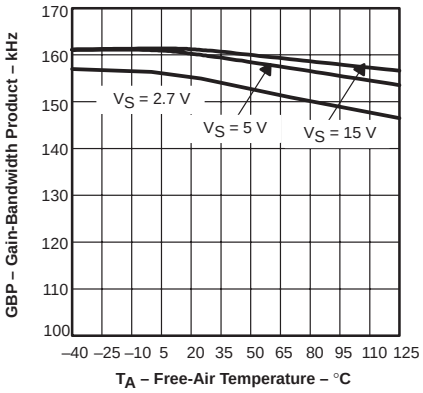



Figure 15

**PHASE MARGIN vs LOAD CAPACITANCE**

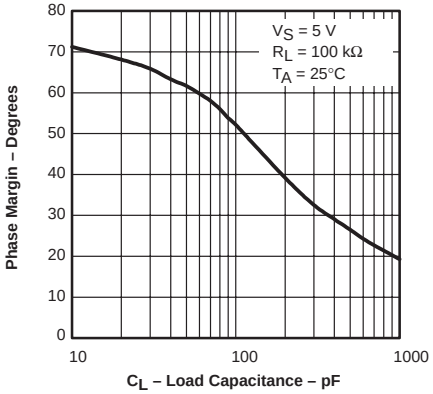



Figure 16

**COMMON-MODE REJECTION RATIO vs FREQUENCY**

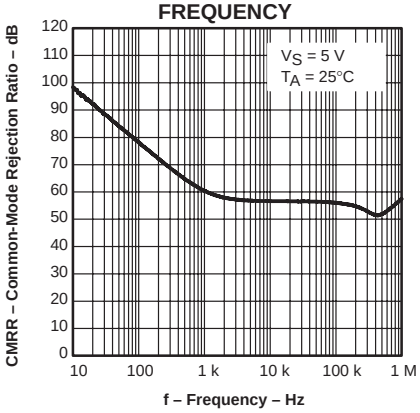



Figure 17

**POWER SUPPLY REJECTION RATIO vs FREQUENCY**

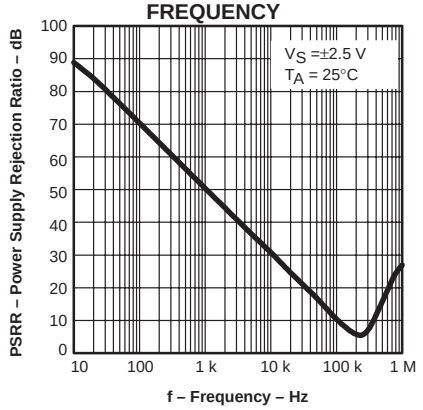



Figure 18

**INPUT REFERRED NOISE VOLTAGE vs FREQUENCY**

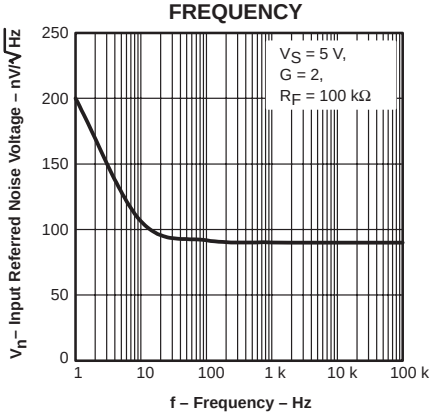



Figure 19

**SLEW RATE vs FREE-AIR TEMPERATURE**

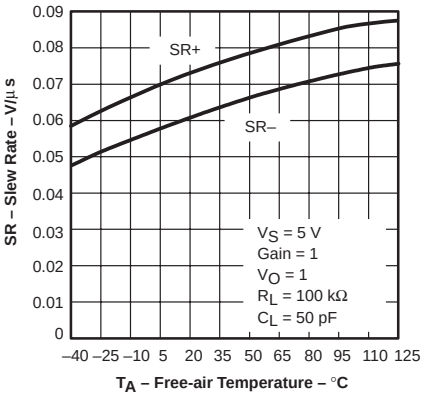



Figure 20

## TYPICAL CHARACTERISTICS

**PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY**

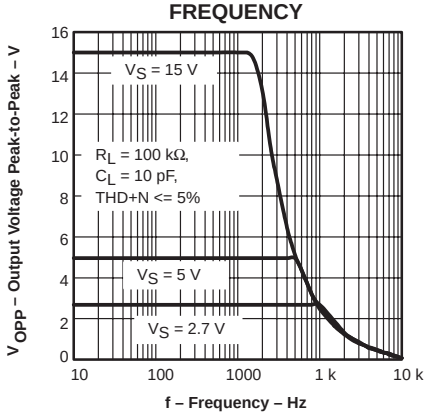



**Figure 21**

**INVERTING SMALL-SIGNAL RESPONSE**

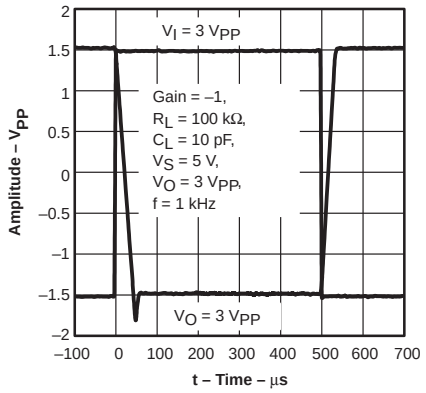



**Figure 22**

**INVERTING LARGE-SIGNAL RESPONSE**

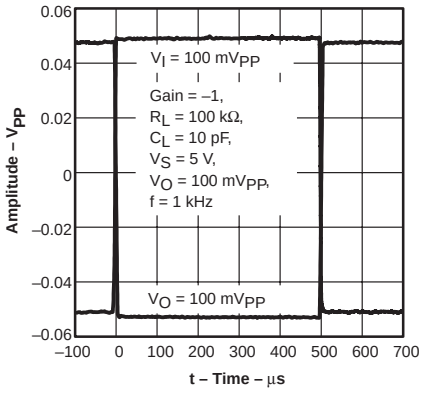



**Figure 23**

**CROSSTALK vs FREQUENCY**

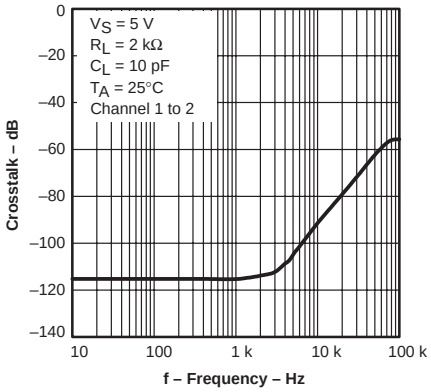
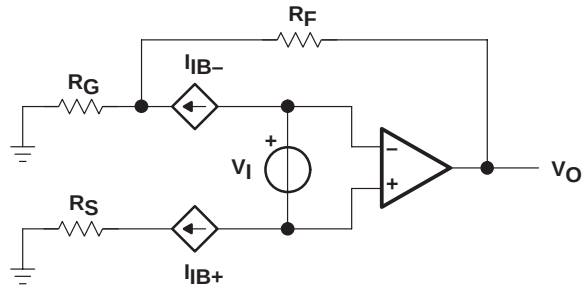



**Figure 24**

## APPLICATION INFORMATION

### offset voltage

The output offset voltage ($V_{OO}$) is the sum of the input offset voltage ($V_{IO}$) and both input bias currents ($I_{IB}$) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:

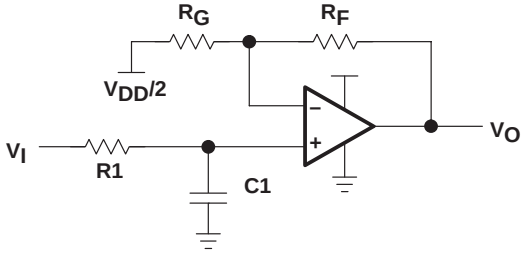



$$V_{OO} = V_{IO}\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB+}\ R_S\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB-}\ R_F$$

**Figure 25. Output Offset Voltage Model**

### general configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the amplifier (see Figure 26).

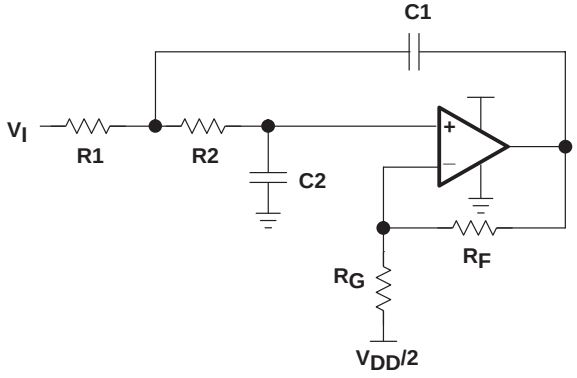



$$\frac{V_O}{V_I} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR1C1}\right)$$

$$f_{-3dB} = \frac{1}{2\pi R1C1}$$

**Figure 26. Single-Pole Low-Pass Filter**

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task. For best results, the amplifier should have a bandwidth that is 8 to 10 times the filter frequency bandwidth. Failure to do this can result in phase shift of the amplifier.




**R1 = R2 = R**
**C1 = C2 = C**
**Q = Peaking Factor**
**(Butterworth Q = 0.707)**

$$f_{-3dB} = \frac{1}{2\pi RC}$$

$$R_G = \frac{R_F}{\left(2 - \frac{1}{Q}\right)}$$

**Figure 27. 2-Pole Low-Pass Sallen-Key Filter**

## APPLICATION INFORMATION

### circuit layout considerations

To achieve the levels of high performance of the TLV238x, follow proper printed-circuit board design techniques. A general set of guidelines is given in the following.

- Ground planes—It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power supply decoupling—Use a 6.8-μF tantalum capacitor in parallel with a 0.1-μF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-μF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-μF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- Sockets—Sockets can be used but are not recommended. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- Short trace runs/compact part placements—Optimum high performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This will help to minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components—Using surface-mount passive components is recommended for high performance amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

## APPLICATION INFORMATION

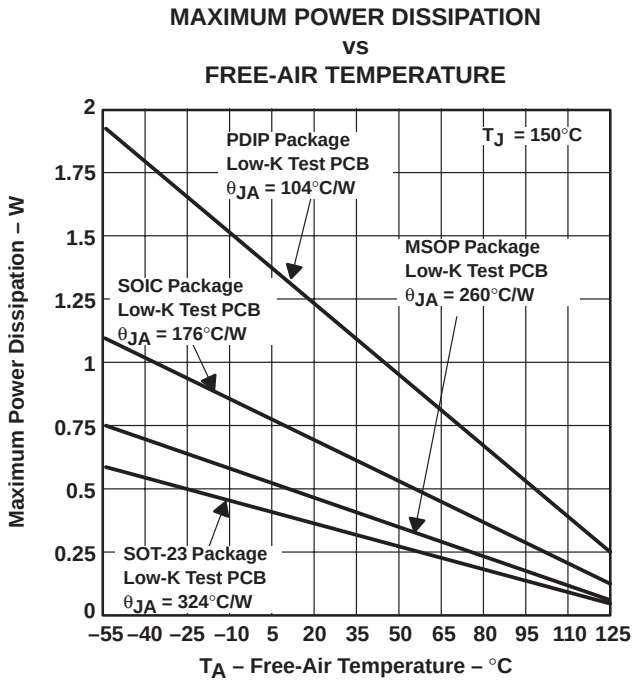
### general power dissipation considerations

For a given $\theta_{JA}$, the maximum power dissipation is shown in Figure 28 and is calculated by the following formula:

$$P_D = \left( \frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

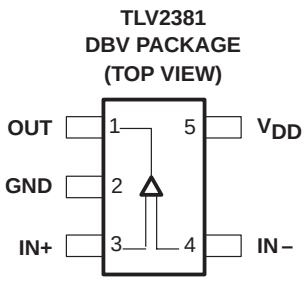
Where:

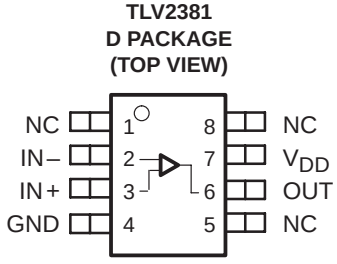
$P_D$ = Maximum power dissipation of TLV238x IC (watts)
$T_{MAX}$ = Absolute maximum junction temperature (150°C)
$T_A$ = Free-ambient air temperature (°C)
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
$\theta_{JC}$ = Thermal coefficient from junction to case
$\theta_{CA}$ = Thermal coefficient from case to ambient air (°C/W)

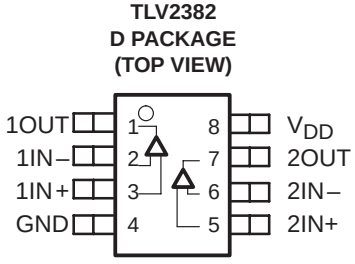



NOTE A: Results are with no air flow and using JEDEC Standard Low-K test PCB.

**Figure 28. Maximum Power Dissipation vs Free-Air Temperature**




NC – No internal connection

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV2381ID | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2381I | Samples |
| TLV2381IDBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VBKI | Samples |
| TLV2381IDBVRG4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VBKI | Samples |
| TLV2381IDBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VBKI | Samples |
| TLV2381IDR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2381I | Samples |
| TLV2382ID | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2382I | Samples |
| TLV2382IDG4 | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2382I | Samples |
| TLV2382IDR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2382I | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

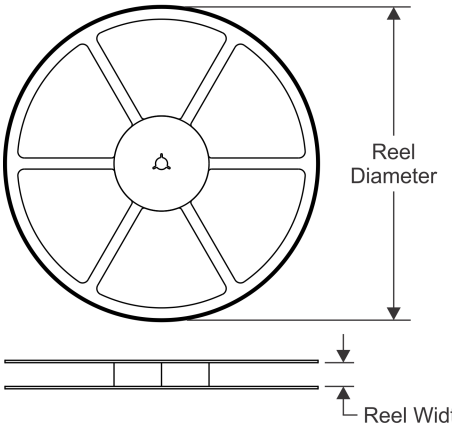
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

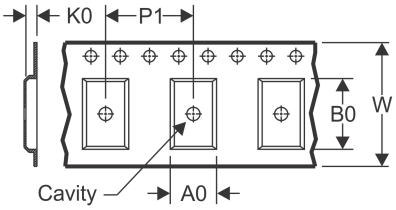
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

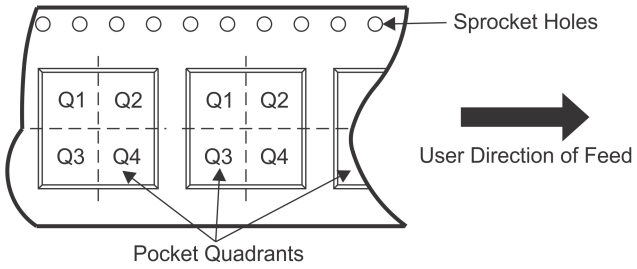



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

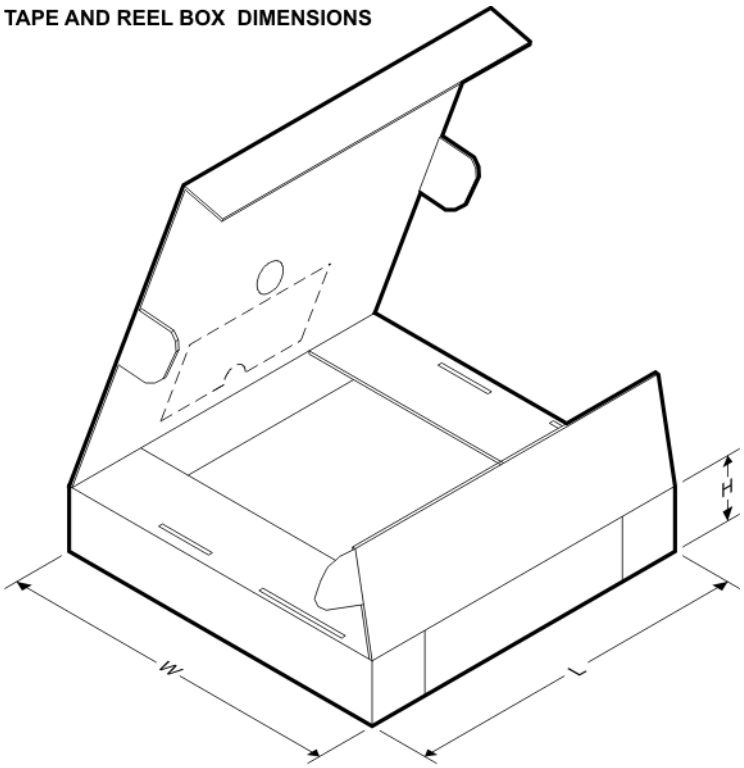
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV2381IDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 9.0 | 3.15 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV2381IDBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 9.0 | 3.15 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV2381IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLV2382IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

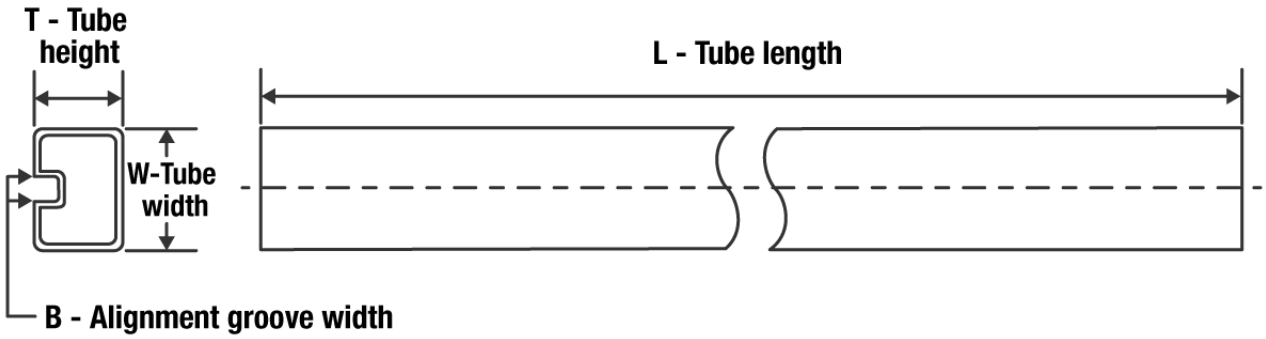
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TLV2381IDBVR | SOT-23 | DBV | 5 | 3000 | 182.0 | 182.0 | 20.0 |
| TLV2381IDBVT | SOT-23 | DBV | 5 | 250 | 182.0 | 182.0 | 20.0 |
| TLV2381IDR | SOIC | D | 8 | 2500 | 340.5 | 336.1 | 25.0 |
| TLV2382IDR | SOIC | D | 8 | 2500 | 340.5 | 336.1 | 25.0 |

## TUBE




*All dimensions are nominal

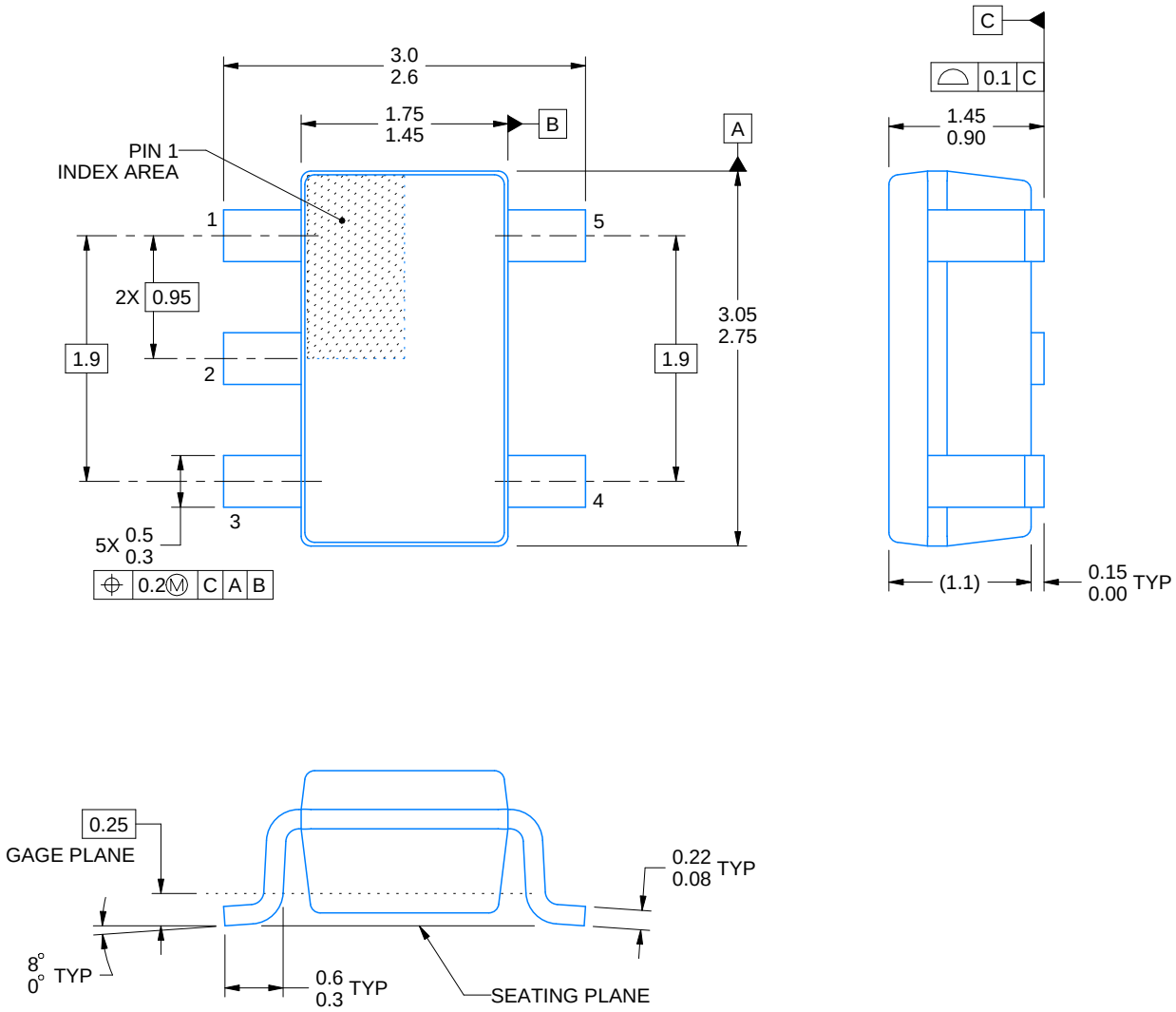
| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| TLV2381ID | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| TLV2382ID | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| TLV2382IDG4 | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |

# PACKAGE OUTLINE

## DBV0005A

## SOT-23 - 1.45 mm max height

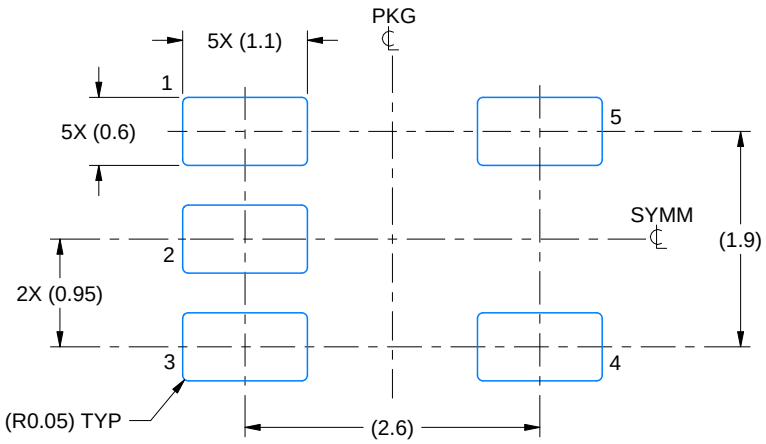
SMALL OUTLINE TRANSISTOR



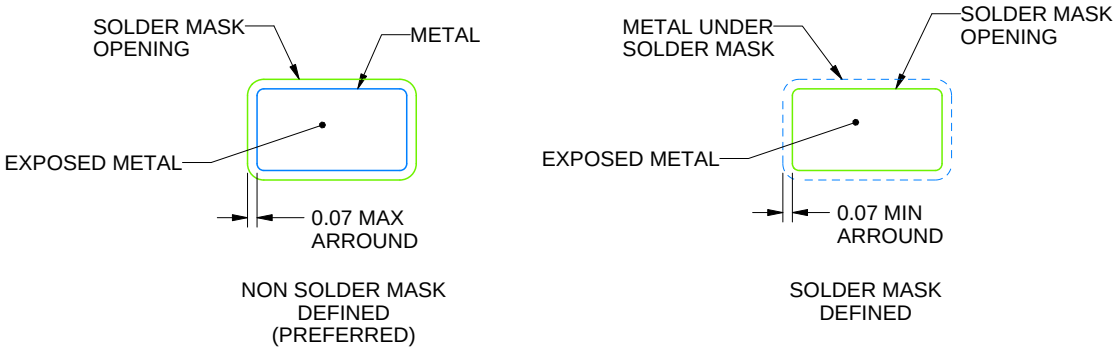

4214839/F 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

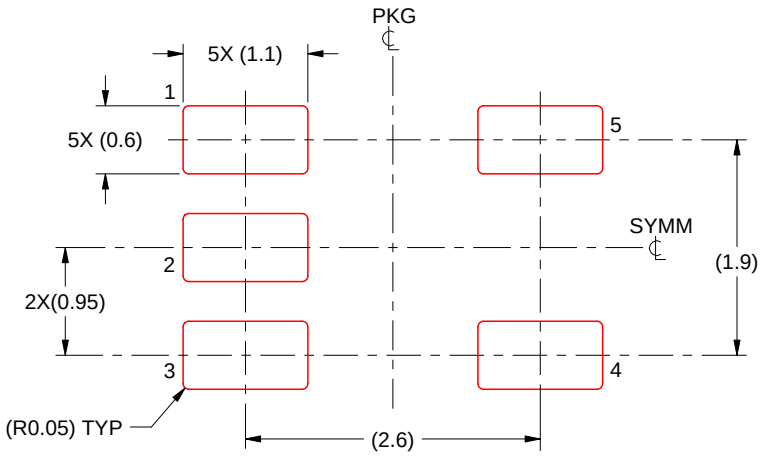



SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

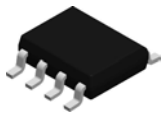



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/F 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

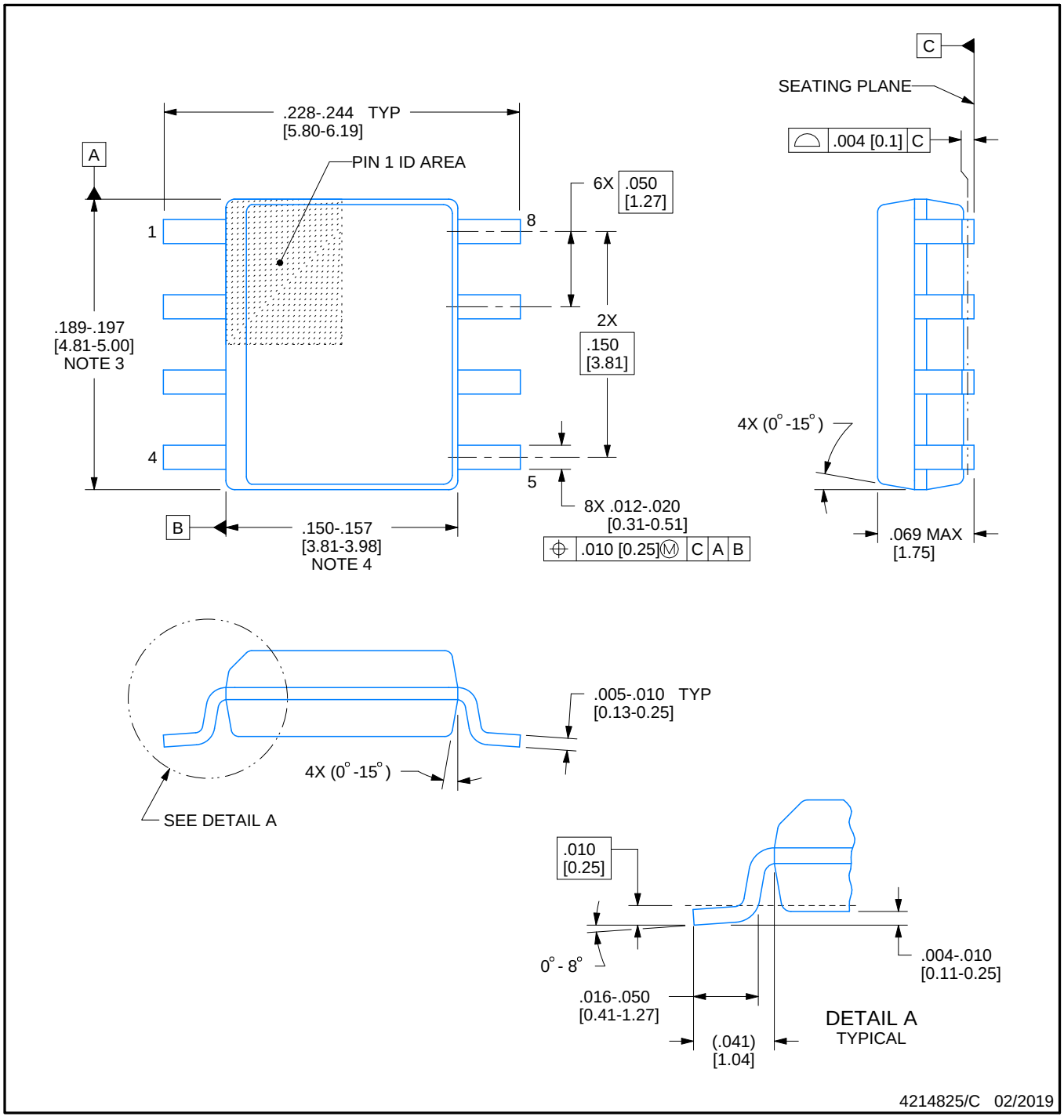


# PACKAGE OUTLINE

## D0008A

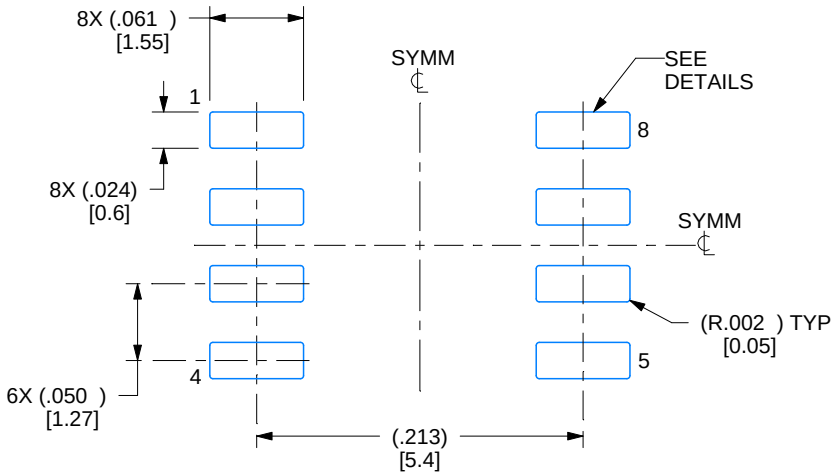
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

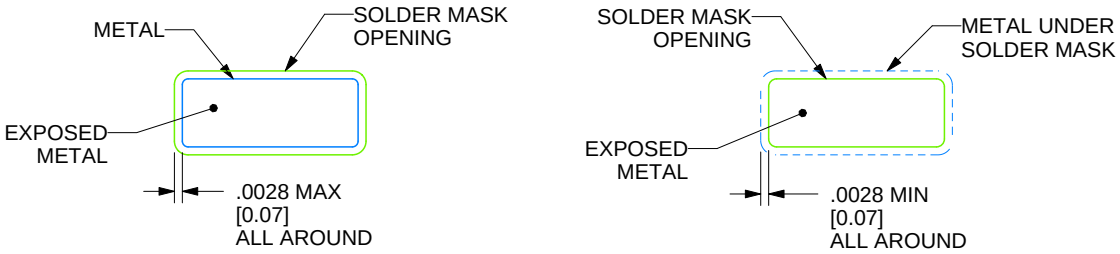



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X




SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

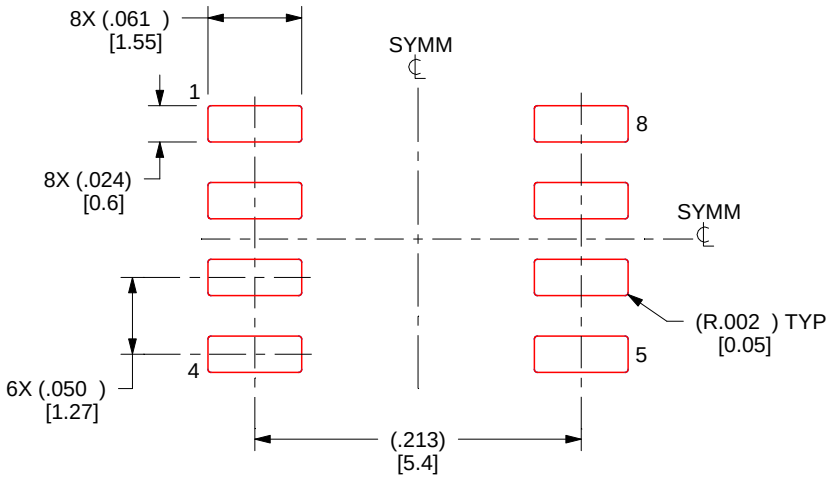
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0008A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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