High Speed, High Voltage, 1 A Output Drive Amplifier

Data Sheet **ADA4870**

FEATURES

Ideal for driving high capacitive or low resistive loads
Wide supply range: 10 V to 40 V
High output current drive: 1 A
Wide output voltage swing: 37 V swing with 40 V supply
High slew rate: 2500 V/µs
High bandwidth: 52 MHz large signal, 70 MHz small signal
Low noise: 2.1 nV/√Hz
Quiescent current: 32.5 mA
Power down: 0.75 mA
Short-circuit protection and flag
Current limit: 1.2 A
Thermal protection

APPLICATIONS

Envelope tracking
Power FET driver
Ultrasound
Piezo drivers
PIN diode drivers
Waveform generation
Automated test equipment (ATE)
CCD panel drivers
Composite amplifiers

FUNCTIONAL BLOCK DIAGRAM

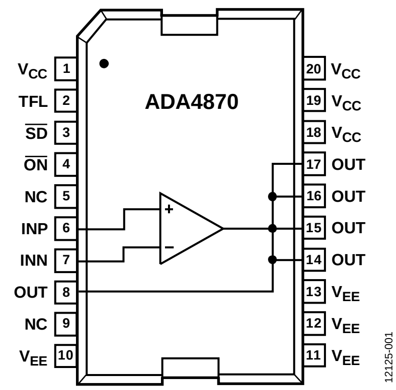

Figure 1.

GENERAL DESCRIPTION

The ADA4870 is a unity gain stable, high speed current feedback amplifier capable of delivering 1 A of output current and 2500 V/µs slew rate from a 40 V supply. Manufactured using the Analog Devices, Inc., proprietary high voltage extra fast complementary bipolar (XFCB) process, the innovative architecture of the ADA4870 enables high output power, high speed signal processing solutions in applications that require driving a low impedance load.

The ADA4870 is ideal for driving high voltage power FETs, piezo transducers, PIN diodes, CCD panels, and a variety of other demanding applications that require high speed from high supply voltage at high output current.

The ADA4870 is available in a power SOIC package (PSOP_3), featuring an exposed thermal slug that provides high thermal conductivity, enabling efficient heat transfer for improved performance and reliability in demanding applications. The ADA4870 operates over the industrial temperature range (−40°C to +85°C).

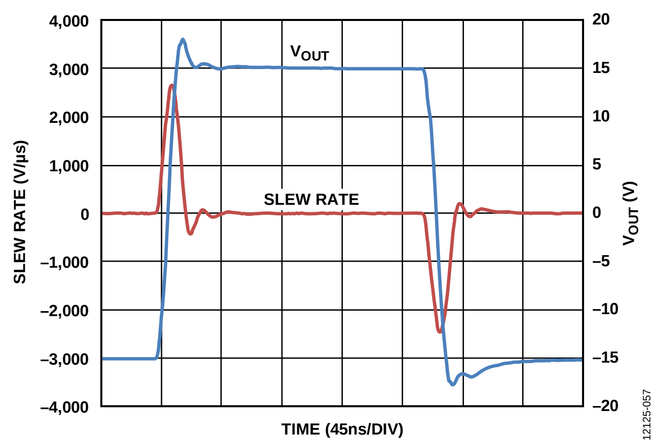

Figure 2. Slew Rate, $V_S = \pm 20$ V, $V_{OUT} = 30$ V p-p, $A_V = +2$, $R_F = 1.5$ kΩ, $C_L = 300$ pF, $R_S = 5$ Ω

Rev. 0 **Document Feedback**

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REVISION HISTORY

5/14—Revision 0: Initial Version

SPECIFICATIONS

±20 V SUPPLY

T_{CASE} = 25°C, A_V = −5, R_F = 1.21 kΩ, R_G = 243 Ω, C_L = 300 pF, R_S = 5 Ω, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_{OUT} = 2 V p-p		60		MHz
	V_{OUT} = 2 V p-p, A_V = +2		70		MHz
	V_{OUT} = 20 V p-p		52		MHz
Slew Rate (Peak)	V_{OUT} = 30 V step, A_V = +2		2500		V/µs
Settling Time to 0.1%	V_{OUT} = 10 V step		82		ns
NOISE/DISTORTION PERFORMANCE					
Harmonic Distortion, HD2/HD3	f = 30 MHz, V_{OUT} = 20 V p-p, A_V = −10		−40/−39		dBc
	f = 1 MHz, V_{OUT} = 20 V p-p, A_V = −10		−91/−74		dBc
	f = 0.1 MHz, V_{OUT} = 20 V p-p, A_V = −10		−95/−96		dBc
	f = 1 MHz, V_{OUT} = 20 V p-p, R_L = 25 Ω, A_V = −10		−70/−77		dBc
	f = 0.1 MHz, V_{OUT} = 20 V p-p, R_L = 25 Ω, A_V = −10		−79/−99		dBc
Input Voltage Noise Density	f = 100 kHz		2.1		nV/√Hz
Input Current Noise Density	f = 100 kHz				
INP			4.2		pA/√Hz
INN			47		pA/√Hz
DC PERFORMANCE					
Input Offset Voltage		−15	−1	+10	mV
Input Offset Voltage Drift			4		µV/°C
Input Bias Current					
Noninverting Input			9	23	µA
Inverting Input			−12	−25	µA
Input Bias Current Drift, Inverting Input			24		nA/°C
Open-Loop Transresistance			2.5		MΩ
INPUT CHARACTERISTICS					
Input Resistance	INP		2		MΩ
Input Capacitance	INP		0.75		pF
Input Common-Mode Voltage Range (V_{ICM})			±18		V
Common-Mode Rejection Ratio	V_{ICM} = ±2 V, ±18 V	58	60		dB
$\overline{SD}$ PIN (SHUTDOWN)					
Input Voltages	High (enabled)	V_{EE} + 1.1		V_{EE} + 5	V
	Low (power-down)	V_{EE}		V_{EE} + 0.9	V
Input Bias Current	Enabled ($\overline{SD}$ = V_{EE} + 5 V)		110		µA
	Power down $\overline{SD}$ = V_{EE})		−50		µA
$\overline{ON}$ PIN (RESET AND SHORT-CIRCUIT PROTECTION)					
Input Voltages	High (power-down)	V_{EE} + 1.8		V_{EE} + 5	V
	Low (enabled)	V_{EE}		V_{EE} + 1.3	V
Input Bias Current	Enabled ($\overline{ON}$ = V_{EE})		−75		µA
	Power down ($\overline{ON}$ = V_{EE} + 5 V)		100		µA
OUTPUT CHARACTERISTICS					
Output Voltage Range	R_G = 1.2 kΩ, R_L = open		±18.6		V
	R_G = 1.2 kΩ, R_L = 50 Ω		±18		V
Output Current Drive			1		A
Short-Circuit Protection Current Limit	$\overline{ON}$ = floating		1.2		A

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY					
Operating Range		10		40	V
Quiescent Current	$\overline{SD}$ = V_{EE} + 5 V, $\overline{ON}$ = V_{EE}		32.5	33	mA
	$\overline{SD}$ = V_{EE}, $\overline{ON}$ = not applicable		0.75	1	mA
	$\overline{SD}$ = V_{EE} + 5 V, $\overline{ON}$ = V_{EE} + 5 V		5.1	5.8	mA
Positive Power Supply Rejection Ratio		67	69		dB
Negative Power Supply Rejection Ratio		62	64		dB

±5 V SUPPLY

T_{CASE} = 25°C, A_V = −5, R_F = 1.21 kΩ, R_G = 243 Ω, C_L = 300 pF, R_S = 5 Ω, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_{OUT} = 2 V p-p		52		MHz
Settling Time to 0.1%	V_{OUT} = 2 V step		55		ns
NOISE/DISTORTION PERFORMANCE					
Harmonic Distortion, HD2/HD3	f = 30 MHz, V_{OUT} = 2 V p-p, A_V = −10		−42/−38		dBc
	f = 1 MHz, V_{OUT} = 2 V p-p, A_V = −10		−90/−88		dBc
	f = 0.1 MHz, V_{OUT} = 2 V p-p, A_V = −10		−101/−107		dBc
	f = 1 MHz, V_{OUT} = 2 V p-p, R_L = 25 Ω, A_V = −10		−70/−66		dBc
	f = 0.1 MHz, V_{OUT} = 2 V p-p, R_L = 25 Ω, A_V = −10		−85/−86		dBc
Input Voltage Noise Density	f = 100 kHz		2.1		nV/√Hz
Input Current Noise Density	f = 100 kHz				
INP			4.2		pA/√Hz
INN			47		pA/√Hz
DC PERFORMANCE					
Input Offset Voltage		−15	−4	+5	mV
Input Offset Voltage Drift			14		µV/°C
Input Bias Current					
Noninverting Input			13	23	µA
Inverting Input			−5	−18	µA
Input Bias Current Drift, Inverting Input			10		nA/°C
Open-Loop Transresistance			1.9		MΩ
INPUT CHARACTERISTICS					
Input Resistance	INP		2		MΩ
Input Capacitance	INP		0.75		pF
Input Common-Mode Voltage Range (V_{ICM})			±3.0		V
Common-Mode Rejection Ratio	V_{ICM} = ±0.5 V, ±3.0 V	57	59		dB
$\overline{SD}$ PIN (SHUTDOWN)					
Input Voltages	High (enabled)	V_{EE} + 1.1		V_{EE} + 5	V
	Low (power-down)	V_{EE}		V_{EE} + 0.9	V
Input Bias Current	Enabled ($\overline{SD}$ = V_{EE} + 5 V)		110		µA
	Power down ($\overline{SD}$ = V_{EE})		−65		µA
$\overline{ON}$ PIN (RESET AND SHORT-CIRCUIT PROTECTION)					
Input Voltages	High (power-down)	V_{EE} + 1.8		V_{EE} + 5	V
	Low (enabled)	V_{EE}		V_{EE} + 1.3	V
Input Bias Current	Enabled ($\overline{ON}$ = V_{EE})		−75		µA
	Power down ($\overline{ON}$ = V_{EE} + 5 V)		100		µA

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OUTPUT CHARACTERISTICS					
Output Voltage Range	R_G = 1.2 kΩ, R_L = open		±3.7		V
Output Current Drive			1		A
Short-Circuit Protection Current Limit	$\overline{ON}$ = floating		1.2		A
POWER SUPPLY					
Operating Range		10		40	V
Quiescent Current	$\overline{SD}$ = V_{EE} + 5 V, $\overline{ON}$ = V_{EE}		28	30	mA
	$\overline{SD}$ = V_{EE}, $\overline{ON}$ = not applicable		0.65	1	mA
	$\overline{SD}$ = V_{EE} + 5 V, $\overline{ON}$ = V_{EE} + 5 V		4.7	5.5	mA
Positive Power Supply Rejection Ratio		66	68		dB
Negative Power Supply Rejection Ratio		61	63		dB

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	42 V
Power Dissipation	See the Power Dissipation section and the Safe Operating Area section
Common-Mode Input Voltage Range	V_{EE} to V_{CC}
Differential Input Voltage Range	±0.7 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C
Junction Temperature	150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation in the package is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Exceeding a junction temperature of 150°C can result in changes in the silicon devices, potentially causing failure. Table 4 shows the junction to case thermal resistance (θ_{JC}) for the PSOP_3 package. For more detailed information on power dissipation and thermal management, see the Applications Information section.

Table 4. Thermal Resistance

Package Type	θ_{JC}	Unit
20-Lead PSOP_3	1.1	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

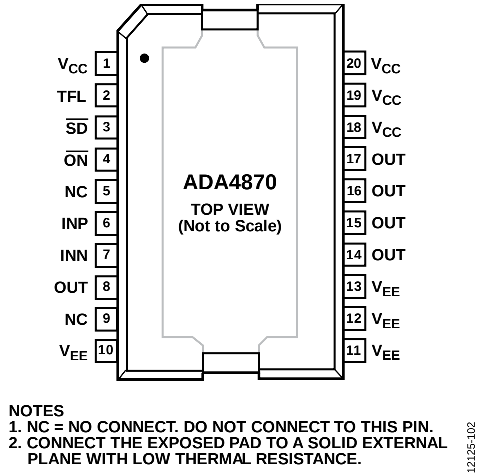


Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{CC}	Positive Power Supply Input.
2	TFL	Thermal Monitor and Short-Circuit Flag (Referenced to V_{EE}).
3	$\overline{SD}$	Shutdown (Active Low, Referenced to V_{EE}).
4	$\overline{ON}$	Turn On/Enable (Active Low, Referenced to V_{EE}).
5	NC	No Connect. Do not connect to this pin.
6	INP	Noninverting Input.
7	INN	Inverting Input.
8	OUT	Output Connection for Feedback Resistor.
9	NC	No Connect. Do not connect to this pin.
10 to 13	V_{EE}	Negative Power Supply Input.
14 to 17	OUT	Output.
18 to 20	V_{CC}	Positive Power Supply Input.
	EPAD	Exposed Thermal Pad. No internal electrical connection. Connect the exposed pad to a solid external plane with low thermal resistance.

TYPICAL PERFORMANCE CHARACTERISTICS

T_{CASE} = 25°C, unless otherwise noted.

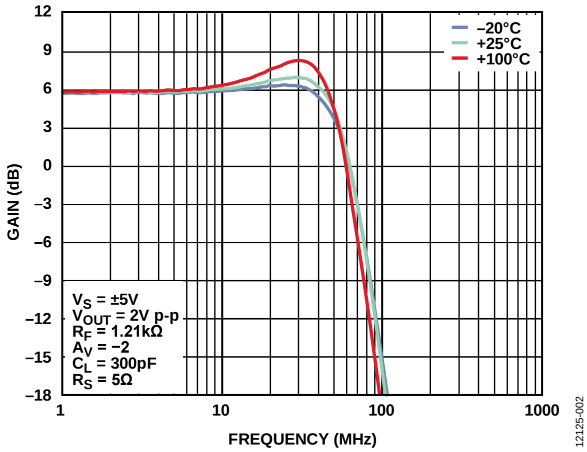


Figure 4. Small Signal Frequency Response vs. Case Temperature, A_V = −2, V_S = ±5 V, V_{OUT} = 2 V p-p, R_F = 1.21 kΩ, C_L = 300 pF, R_S = 5 Ω

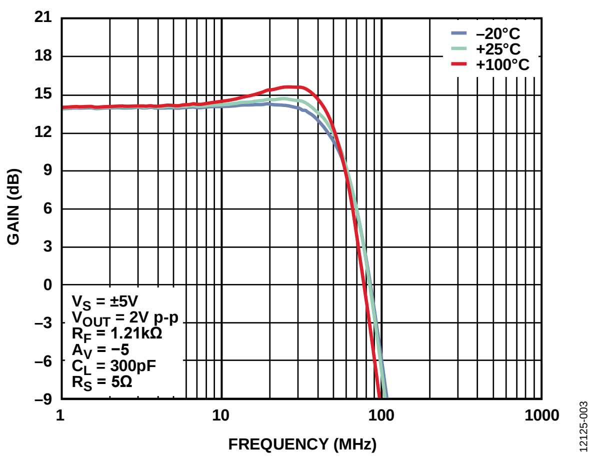


Figure 5. Small Signal Frequency Response vs. Case Temperature, A_V = −5, V_S = ±5 V, V_{OUT} = 2 V p-p, R_F = 1.21 kΩ, C_L = 300 pF, R_S = 5 Ω

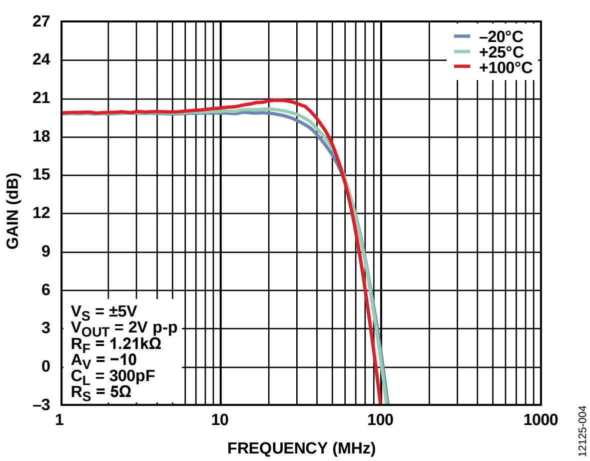


Figure 6. Small Signal Frequency Response vs. Case Temperature, A_V = −10, V_S = ±5 V, V_{OUT} = 2 V p-p, R_F = 1.21 kΩ, C_L = 300 pF, R_S = 5 Ω

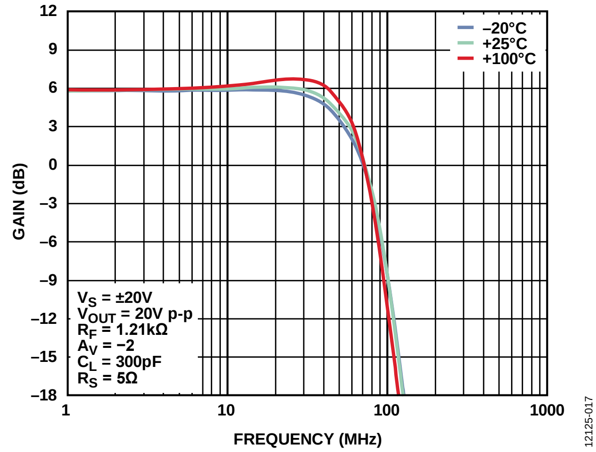


Figure 7. Large Signal Frequency Response vs. Case Temperature, A_V = −2, V_S = ±20 V, V_{OUT} = 20 V p-p, R_F = 1.21 kΩ, C_L = 300 pF, R_S = 5 Ω

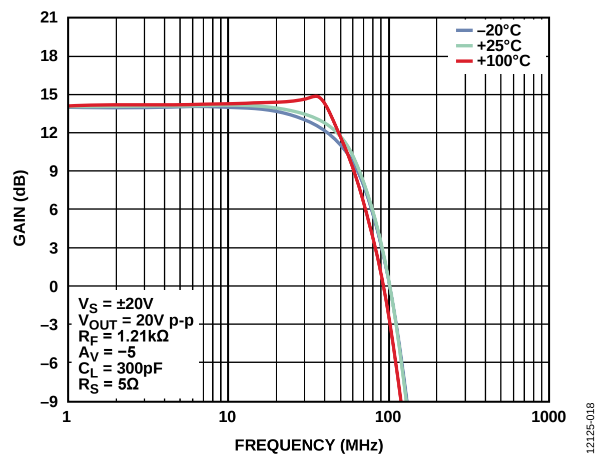


Figure 8. Large Signal Frequency Response vs. Case Temperature, A_V = −5, V_S = ±20 V, V_{OUT} = 20 V p-p, R_F = 1.21 kΩ, C_L = 300 pF, R_S = 5 Ω

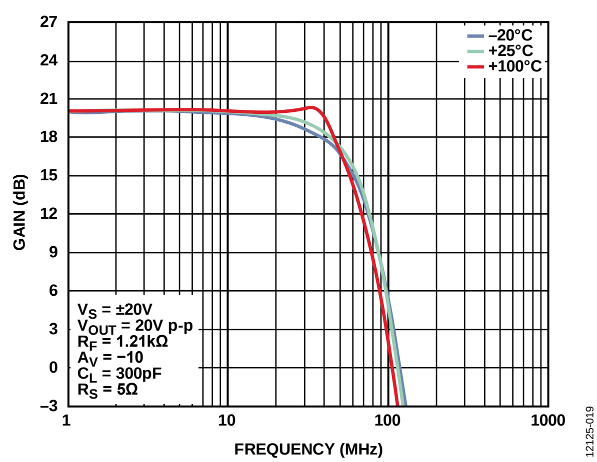


Figure 9. Large Signal Frequency Response vs. Case Temperature, A_V = −10, V_S = ±20 V, V_{OUT} = 20 V p-p, R_F = 1.21 kΩ, C_L = 300 pF, R_S = 5 Ω

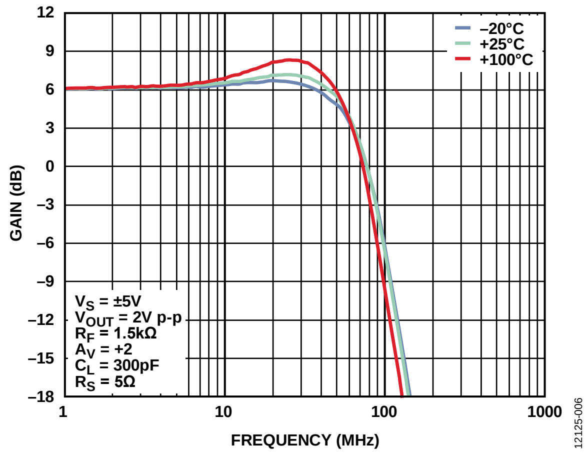


Figure 10. Small Signal Frequency Response vs. Case Temperature, $A_V = +2$, $V_S = \pm5$ V, $V_{OUT} = 2$ V p-p, $R_F = 1.5$ kΩ, $C_L = 300$ pF, $R_S = 5$ Ω

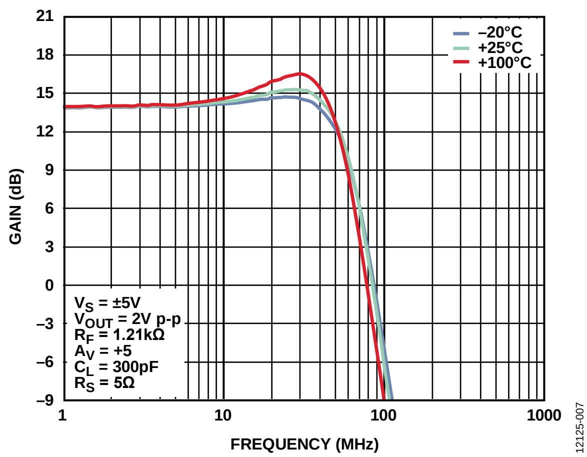


Figure 11. Small Signal Frequency Response vs. Case Temperature, $A_V = +5$, $V_S = \pm5$ V, $V_{OUT} = 2$ V p-p, $R_F = 1.21$ kΩ, $C_L = 300$ pF, $R_S = 5$ Ω

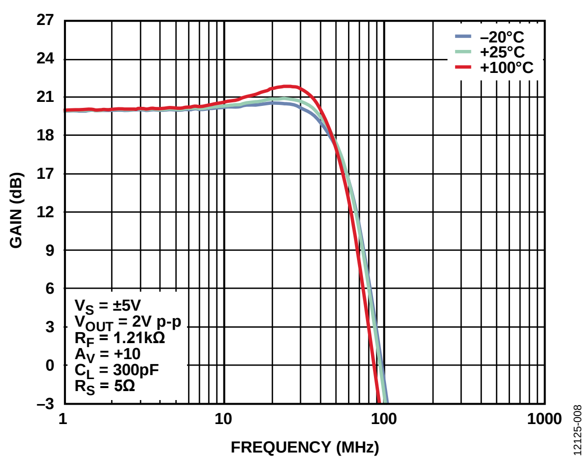


Figure 12. Small Signal Frequency Response vs. Case Temperature, $A_V = +10$, $V_S = \pm5$ V, $V_{OUT} = 2$ V p-p, $R_F = 1.21$ kΩ, $C_L = 300$ pF, $R_S = 5$ Ω

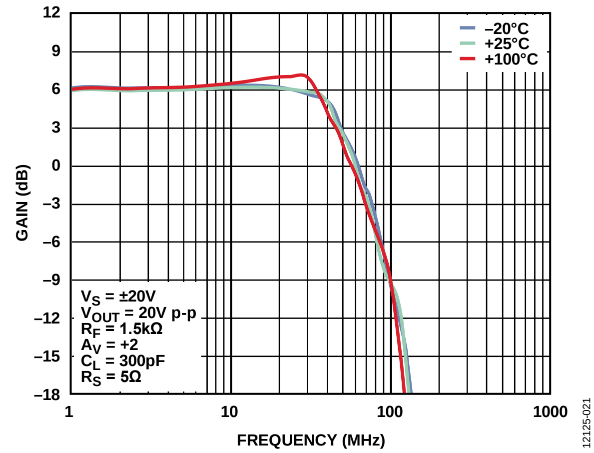


Figure 13. Large Signal Frequency Response vs. Case Temperature, $A_V = +2$, $V_S = \pm20$ V, $V_{OUT} = 20$ V p-p, $R_F = 1.5$ kΩ, $C_L = 300$ pF, $R_S = 5$ Ω

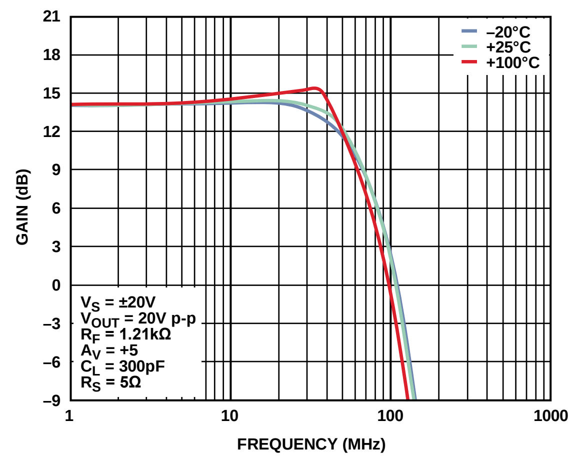


Figure 14. Large Signal Frequency Response vs. Case Temperature, $A_V = +5$, $V_S = \pm20$ V, $V_{OUT} = 20$ V p-p, $R_F = 1.21$ kΩ, $C_L = 300$ pF, $R_S = 5$ Ω

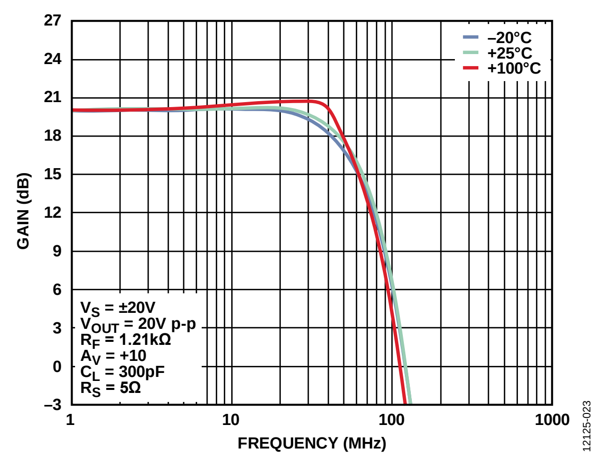


Figure 15. Large Signal Frequency Response vs. Case Temperature, $A_V = +10$, $V_S = \pm20$ V, $V_{OUT} = 20$ V p-p, $R_F = 1.21$ kΩ, $C_L = 300$ pF, $R_S = 5$ Ω

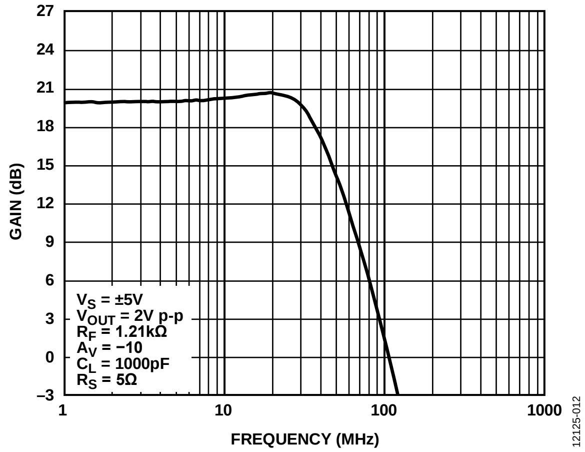


Figure 16. Small Signal Frequency Response, $A_V = -10$, $V_S = \pm 5$ V, $V_{OUT} = 2$ V p-p, $R_F = 1.21$ kΩ, $C_L = 1000$ pF, $R_S = 5$ Ω

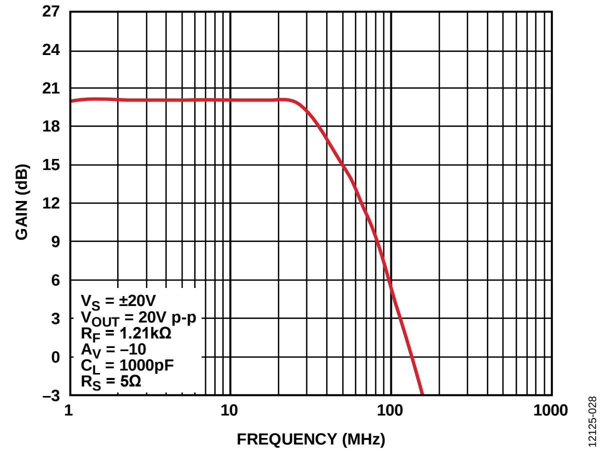


Figure 19. Large Signal Frequency Response, $A_V = -10$, $V_S = \pm 20$ V, $V_{OUT} = 20$ V p-p, $R_F = 1.21$ kΩ, $C_L = 1000$ pF, $R_S = 5$ Ω

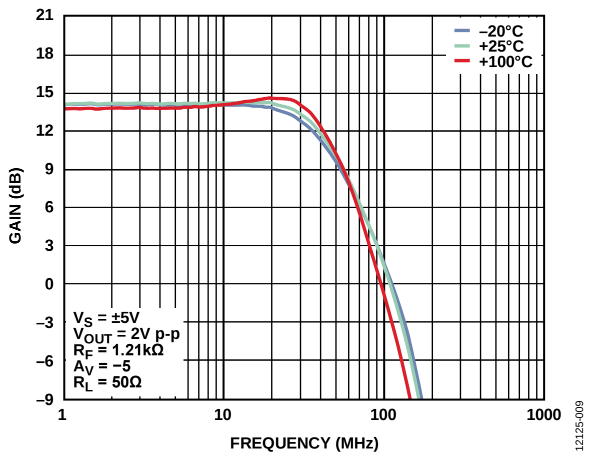


Figure 17. Small Signal Frequency Response vs. Case Temperature, $A_V = -5$, $V_S = \pm 5$ V, $V_{OUT} = 2$ V p-p, $R_F = 1.21$ kΩ, $R_L = 50$ Ω

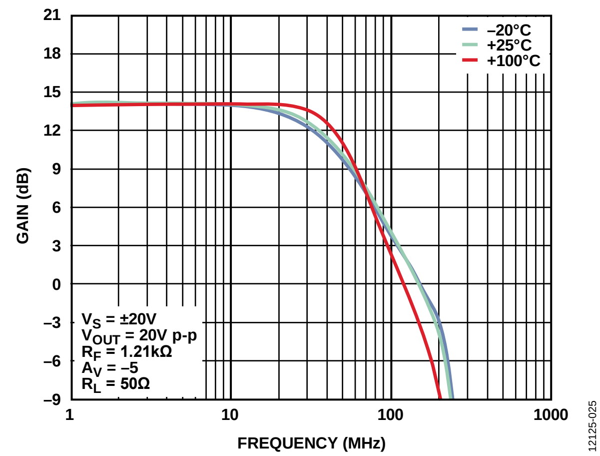


Figure 20. Large Signal Frequency Response vs. Case Temperature, $A_V = -5$, $V_S = \pm 20$ V, $V_{OUT} = 20$ V p-p, $R_F = 1.21$ kΩ, $R_L = 50$ Ω

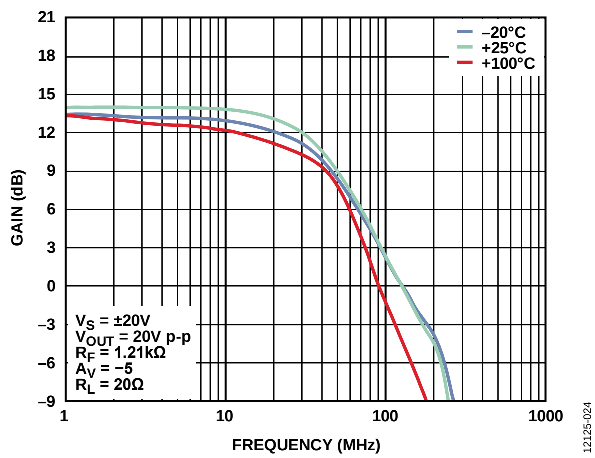


Figure 18. Large Signal Frequency Response vs. Case Temperature, $A_V = -5$, $V_S = \pm 20$ V, $V_{OUT} = 20$ V p-p, $R_F = 1.21$ kΩ, $R_L = 20$ Ω

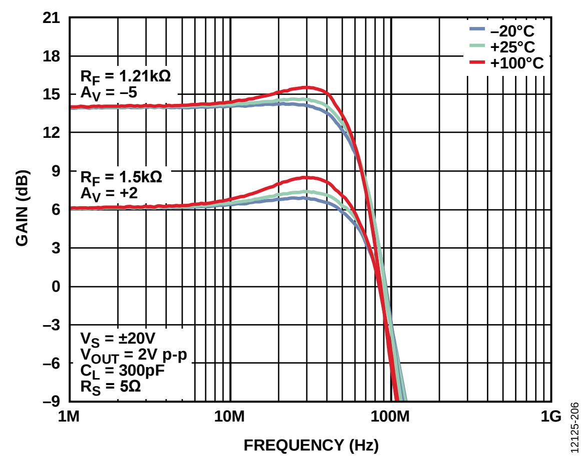


Figure 21. Small Signal Frequency Response vs. Case Temperature, $V_S = \pm 20$ V, $V_{OUT} = 2$ V p-p, $C_L = 300$ pF, $R_S = 5$ Ω

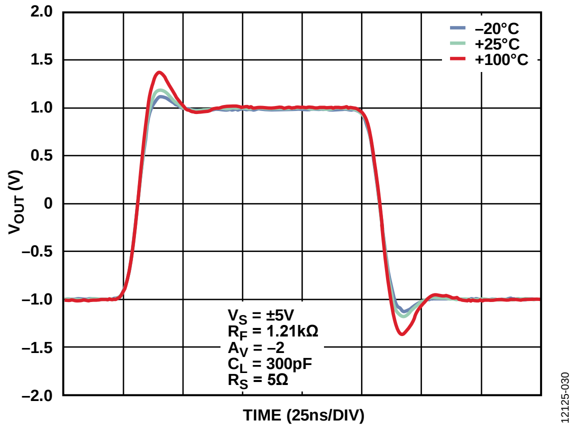


Figure 22. Small Signal Pulse Response vs. Case Temperature, $A_V = -2$, $V_S = \pm 5$ V, $V_{OUT} = 2$ V p-p, $R_F = 1.21$ kΩ, $C_L = 300$ pF, $R_S = 5$ Ω

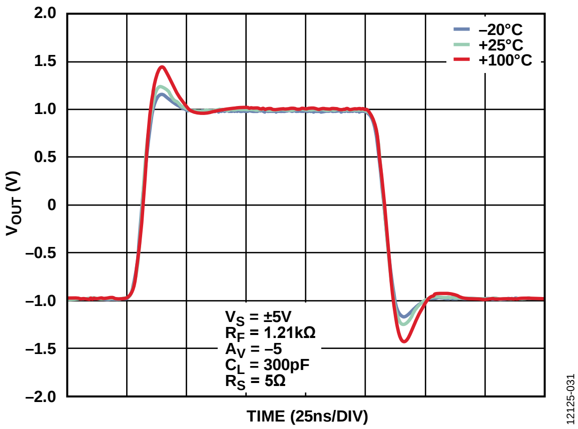


Figure 23. Small Signal Pulse Response vs. Case Temperature, $A_V = -5$, $V_S = \pm 5$ V, $V_{OUT} = 2$ V p-p, $R_F = 1.21$ kΩ, $C_L = 300$ pF, $R_S = 5$ Ω

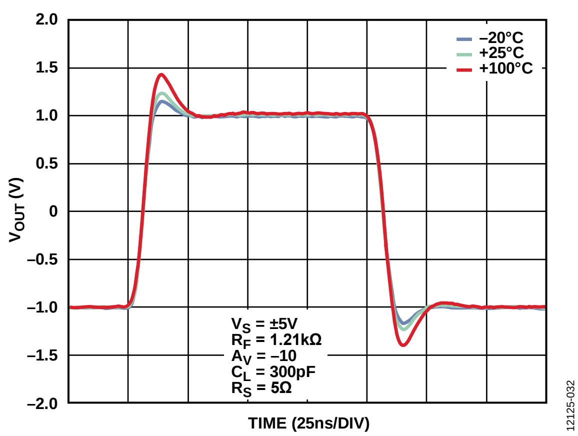


Figure 24. Small Signal Pulse Response vs. Case Temperature, $A_V = -10$, $V_S = \pm 5$ V, $V_{OUT} = 2$ V p-p, $R_F = 1.21$ kΩ, $C_L = 300$ pF, $R_S = 5$ Ω

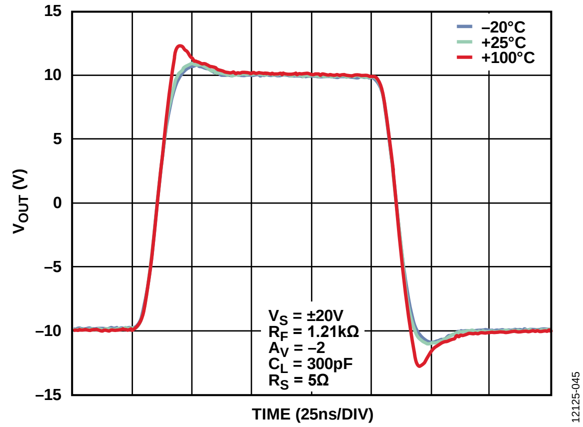


Figure 25. Large Signal Pulse Response vs. Case Temperature, $A_V = -2$, $V_S = \pm 20$ V, $V_{OUT} = 20$ V p-p, $R_F = 1.21$ kΩ, $C_L = 300$ pF, $R_S = 5$ Ω

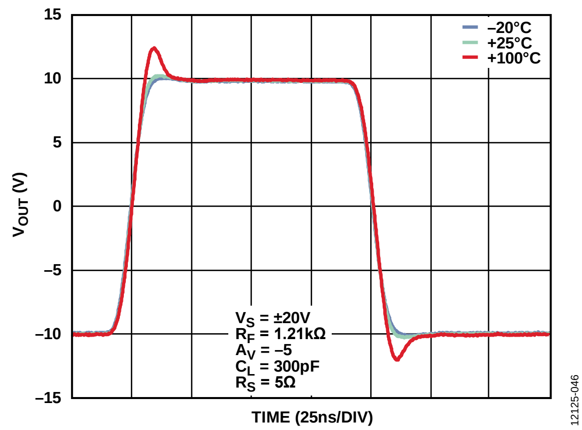


Figure 26. Large Signal Pulse Response vs. Case Temperature, $A_V = -5$, $V_S = \pm 20$ V, $V_{OUT} = 20$ V p-p, $R_F = 1.21$ kΩ, $C_L = 300$ pF, $R_S = 5$ Ω

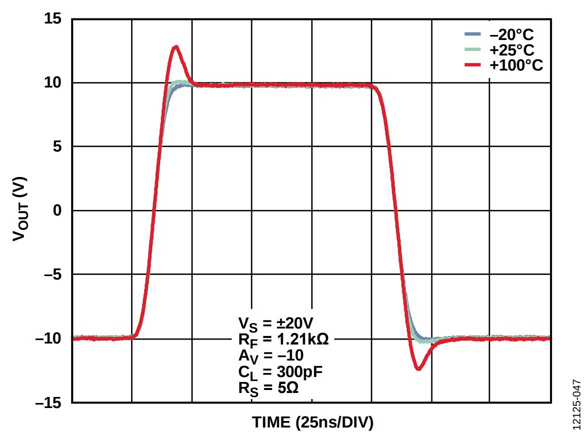


Figure 27. Large Signal Pulse Response vs. Case Temperature, $A_V = -10$, $V_S = \pm 20$ V, $V_{OUT} = 20$ V p-p, $R_F = 1.21$ kΩ, $C_L = 300$ pF, $R_S = 5$ Ω

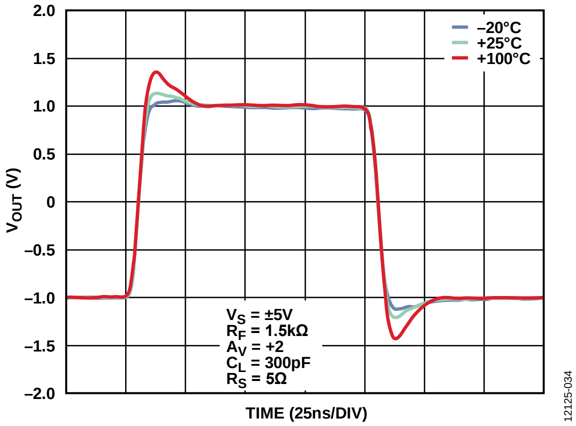


Figure 28. Small Signal Pulse Response vs. Case Temperature, A_V = +2, V_S = ±5 V, V_{OUT} = 2 V p-p, R_F = 1.5 kΩ, C_L = 300 pF, R_S = 5 Ω

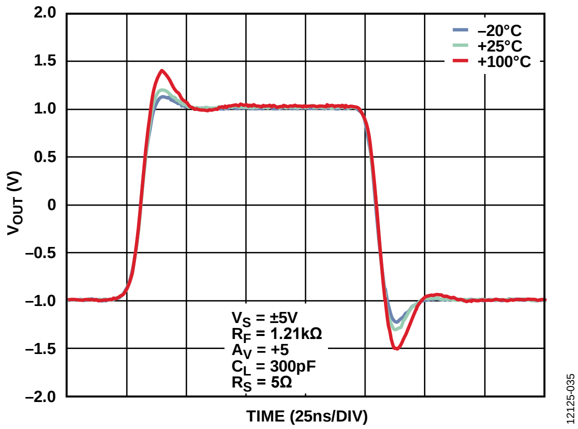


Figure 29. Small Signal Pulse Response vs. Case Temperature, A_V = +5, V_S = ±5 V, V_{OUT} = 2 V p-p, R_F = 1.21 kΩ, C_L = 300 pF, R_S = 5 Ω

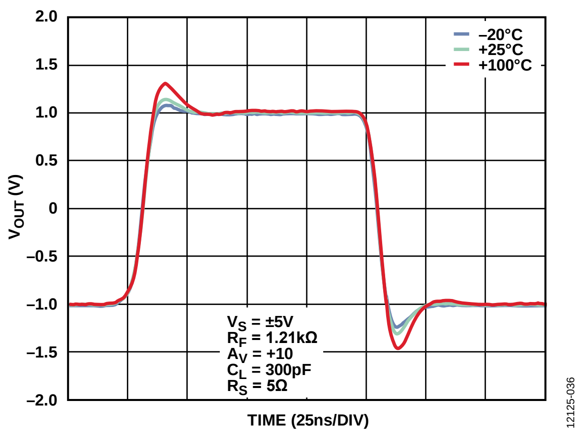


Figure 30. Small Signal Pulse Response vs. Case Temperature, A_V = +10, V_S = ±5 V, V_{OUT} = 2 V p-p, R_F = 1.21 kΩ, C_L = 300 pF, R_S = 5 Ω

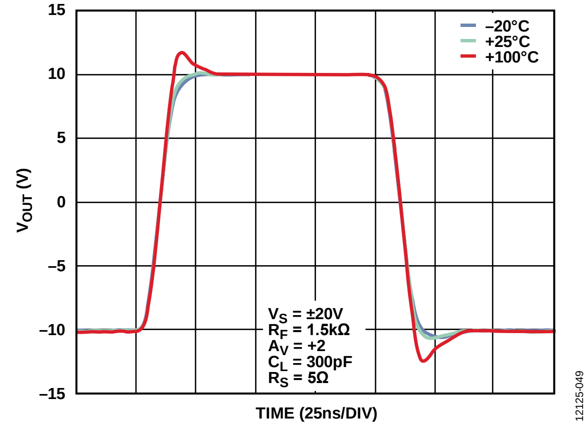


Figure 31. Large Signal Pulse Response vs. Case Temperature, A_V = +2, V_S = ±20 V, V_{OUT} = 20 V p-p, R_F = 1.5 kΩ, C_L = 300 pF, R_S = 5 Ω

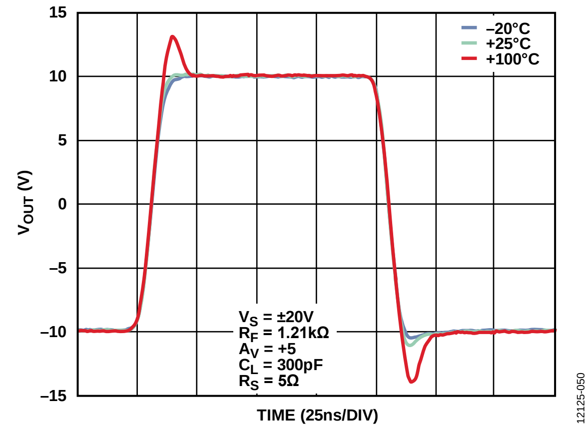


Figure 32. Large Signal Pulse Response vs. Case Temperature, A_V = +5, V_S = ±20 V, V_{OUT} = 20 V p-p, R_F = 1.21 kΩ, C_L = 300 pF, R_S = 5 Ω

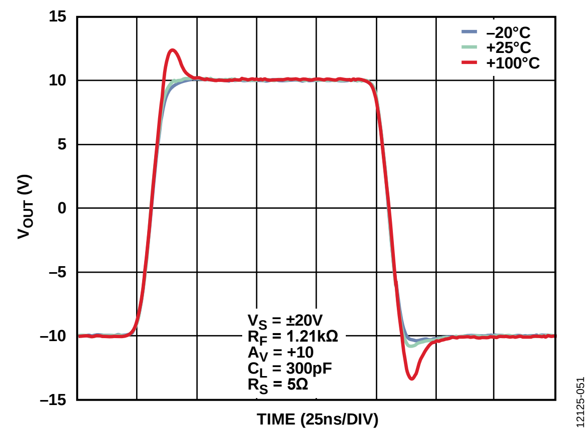


Figure 33. Large Signal Pulse Response vs. Case Temperature, A_V = +10, V_S = ±20 V, V_{OUT} = 20 V p-p, R_F = 1.21 kΩ, C_L = 300 pF, R_S = 5 Ω

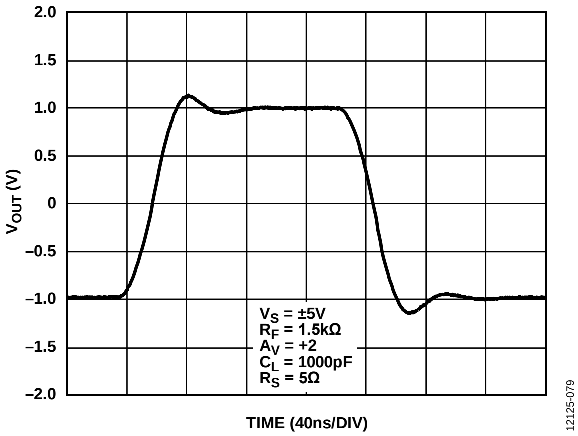


Figure 34. Small Signal Pulse Response, $A_V = +2$, $V_S = \pm 5$ V, $V_{OUT} = 2$ V p-p, $R_F = 1.5$ kΩ, $C_L = 1000$ pF, $R_S = 5$ Ω

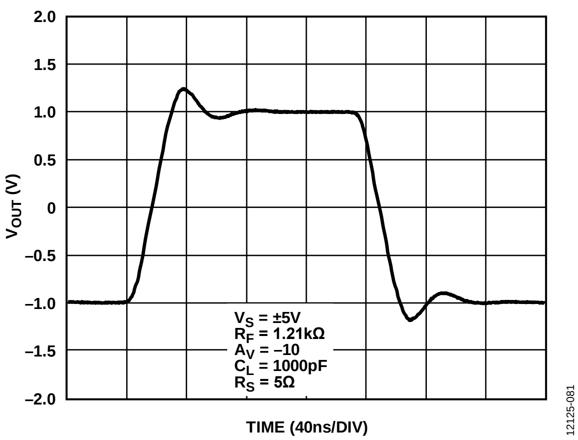


Figure 35. Small Signal Pulse Response, $A_V = -10$, $V_S = \pm 5$ V, $V_{OUT} = 2$ V p-p, $R_F = 1.21$ kΩ, $C_L = 1000$ pF, $R_S = 5$ Ω

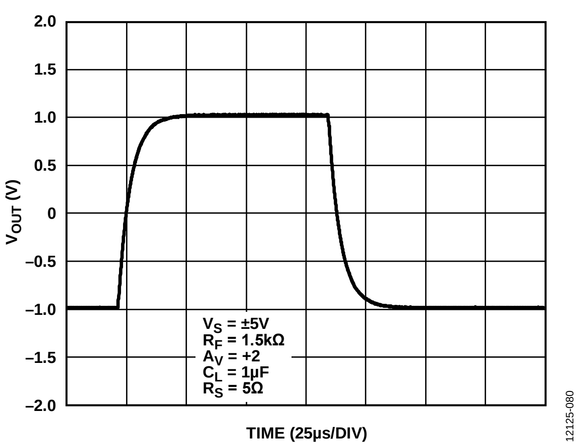


Figure 36. Small Signal Pulse Response, $A_V = +2$, $V_S = \pm 5$ V, $V_{OUT} = 2$ V p-p, $R_F = 1.5$ kΩ, $C_L = 1$ µF, $R_S = 5$ Ω

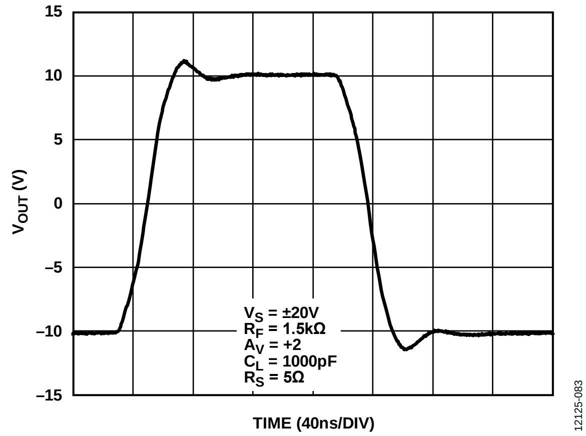


Figure 37. Large Signal Pulse Response, $A_V = +2$, $V_S = \pm 20$ V, $V_{OUT} = 20$ V p-p, $R_F = 1.5$ kΩ, $C_L = 1000$ pF, $R_S = 5$ Ω

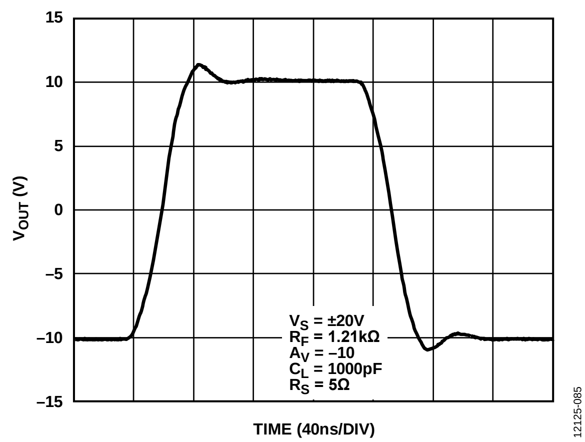


Figure 38. Large Signal Pulse Response, $A_V = -10$, $V_S = \pm 20$ V, $V_{OUT} = 20$ V p-p, $R_F = 1.21$ kΩ, $C_L = 1000$ pF, $R_S = 5$ Ω

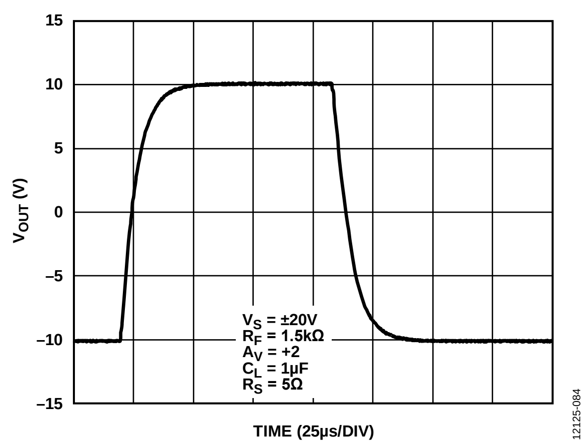


Figure 39. Large Signal Pulse Response, $A_V = +2$, $V_S = \pm 20$ V, $V_{OUT} = 20$ V p-p, $R_F = 1.5$ kΩ, $C_L = 1$ µF, $R_S = 5$ Ω

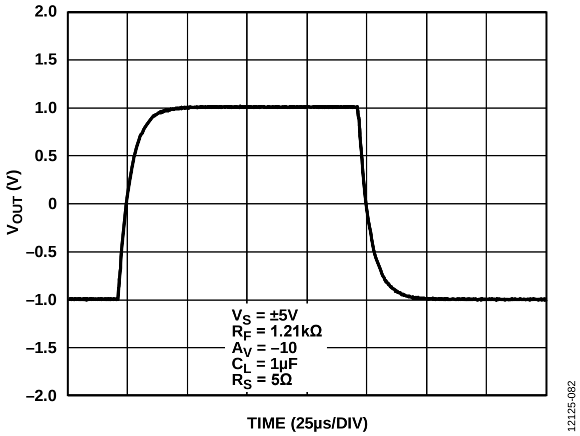


Figure 40. Small Signal Pulse Response, $A_V = -10$, $V_S = \pm 5$ V, $V_{OUT} = 2$ V p-p, $R_F = 1.21$ kΩ, $C_L = 1$ µF, $R_S = 5$ Ω

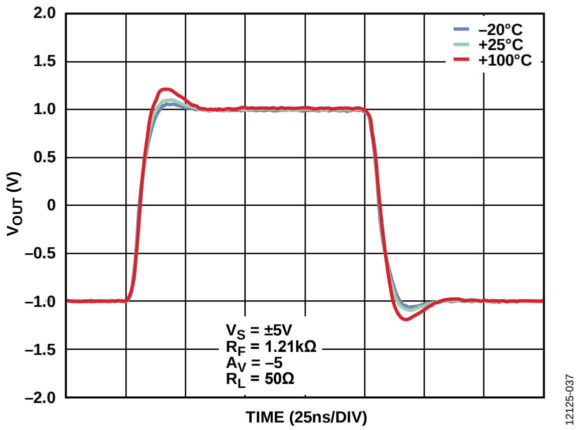


Figure 41. Small Signal Pulse Response vs. Case Temperature, $A_V = -5$, $V_S = \pm 5$ V, $V_{OUT} = 2$ V p-p, $R_F = 1.21$ kΩ, $R_L = 50$ Ω

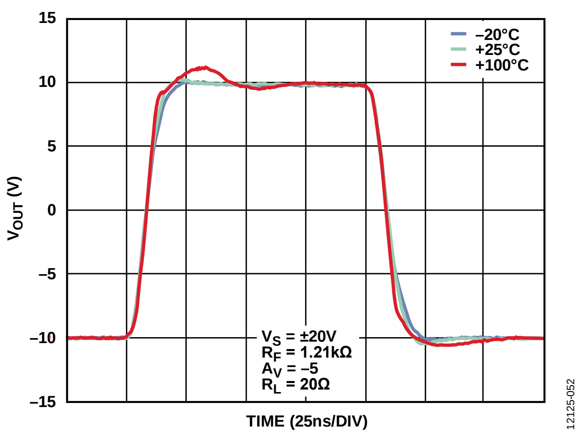


Figure 42. Large Signal Pulse Response vs. Case Temperature, $A_V = -5$, $V_S = \pm 20$ V, $V_{OUT} = 20$ V p-p, $R_F = 1.21$ kΩ, $R_L = 20$ Ω

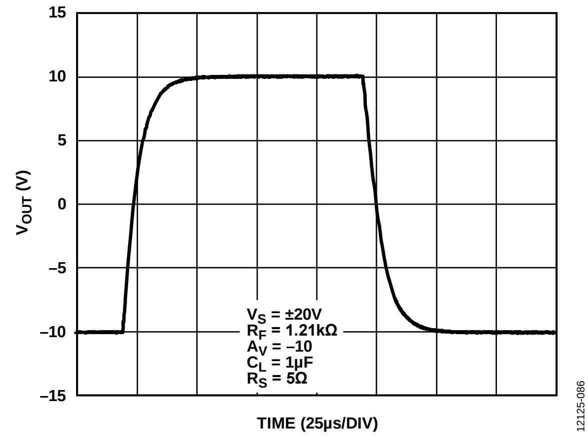


Figure 43. Large Signal Pulse Response, $A_V = -10$, $V_S = \pm 20$ V, $V_{OUT} = 20$ V p-p, $R_F = 1.21$ kΩ, $C_L = 1$ µF, $R_S = 5$ Ω

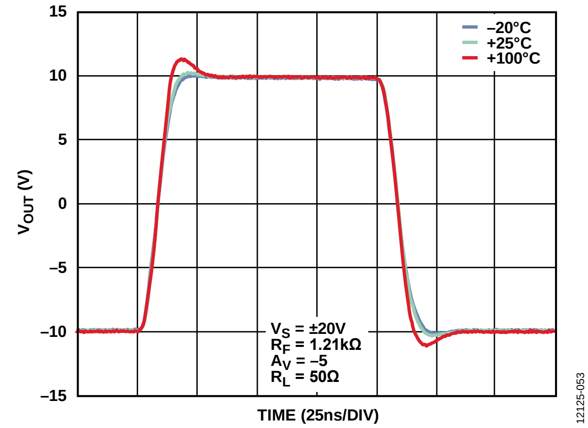


Figure 44. Large Signal Pulse Response vs. Case Temperature, $A_V = -5$, $V_S = \pm 20$ V, $V_{OUT} = 20$ V p-p, $R_F = 1.21$ kΩ, $R_L = 50$ Ω

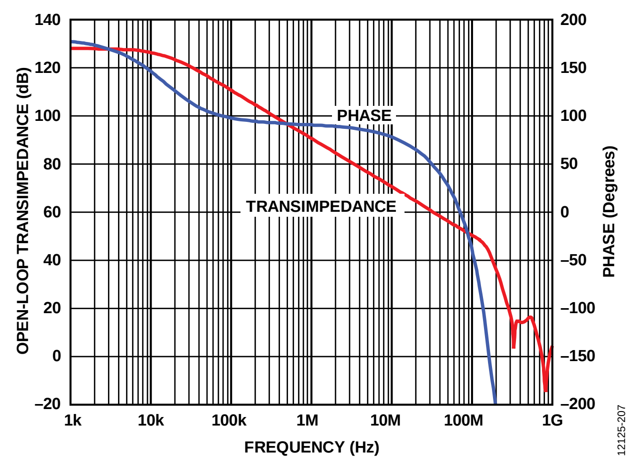


Figure 45. Open-Loop Transimpedance and Phase vs. Frequency

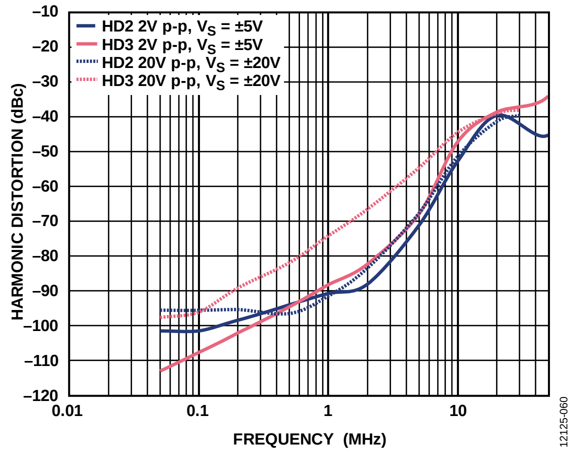


Figure 46. Harmonic Distortion vs. Frequency, C_L = 300 pF, R_S = 5 Ω, R_F = 1.21 kΩ, A_V = −10

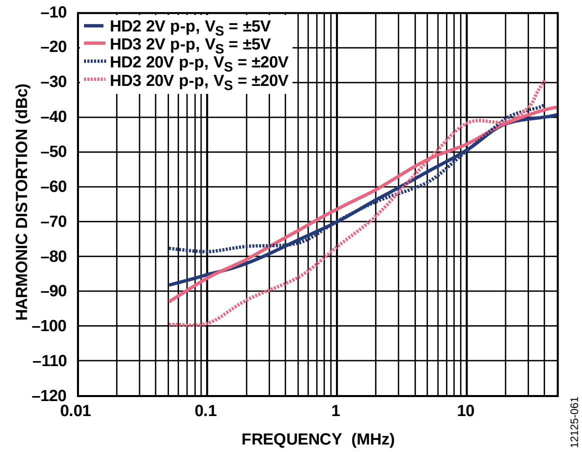


Figure 49. Harmonic Distortion vs. Frequency, R_L = 25 Ω, R_F = 1.21 kΩ, A_V = −10

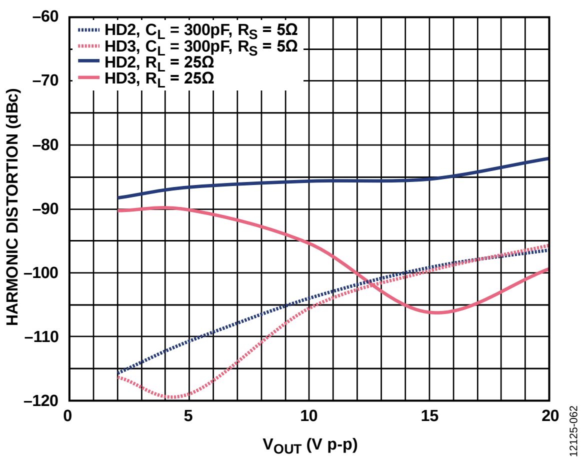


Figure 47. Harmonic Distortion vs. V_{OUT}, V_S = ±20 V, Frequency = 100 kHz, R_F = 1.21 kΩ, A_V = −10

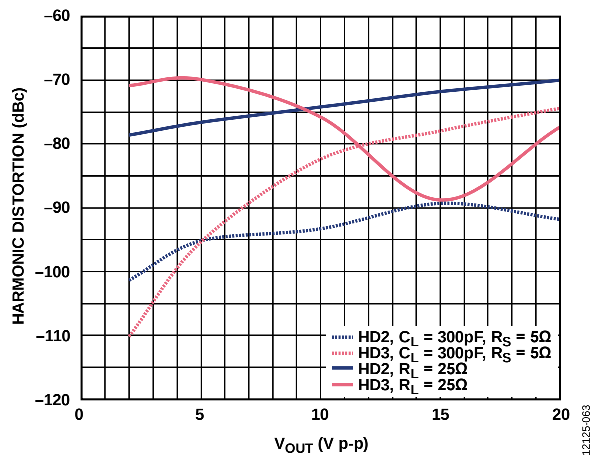


Figure 50. Harmonic Distortion vs. V_{OUT}, V_S = ±20 V, Frequency = 1 MHz, R_F = 1.21 kΩ, A_V = −10

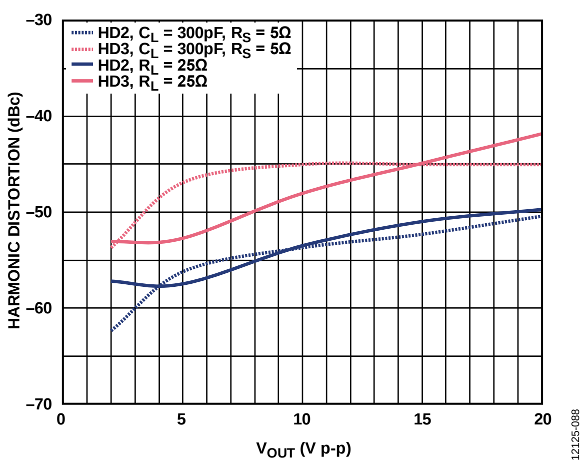


Figure 48. Harmonic Distortion vs. V_{OUT}, V_S = ±20 V, Frequency = 10 MHz, R_F = 1.21 kΩ, A_V = −10

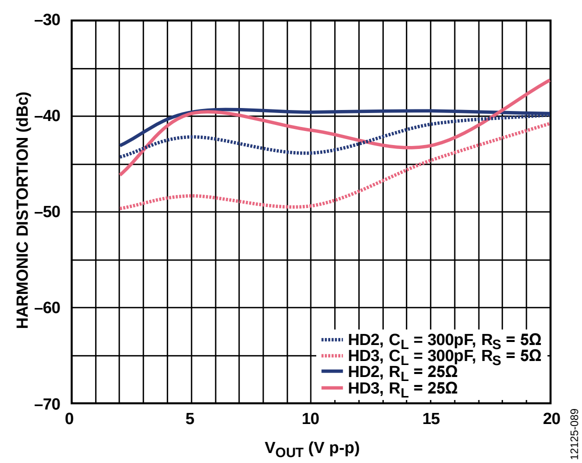


Figure 51. Harmonic Distortion vs. V_{OUT}, V_S = ±20 V, Frequency = 30 MHz, R_F = 1.21 kΩ, A_V = −10

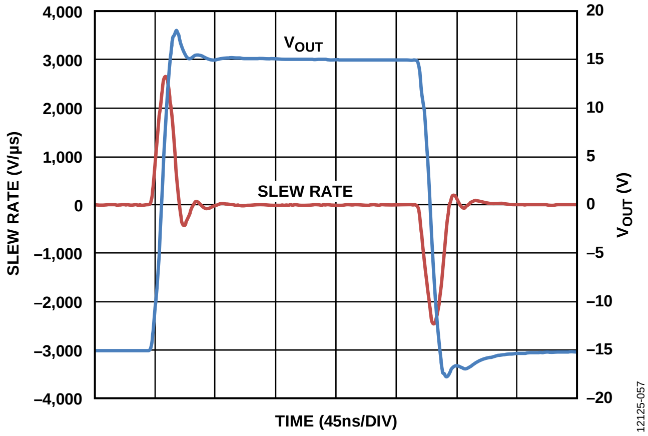


Figure 52. Large Signal Instantaneous Slew Rate, $A_V = +2$, $V_S = \pm20$ V, $R_F = 1.5$ kΩ, $C_L = 300$ pF, $R_S = 5$ Ω

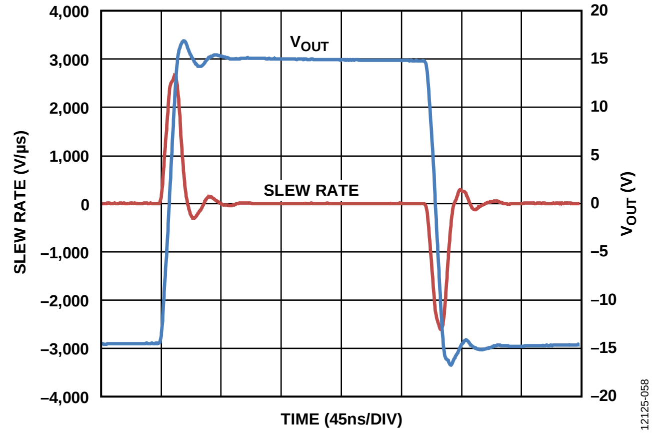


Figure 55. Large Signal Instantaneous Slew Rate, $A_V = +2$, $V_S = \pm20$ V, $R_F = 1.5$ kΩ, $R_L = 25$ Ω

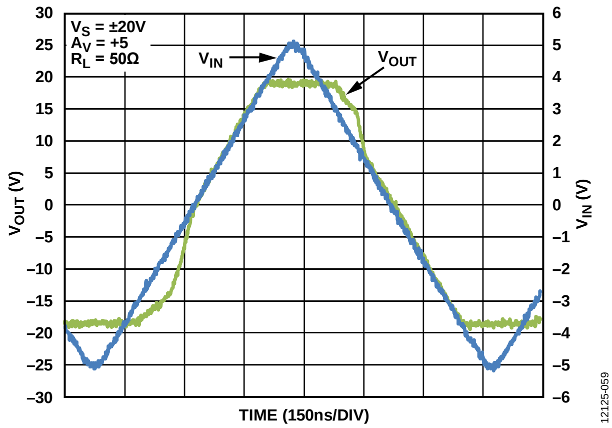


Figure 53. Output Overdrive Recovery, $V_S = \pm 20$ V, $A_V = +5$, $R_L = 50$ Ω

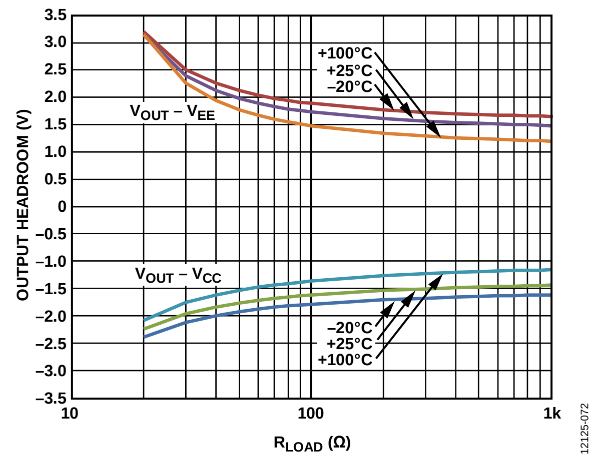


Figure 56. Output Headroom vs. R_{LOAD} Over Case Temperature, $V_S = \pm20$ V

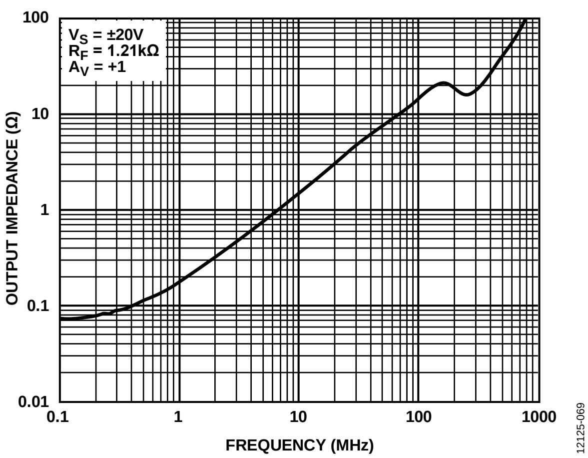


Figure 54. Enabled Closed-Loop Output Impedance vs. Frequency

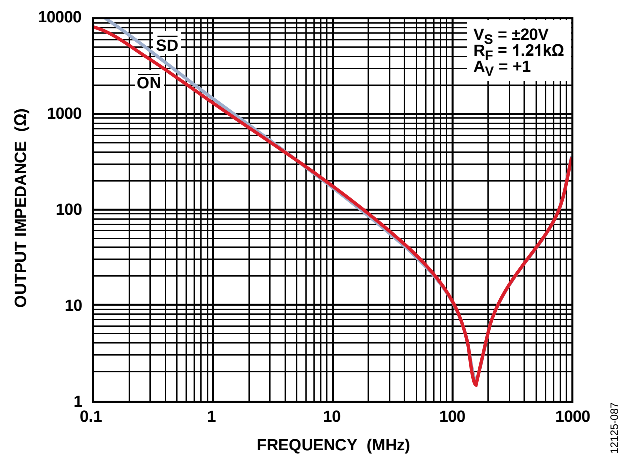


Figure 57. Disabled Closed-Loop Output Impedance vs. Frequency

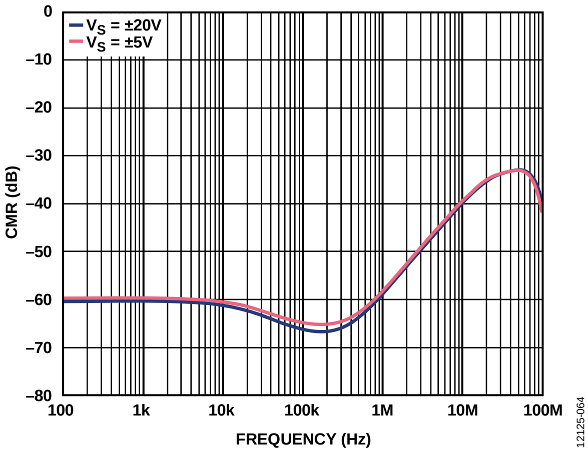


Figure 58. Common-Mode Rejection vs. Frequency

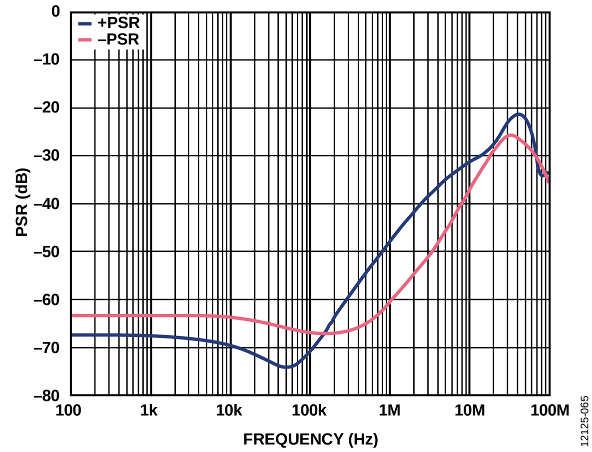


Figure 61. Power Supply Rejection (PSR) vs. Frequency, $V_S = \pm 20$ V

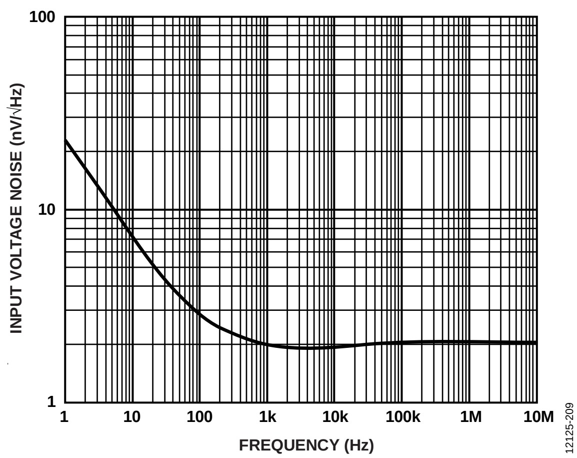


Figure 59. Input Voltage Noise vs. Frequency

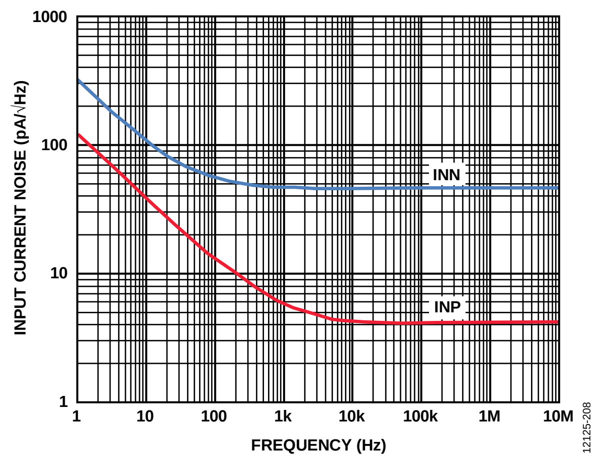


Figure 62. Input Current Noise vs. Frequency

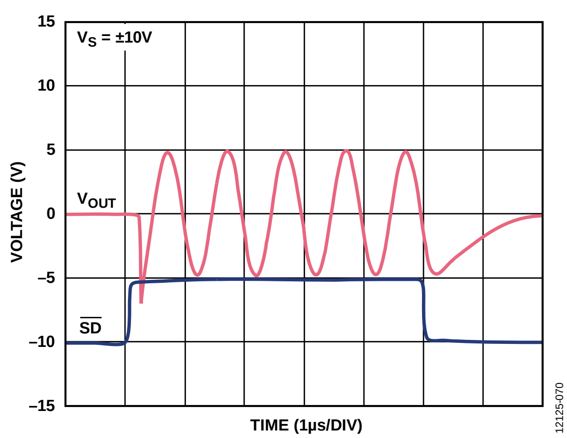


Figure 60. Turn-On/Turn-Off Time, $V_S = \pm 10$ V

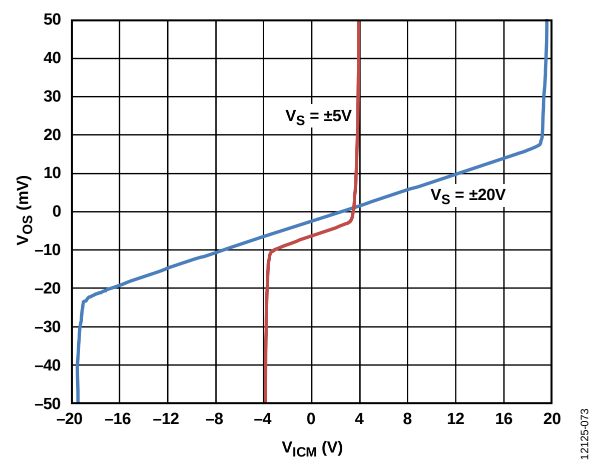


Figure 63. Input Common-Mode Voltage Range

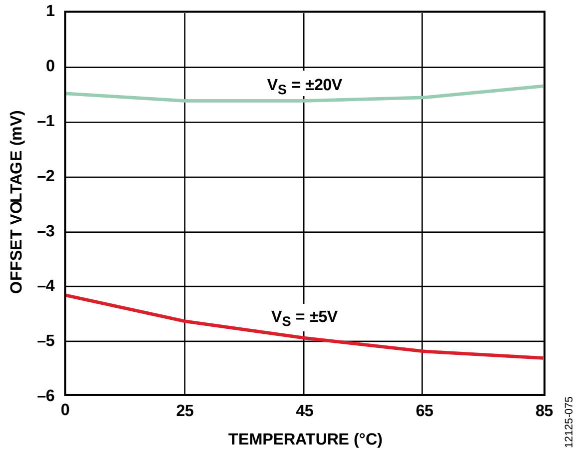


Figure 64. Input Offset Voltage vs. Temperature, V_S = ±5 V, V_S = ±20 V

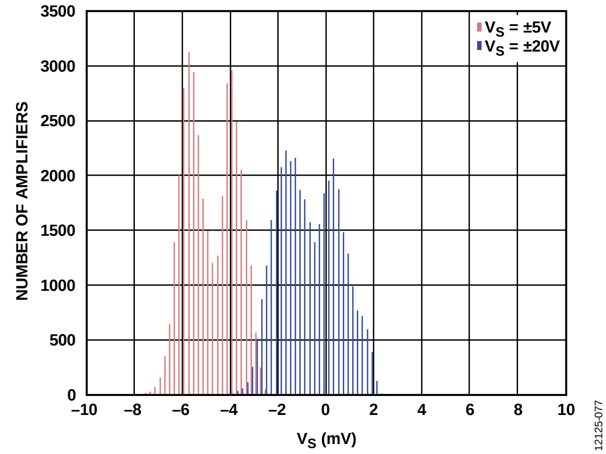


Figure 67. Input Offset Voltage Distribution, V_S = ±5 V, V_S = ±20 V

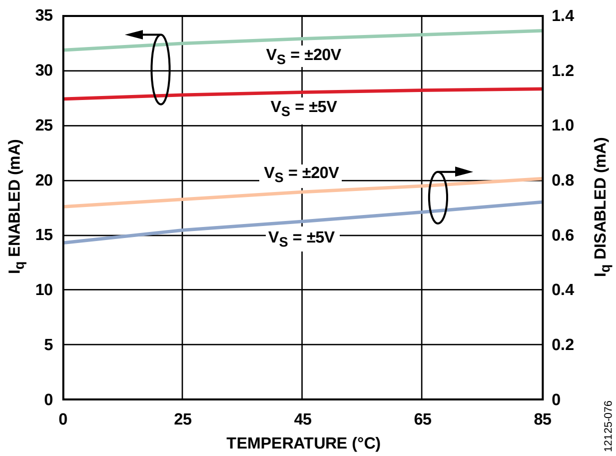


Figure 65. Quiescent Supply Current (I_q) vs. Temperature, V_S = ±5 V, V_S = ±20 V (Enabled/Disabled via SD)

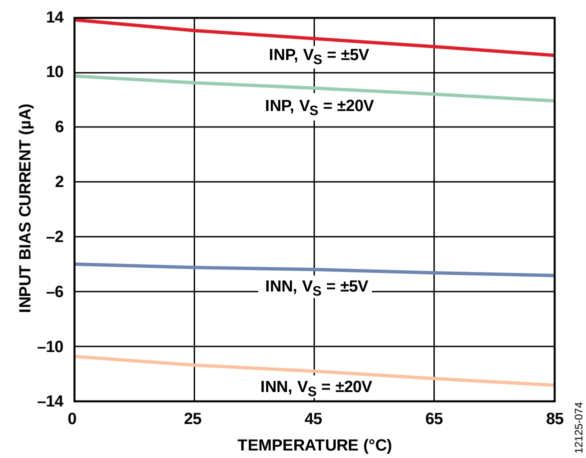


Figure 68. Input Bias Current vs. Temperature, V_S = ±5 V, V_S = ±20 V

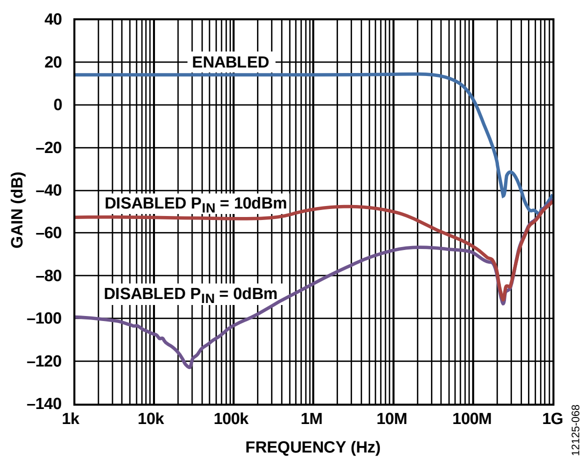


Figure 66. Forward Isolation vs. Frequency for 0 dBm and 10 dBm Input Levels (Disabled via SD or ON)

APPLICATIONS INFORMATION

$\overline{\text{ON}}$, INITIAL POWER-UP, AND SHORT-CIRCUIT

After initial power-up, the $\overline{\text{ON}}$ pin must be pulled low to ensure that the amplifier is turned on. Subsequently, floating the $\overline{\text{ON}}$ pin enables the short-circuit protection feature while the amplifier remains on. While $\overline{\text{ON}}$ is held low, the short-circuit protection feature is disabled.

When a short-circuit condition is detected, the amplifier is disabled, the supply current drops to about 5 mA, and the TFL pin outputs a dc voltage of ~300 mV. To turn the amplifier back on after a short-circuit event, follow the sequence for initial power-up.

Pulling the $\overline{\text{ON}}$ pin high disables the amplifier and causes the supply current to drop to about 5 mA, as if a short-circuit condition had been detected.

The impedance at the $\overline{\text{ON}}$ pin is ~20 kΩ. Lay out the PCB trace leading to $\overline{\text{ON}}$ to avoid noise coupling into it and triggering a false event. A 1 nF capacitor between $\overline{\text{ON}}$ and V_{EE} is recommended to help shunt noise away from $\overline{\text{ON}}$.

THERMAL PROTECTION

In addition to short-circuit protection, the ADA4870 is also protected against excessive die temperatures.

During normal operation, the TFL pin outputs a dc voltage (referenced to V_{EE}) ranging from 1.5 V to 1.9 V that is relative to die temperature. The voltage on TFL changes at approximately −3 mV/°C and can be used to indicate approximate increases in die temperature. When excessive die temperatures are detected, the amplifier switches to an off state, dropping the supply current to approximately 5 mA, and TFL continues to report a voltage relative to die temperature. When the die temperature returns to an acceptable level, the amplifier automatically resumes normal operation.

SHUTDOWN ($\overline{\text{SD}}$)

The ADA4870 is equipped with a power saving shutdown feature. Pulling $\overline{\text{SD}}$ low places the amplifier in a shutdown state, reducing quiescent current to approximately 750 µA. When turning the amplifier back on from the shutdown state, pull the $\overline{\text{SD}}$ pin high and then pull the $\overline{\text{ON}}$ pin low. Following this sequence ensures power-on. Afterwards, the $\overline{\text{ON}}$ pin can be floated to enable short-circuit protection.

Pull $\overline{\text{SD}}$ high or low; do not leave $\overline{\text{SD}}$ floating.

FEEDBACK RESISTOR SELECTION

The feedback resistor value has a direct impact on the stability and closed-loop bandwidth of current feedback amplifiers. Table 6 provides a guideline for the selection of feedback resistors for some common gain configurations.

Table 6. Recommended R_F Values

Closed-Loop Gain (V/V)	R_F (Ω)	R_G (Ω)	C_L (pF)	R_S (Ω)
+1	2000	Open	300	5
−1	1210	1210	300	5
+2	1500	1500	300	5
−2	1210	604	300	5
+5	1210	301	300	5
+10	1210	133	300	5

CAPACITIVE LOAD DRIVING

When driving a capacitive load (C_L), the amplifier output resistance and the load capacitance form a pole in the transfer function of the amplifier. This additional pole reduces phase margin at higher frequencies and, if left uncompensated, can result in excessive peaking and instability. Placing a small series resistor (R_S) between the amplifier output and C_L (as shown in Figure 69) allows the ADA4870 to drive capacitive loads beyond 1 µF. Figure 70 shows the series resistor value vs. capacitive load for a maximum of 1 dB peaking in the circuit of Figure 69. For large capacitive loads, R_S values of less than 0.3 Ω are not recommended.

Figure 71 shows the small signal bandwidth (SSBW) vs. C_L with corresponding R_S values from Figure 70.

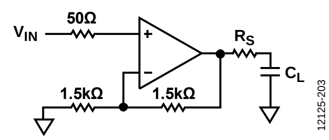


Figure 69. Circuit for Capacitive Load Drive

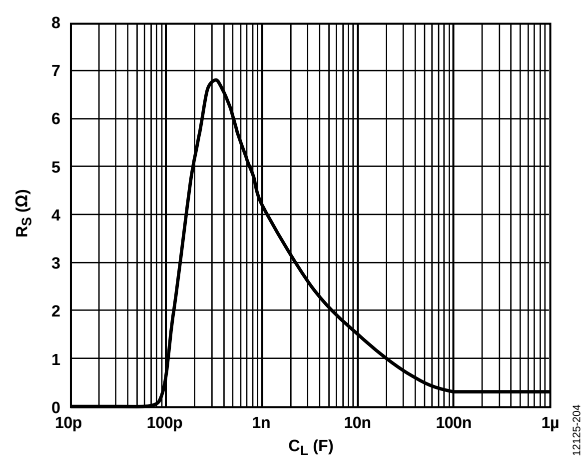


Figure 70. R_S vs. C_L for Maximum 1 dB Peaking for Circuit from Figure 69

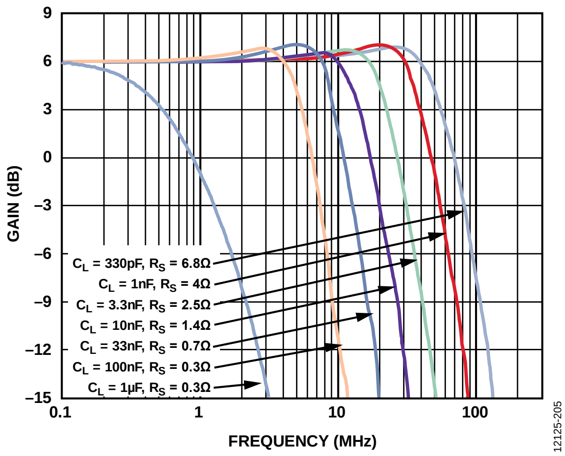


Figure 71. Small Signal Bandwidth for Various C_L and R_S Values from Figure 70

HEAT AND THERMAL MANAGEMENT

High output current amplifiers like the ADA4870 generate heat, instantaneous or continuous, depending on the signal being processed. Properly applied thermal management techniques move heat away from the ADA4870 die and help to maintain acceptable junction temperatures (T_J). A highly conductive thermal path from the slug of the PSOP_3 package to the ambient air is required to obtain the best performance at the lowest T_J.

POWER DISSIPATION

The first step in identifying a thermal solution is to compute the power generated in the amplifier during normal operation. The schematic in Figure 72 shows a simplified output stage of the ADA4870. The most significant heat is generated by the output stage push-pull pair, particularly when driving heavy loads.

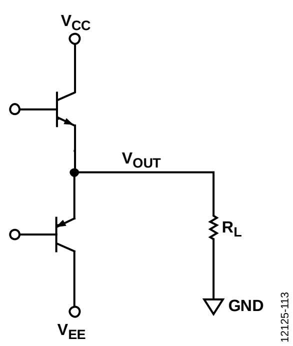


Figure 72. Simplified Output Stage

The total power dissipation in the amplifier is the sum of the power dissipated in the output stage plus the quiescent power. The average power for an amplifier processing sine signals is computed by Equation 1. Equation 2 can be used to compute the peak power of a sine wave and can be used to compute the continuous power dissipation of dc output voltages where V_{PEAK} is the dc load voltage. These equations assume symmetrical supplies and a load referred to midsupply.

$$P_{AVG,\,SINE} = (V_S \times I_q) + \left(\frac{2}{\pi} \times \frac{V_{CC} V_{PEAK}}{R_L}\right) - \left(\frac{V_{PEAK}^{\ 2}}{2R_L}\right) \quad (1)$$

$$P_{PEAK} = (V_S \times I_q) + (V_S - V_{PEAK}) \times \left(\frac{V_{PEAK}}{R_L}\right) \quad (2)$$

where
V_S is the total supply voltage ($V_{CC} - V_{EE}$).
I_q is the amplifier quiescent current.

A graphical representation of the $P_{AVG,\,SINE}$ and P_{PEAK} power equations is shown in Figure 73. The power curves were generated for the ADA4870 operating from ±20 V supplies and driving a 20 Ω load. The quiescent power intersects the vertical axis at ~1.3 W when V_{OUT} is at 0 V or midsupply. The graphs stop at the output swing limit of 18 V.

For dc analysis, peak power dissipation occurs at $V_{OUT} = V_{CC}/2$, while the maximum average power for sine wave signals occurs at $V_{OUT} = 2V_{CC}/\pi$.

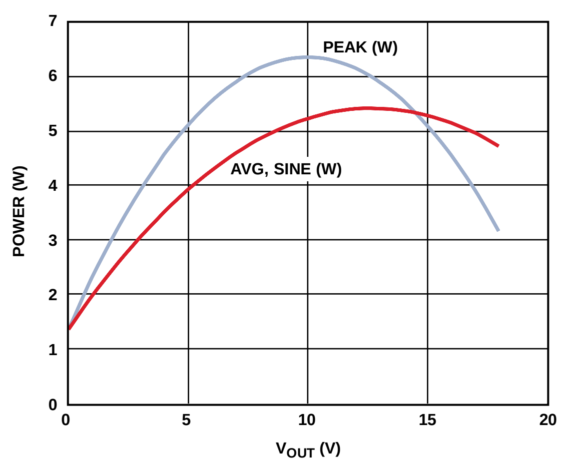


Figure 73. Average Sine and Peak Power vs. V_{OUT}, V_S = ±20 V, R_L = 20 Ω

SAFE OPERATING AREA

The safe operating area (SOA) is a curve of output current vs. output stage collector-emitter voltage (V_{CE}), under which the amplifier can operate at a safe junction temperature (T_J). The area under the curves of Figure 74 shows the operational boundaries of the ADA4870 for the PCB of Figure 75 that maintains a $T_J \leq 150°C$. The SOA curves of Figure 74 are unique to the conditions under which they were developed, such as PCB, heat sink, and ambient temperature.

Two heat sinks (VHS-45 and VHS-95) were used in the evaluation. Both were assembled to the PCB using CT40-5 thermal interface material.

All testing was done in a still-air environment. Forced air convection in any of the test cases effectively lowers θ_{JA} and moves the corresponding curve toward the upper right, expanding the SOA. For more information on the ADA4870 evaluation board, see the ADA4870 User Guide.

In Figure 74, the horizontal line at 1 A is the output current drive of the ADA4870. The curved section maintains a fixed power dissipation that results in a junction temperature (T_J) of 150°C or less. Note that the x-axis is the output stage V_{CE} (V_{CC} – V_{OUT} or V_{OUT} – V_{EE}) developed across the relevant output transistor of Figure 72 and ends at a maximum V_{CE} of 20 V.

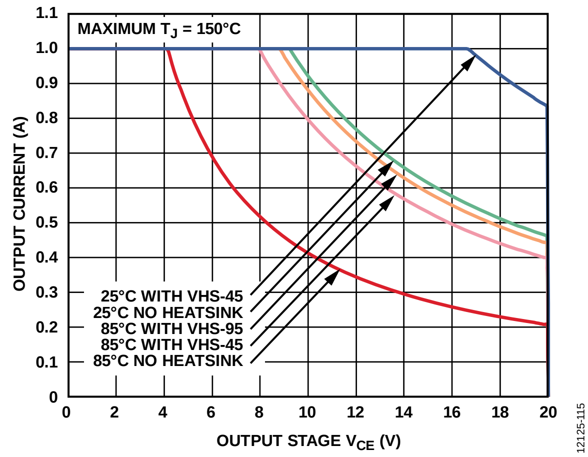


Figure 74. Safe Operating Area for Evaluation Board from Figure 75 at 25°C and 85°C Ambient Temperature With and Without Heat Sink, No Air Flow

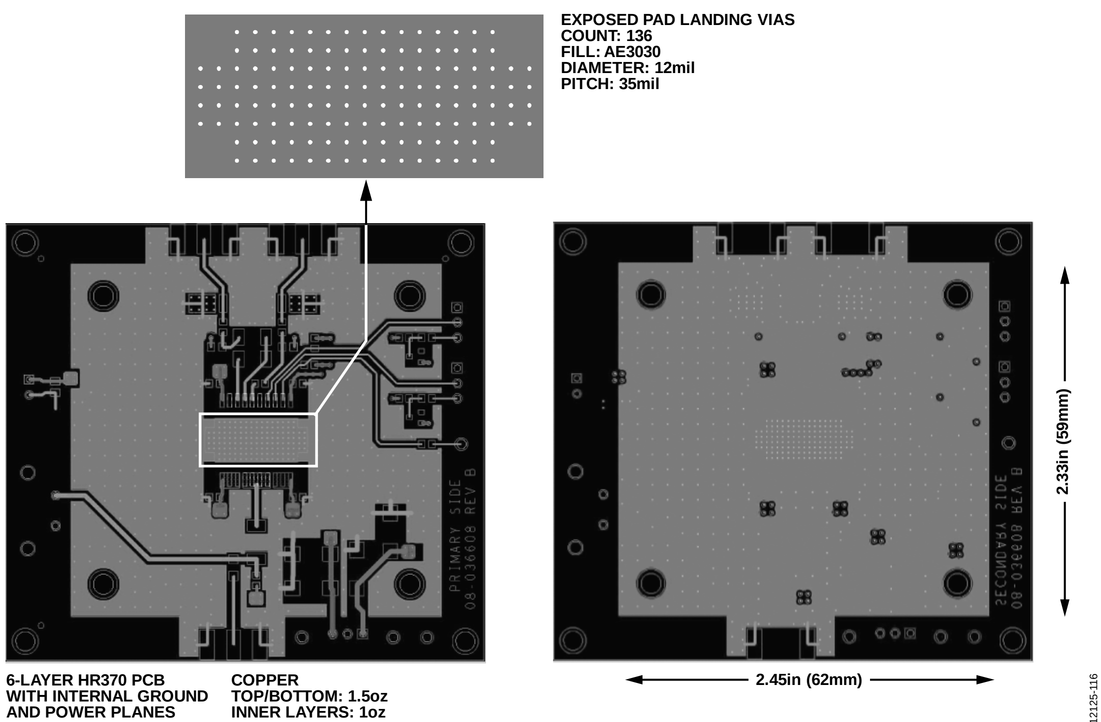


Figure 75. Details of the ADA4870 Evaluation Board

PRINTED CIRCUIT BOARD (PCB)

All current feedback amplifiers, including the ADA4870, can be affected by stray capacitance. Paying careful attention during PCB layout can reduce parasitic capacitance and improve overall circuit performance. Minimize signal trace lengths by placing feedback and gain setting resistors as close as possible to the amplifier.

Additionally, for high output current amplifiers like the ADA4870, lay out the PCB with heat dissipation in mind. A good thermal design includes an exposed copper landing area on the top side of the board on which to solder the thermal slug of the PSOP3 package. The PCB should also provide an exposed copper area on the bottom side to accommodate a heat sink. Stitch the top and bottom layers together with an array of plated-through thermal vias to facilitate efficient heat transfer through the board. Thermal conductivity may be further improved by using widely available via fill materials.

THERMAL MODELING

Computational fluid dynamics (CFD) tools like FloTherm® can be used to create layers of materials that include PCB construction, thermal vias, thermal interface materials, and heat sinks, and can predict junction temperature and/or junction to ambient thermal resistance (θ_{JA}) for a given set of conditions. Table 7 shows an example of how θ_{JA} is affected by the addition of an aluminum heat sink and forced convection. Figure 76 shows an image of the model used to establish the thermal results in Table 7.

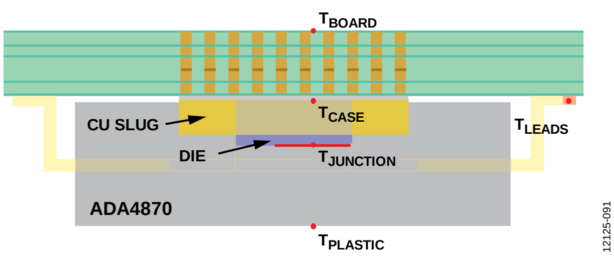


Figure 76. Thermal Model Stack-Up for Data in Table 7 (Heat Sink Not Shown)

HEAT SINK SELECTION

A heat sink increases the surface area to ambient temperature (T_A) and extends the power dissipation capability of the ADA4870 and PCB combination. To maximize heat transfer from the board to the heat sink, attach the heat sink to the PCB using a high conductivity thermal interface material (TIM). The heat sinks presented in the Safe Operating Area section and Figure 74 are effective up to ~10 W in still air. If lower power dissipation is anticipated and/or forced air convection is used, a smaller heat sink may be appropriate. If the thermal resistance of the chip (θ_{JC}), PCB (θ_{CB}), and TIM (θ_{TIM}) are known, use Equation 3 to compute the thermal resistance (θ_{HS}) of the required heat sink.

$$\theta_{HS} = \left(\frac{T_J - T_A}{P_{DISS}}\right) - (\theta_{JC} + \theta_{CB} + \theta_{TIM}) \quad (3)$$

POWER SUPPLIES AND DECOUPLING

The ADA4870 can operate from a single supply or dual supplies. The total supply voltage ($V_{CC} - V_{EE}$) must be between 10 V and 40 V. Decouple each supply pin to ground using high quality, low ESR, 0.1 µF capacitors. Place decoupling capacitors as close to the supply pins as possible. Additionally, place 22 µF tantalum capacitors from each supply to ground to provide good low frequency decoupling and supply the needed current to support large, fast slewing signals at the ADA4870 output.

Table 7. Effects of Heat Sink and Forced Convection on θ_{JA}

Heat Sink Dimensions, L × W × Total Height (mm)	Heat Sink Base Thickness (mm)	No. of Fins	Air Flow (m/sec)	θ_{JA} (°C/W)
61 × 58, Exposed Copper on Board, No Heat Sink	Not applicable	Not applicable	0	15.95
61 × 58, Exposed Copper on Board, No Heat Sink	Not applicable	Not applicable	1	12.27
61 × 58, Exposed Copper on Board, No Heat Sink	Not applicable	Not applicable	2	10.95
30 × 30 × 24	3	10	0	11.36
30 × 30 × 24	3	10	1	4.90
30 × 30 × 24	3	10	2	3.86
61 × 58 × 24	3	10	0	5.74
61 × 58 × 24	3	10	1	3.59
61 × 58 × 24	3	10	2	3.18

COMPOSITE AMPLIFIER

When dc precision and high output current are required, the ADA4870 can be combined with a precision amplifier such as the ADA4637-1 to form a composite amplifier as shown in Figure 77.

By placing the ADA4870 inside the feedback loop of the ADA4637-1, the composite amplifier provides the high output current of the ADA4870 while preserving the dc precision of the ADA4637-1.

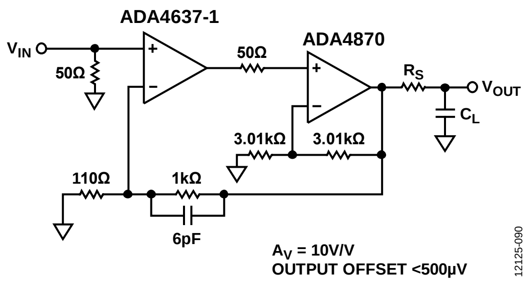


Figure 77. Composite Amplifier

Figure 78 shows the bandwidth of the composite amplifier at a gain of 10. The offset voltage at the output is <500 µV.

The circuit can be tailored for different gains as desired. Depending on the board parasitics, the 6 pF capacitor may need to be empirically adjusted to optimize performance. Minimize PCB stray capacitance as much as possible, particularly in the feedback path.

The small signal and large signal pulse response is shown in Figure 79 and Figure 80, respectively.

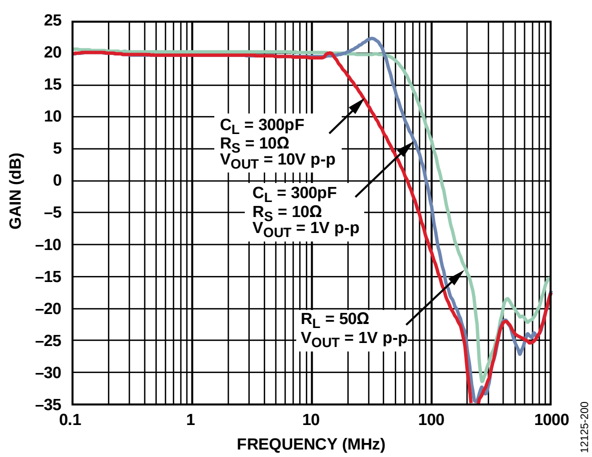


Figure 78. Composite Amplifier Frequency Response

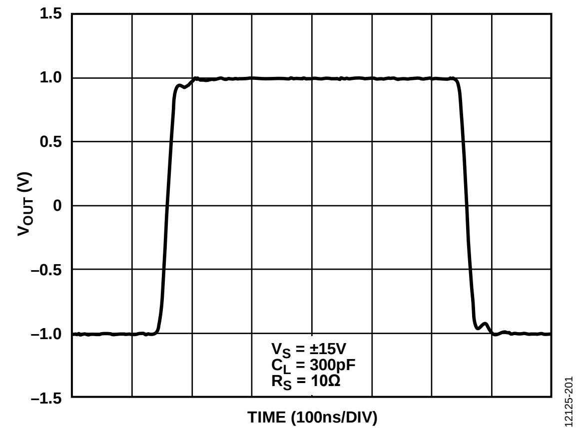


Figure 79. Composite Amplifier Small Signal Pulse Response

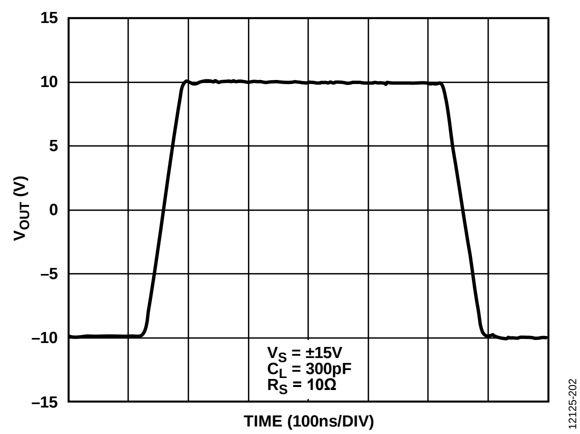
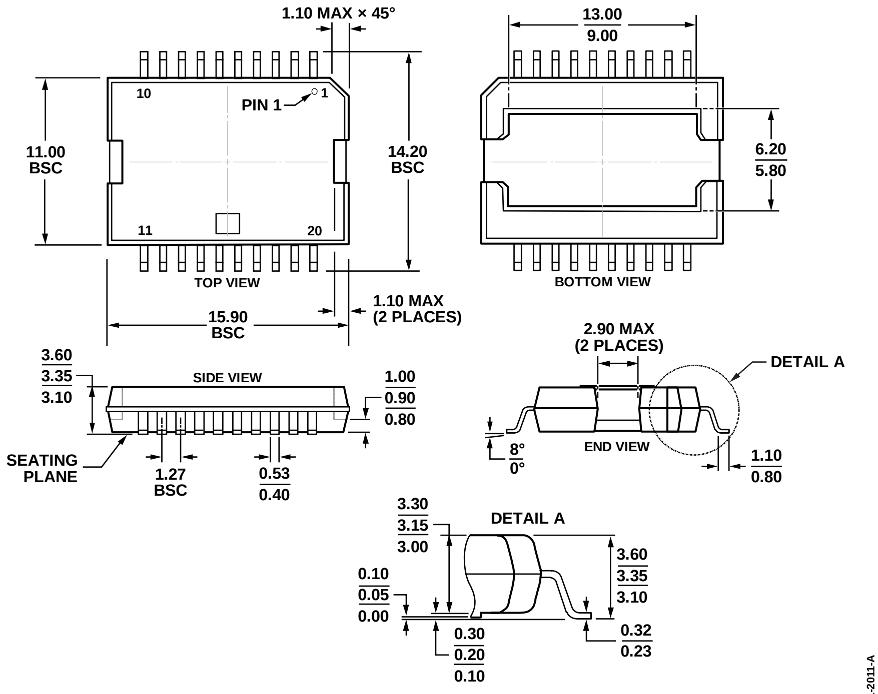


Figure 80. Composite Amplifier Large Signal Pulse Response

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-166-AA

Figure 81. 20-Lead Power SOIC, Thermally Enhanced Package [PSOP_3] (RR-20-1) Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADA4870ARRZ	−40°C to +85°C	20-Lead PSOP_3	RR-20-1
ADA4870ARRZ-RL	−40°C to +85°C	20-Lead PSOP_3	RR-20-1
ADA4870ARR-EBZ		Evaluation Board	

[1] Z = RoHs Compliant Part.