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October 2014

# FDMS86252L

## N-Channel Shielded Gate PowerTrench<sup>®</sup> MOSFET

150 V, 12 A, 56 mΩ

### Features

- Shielded Gate MOSFET Technology
- Max  $r_{DS(on)}$  = 56 mΩ at  $V_{GS} = 10$  V,  $I_D = 4.4$  A
- Max  $r_{DS(on)}$  = 71 mΩ at  $V_{GS} = 6$  V,  $I_D = 3.8$  A
- Max  $r_{DS(on)}$  = 75 mΩ at  $V_{GS} = 4.5$  V,  $I_D = 3.7$  A
- Advanced package and silicon combination for low  $r_{DS(on)}$  and high efficiency
- Next generation enhanced body diode technology, engineered for soft recovery
- MSL1 robust package design
- 100% UIL tested
- RoHS Compliant

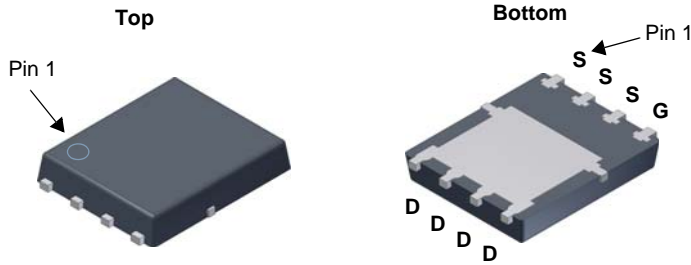


### General Description

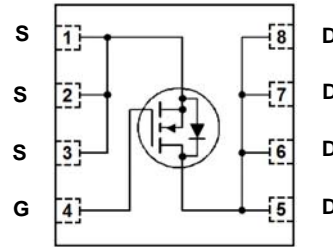
This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench<sup>®</sup> process that incorporates Shielded Gate technology. This process has been optimized for the on-state resistance and yet maintain superior switching performance.

### Applications

- OringFET / Load Switching
- Synchronous Rectification
- DC-DC Conversion



Power 56



### MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	150	V
$V_{GS}$	Gate to Source Voltage	±20	V
$I_D$	Drain Current -Continuous $T_C = 25$ °C	12	A
	-Continuous $T_A = 25$ °C (Note 1a)	4.4	
	-Pulsed (Note 4)	30	
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	73	mJ
$P_D$	Power Dissipation $T_C = 25$ °C	50	W
	Power Dissipation $T_A = 25$ °C (Note 1a)	2.5	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	2.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS86252L	FDMS86252L	Power 56	13 "	12 mm	3000 units

FDMS86252L N-Channel Shielded Gate PowerTrench<sup>®</sup> MOSFET

## Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}, V_{GS} = 0\text{ V}$	150			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		104		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 120\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$			$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	1	1.5	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-6		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 4.4\text{ A}$		46	56	m $\Omega$
		$V_{GS} = 6\text{ V}, I_D = 3.8\text{ A}$		48	71	
		$V_{GS} = 4.5\text{ V}, I_D = 3.7\text{ A}$		52	75	
		$V_{GS} = 10\text{ V}, I_D = 4.4\text{ A}, T_J = 125\text{ }^\circ\text{C}$		90	110	
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 4.4\text{ A}$		21		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 75\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		952	1335	pF
$C_{oss}$	Output Capacitance			74	105	pF
$C_{rss}$	Reverse Transfer Capacitance			3	5	pF
$R_g$	Gate Resistance		0.1	0.6	1.8	$\Omega$

### Switching Characteristics

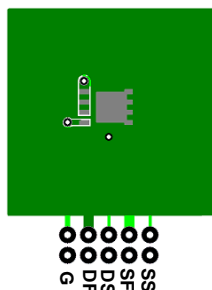
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 75\text{ V}, I_D = 4.4\text{ A}, V_{GS} = 10\text{ V}, R_{GEN} = 6\text{ }\Omega$		6.8	14	ns
$t_r$	Rise Time			1.4	10	ns
$t_{d(off)}$	Turn-Off Delay Time			19	34	ns
$t_f$	Fall Time			2.9	10	ns
$Q_g$	Total Gate Charge	$V_{GS} = 0\text{ V to } 10\text{ V}$		15	21	nC
$Q_g$	Total Gate Charge	$V_{GS} = 0\text{ V to } 4.5\text{ V}$	$V_{DD} = 75\text{ V}, I_D = 4.4\text{ A}$	7.6	11	nC
$Q_{gs}$	Gate to Source Charge			2.1		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			2.3		nC

### Drain-Source Diode Characteristics

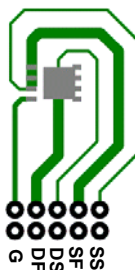
$V_{SD}$	Source-Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 1.9\text{ A}$ (Note 2)		0.7	1.2	V
		$V_{GS} = 0\text{ V}, I_S = 4.4\text{ A}$ (Note 2)		0.8	1.3	
$t_{rr}$	Reverse Recovery Time	$I_F = 4.4\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		53	85	ns
$Q_{rr}$	Reverse Recovery Charge			51	82	nC

#### Notes:

1.  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a. 50  $^\circ\text{C}/\text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



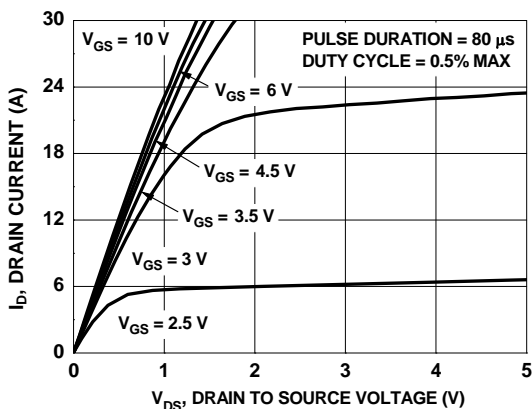
b. 125  $^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0%.

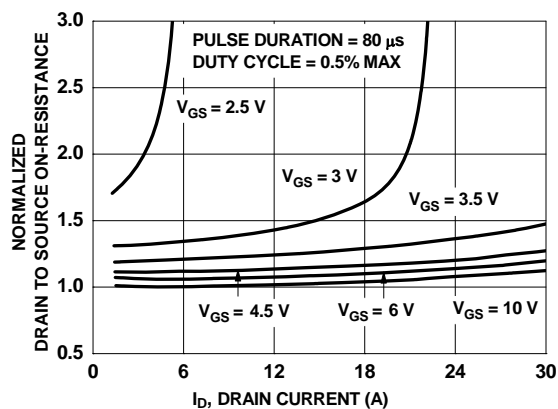
3.  $E_{AS}$  of 73 mJ is based on Starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 3\text{ mH}$ ,  $I_{AS} = 7\text{ A}$ ,  $V_{DD} = 150\text{ V}$ ,  $V_{GS} = 10\text{ V}$ . 100% tested at  $L = 0.1\text{ mH}$ ,  $I_{AS} = 24\text{ A}$ .

4. Pulsed  $I_d$  limited by junction temperature,  $t_d \leq 100\text{ }\mu\text{s}$ , please refer to SOA curve for more details.

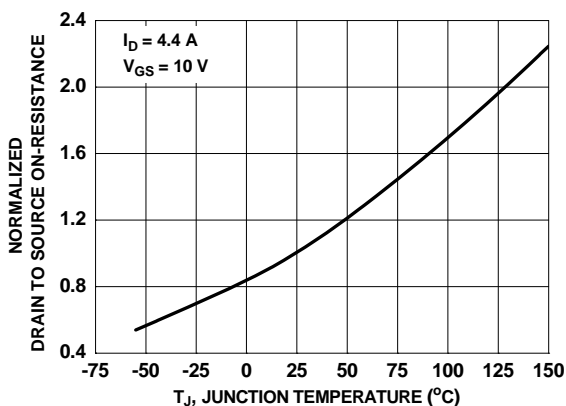
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



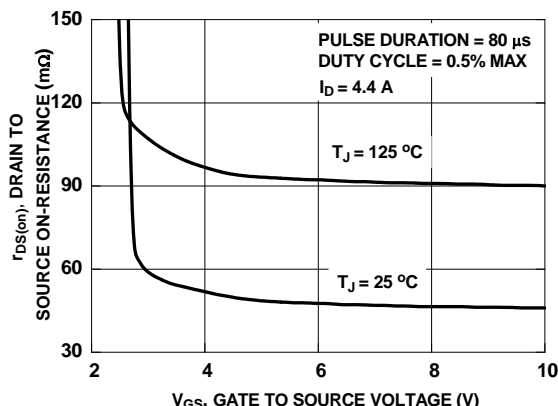
**Figure 1. On Region Characteristics**



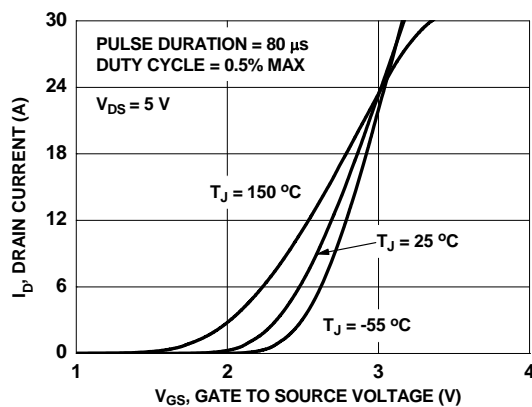
**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**



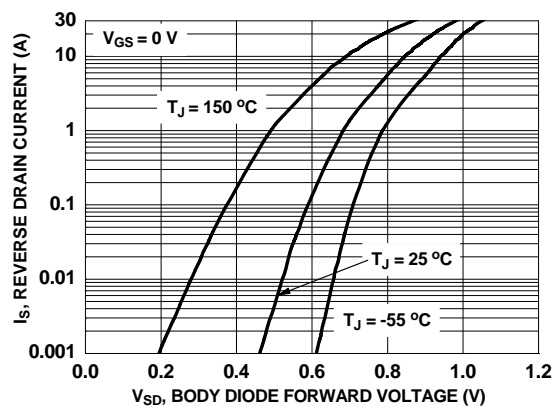
**Figure 3. Normalized On Resistance vs Junction Temperature**



**Figure 4. On-Resistance vs Gate to Source Voltage**

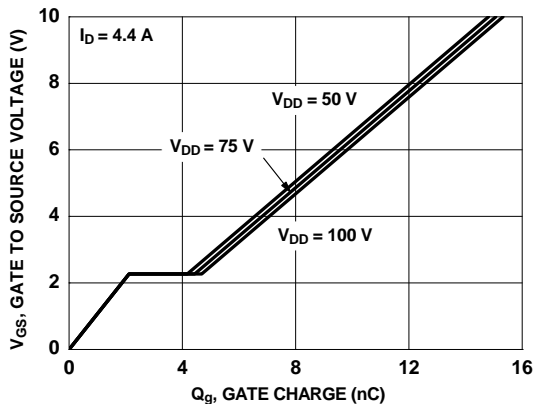


**Figure 5. Transfer Characteristics**

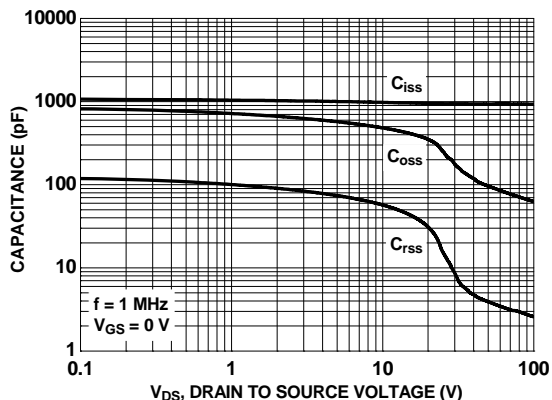


**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

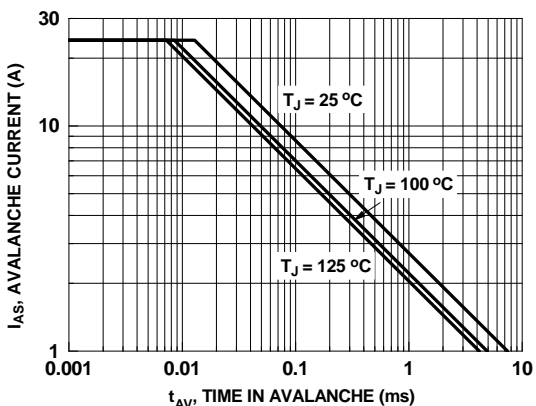
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



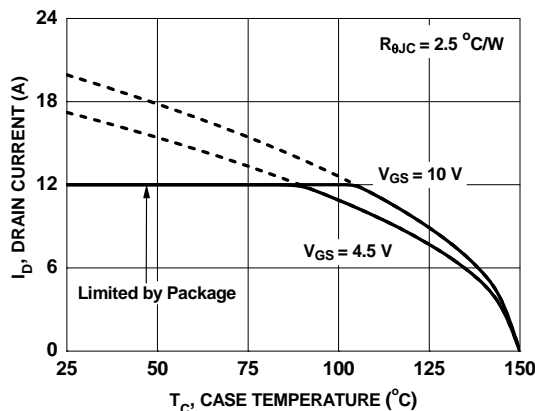
**Figure 7. Gate Charge Characteristics**



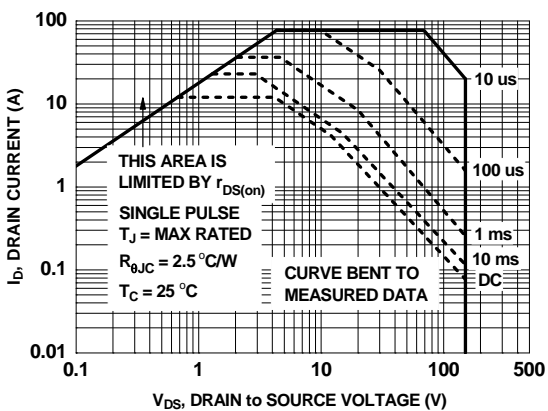
**Figure 8. Capacitance vs Drain to Source Voltage**



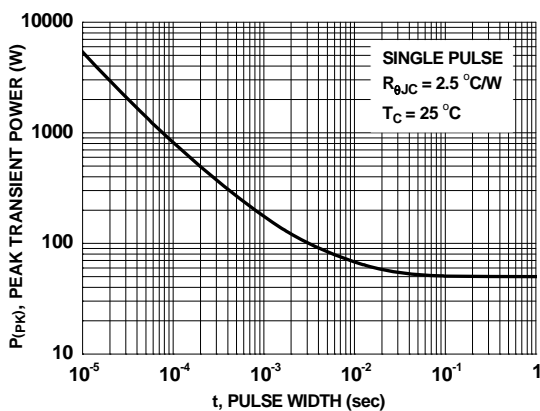
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs Case Temperature**

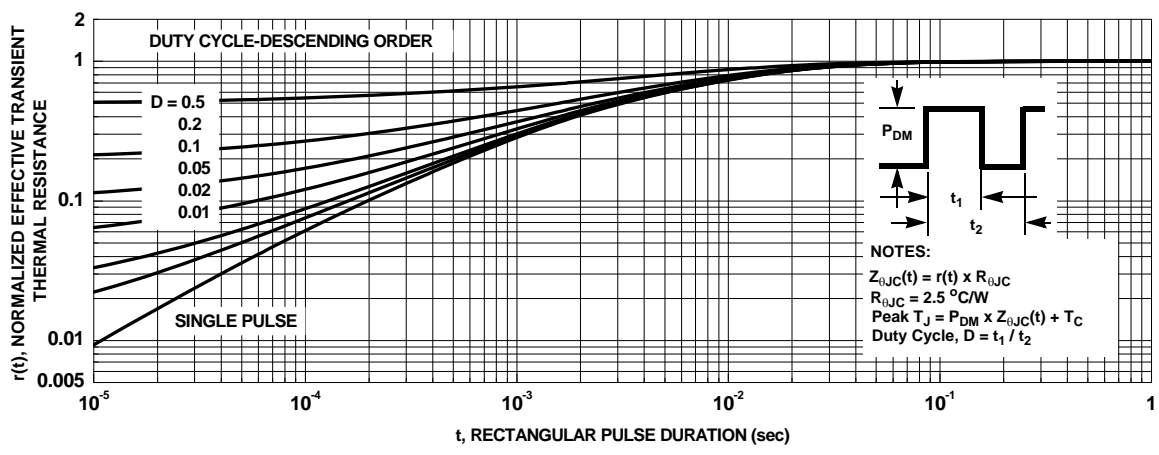


**Figure 11. Forward Bias Safe Operating Area**



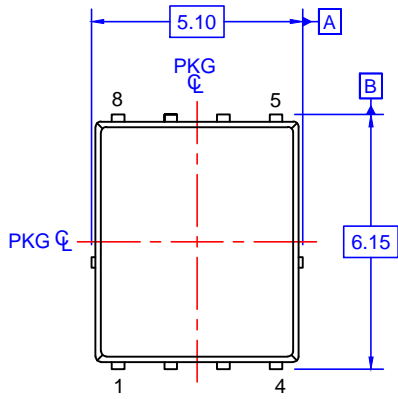
**Figure 12. Single Pulse Maximum Power Dissipation**

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted

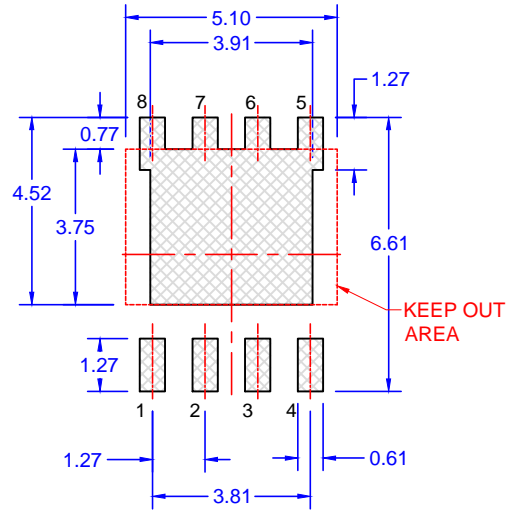
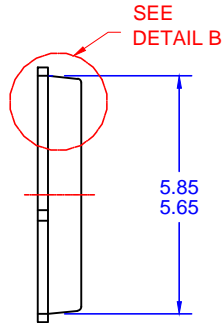


**Figure 13. Junction-to-Case Transient Thermal Response Curve**

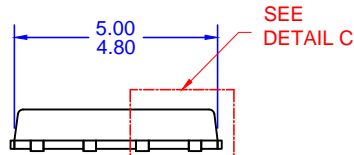
PQFN8 5X6, 1.27P  
CASE 483AE  
ISSUE A



TOP VIEW

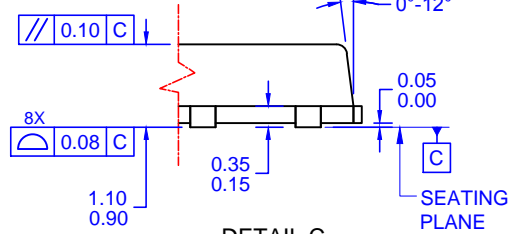


LAND PATTERN RECOMMENDATION

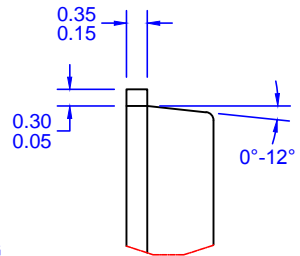


SIDE VIEW

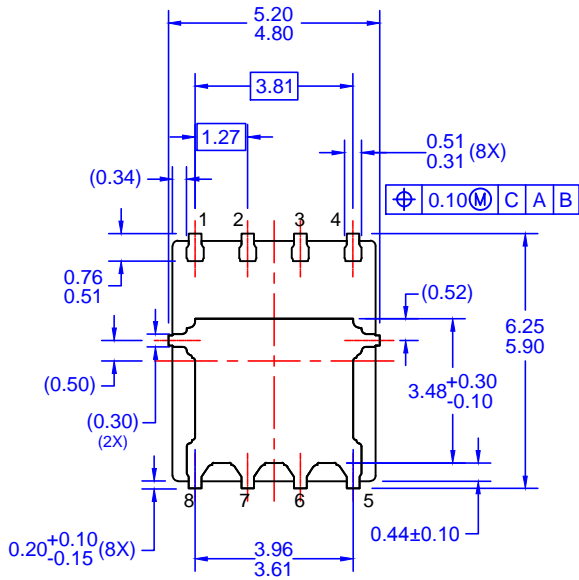
OPTIONAL DRAFT ANGLE MAY APPEAR ON FOUR SIDES OF THE PACKAGE



DETAIL C  
SCALE: 2:1



DETAIL B  
SCALE: 2:1



BOTTOM VIEW

NOTES: UNLESS OTHERWISE SPECIFIED

- A. PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA.
- B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- E. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

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