

CGHV31500F1

2.7 – 3.1 GHz, 500 W GaN HEMT

Description

Wolfspeed's CGHV31500F1 is a gallium nitride (GaN) high electron mobility transistor (HEMT) designed specifically with high efficiency and high gain for the 2.7 - 3.1 GHz S-Band radar band. The device has been developed with long pulse capability to meet the developing trends in radar architectures. The transistor is matched to 50-ohms on the input and 50-ohms on the output. The CGHV31500F1 is based on Wolfspeed's high power density 50 V, 0.4 μm GaN on silicon carbide (SiC) manufacturing process. The transistor is supplied in a ceramic/metal flange package of type 440226.



Figure 1. CGHV31500F1

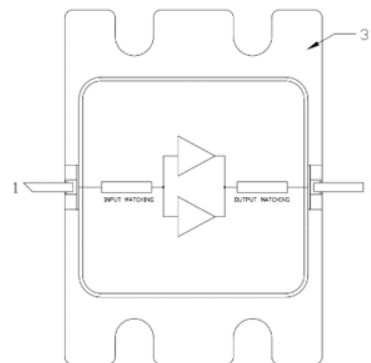


Figure 2. Functional Block Diagram

Features

- Psat: 500 W
- DE: >65%
- LSG: 13 dB

Note: Features are typical performance across frequency under 25C operation. Please reference performance charts for additional information.

Applications

- Civil and Military Pulsed Radar Amplifiers



Absolute Maximum Ratings

Parameter	Symbol	Units	Value	Conditions
Drain Voltage	V_d	V	50	25°C
Gate Voltage	V_g	V	-10, +2	25°C
Drain Current	I_d	A	24	
Gate Current	I_g	mA	80	25°C
Input Power	P_{in}	dBm	48	
Dissipated Power	P_{diss}	W	418	85°C
Storage Temperature	T_{stg}	°C	-55, +150	
Mounting Temperature	T_J	°C	320	30 seconds
Junction Temperature	T_J	°C	225	MTTF $\geq 1E6$ hours
Output Mismatch Stress	VSWR	Ψ	5:1	
Pulse Width	PW	μ S	2000	
Duty Cycle	DC	%	20	

Recommended Operating Conditions

Parameter	Symbol	Units	Typical Value	Conditions
Drain Voltage	V_d	V	50	
Gate Voltage	V_g	V	-2.7	
Drain Current	I_{dq}	mA	500	
Input Power	P_{in}	dBm	46	
Case Temperature	T_{case}	°C	-40 to 75	2mS, DC = 20%

RF Specifications

Test conditions unless otherwise noted: $V_d=50$ V, $I_{dq}=500$ mA, $PW=2000$ μ S, $DC=20\%$, $T_{base}=25$ °C

Parameter	Units	Frequency	Min	Typical	Max	Conditions
Frequency	GHz		2.7		3.1	
Output Power	dBm	2.7 GHz		57.0		$P_{in} = 46$ dBm
		2.9 GHz		57.9		
		3.1 GHz		57.0		
Drain Efficiency	%	2.7 GHz		63		$P_{in} = 46$ dBm
		2.9 GHz		71		
		3.1 GHz		61		
LSG	dB	2.7 GHz		11.0		$P_{in} = 46$ dBm
		2.9 GHz		11.9		
		3.1 GHz		11.0		
Small-Signal	dB			14.5		$P_{in} = -20$ dBm
Input Return	dB			-15		$P_{in} = -20$ dBm
Output Return	dB			-6		$P_{in} = -20$ dBm

Test conditions unless otherwise noted: $V_d = 50$ V, $I_{dq} = 500$ mA, $PW=100$ μ S, $DC=10\%$, $P_{in} = 46$ dBm, $T_{base}=25$ °C, Frequency = 2.9 GHz

Figure 3: Pout v. Frequency v. Temperature

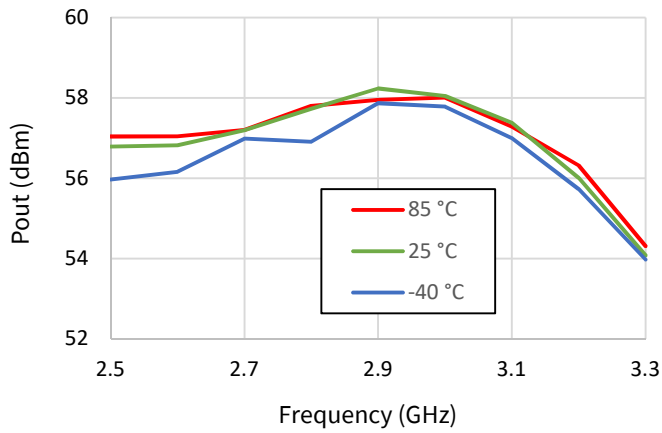


Figure 4: DE v. Frequency v. Temperature

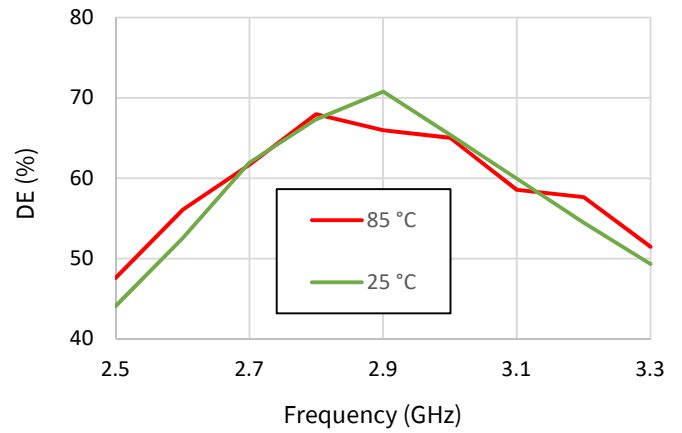


Figure 5: Id v. Frequency v. Temperature

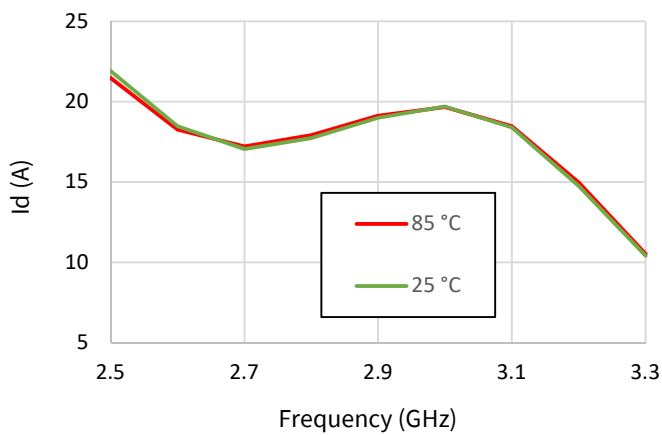


Figure 6: Ig v. Frequency v. Temperature

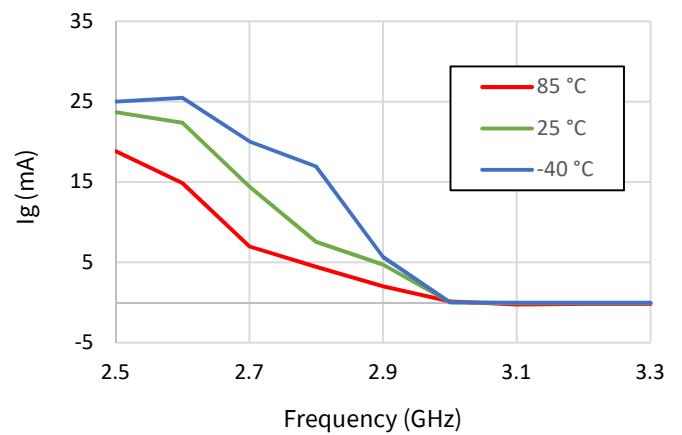
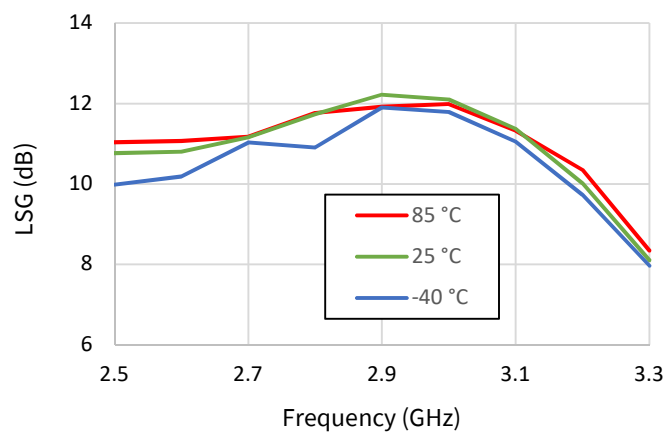


Figure 7: LSG v. Frequency v. Temperature



Test conditions unless otherwise noted: Vd=50V, Idq= 500mA, PW=100uS, DC=10%, Pin =46dBm, T_{base}=25°C, Frequency = 2.9 GHz

Figure 8: Pout v. Frequency v. Vd

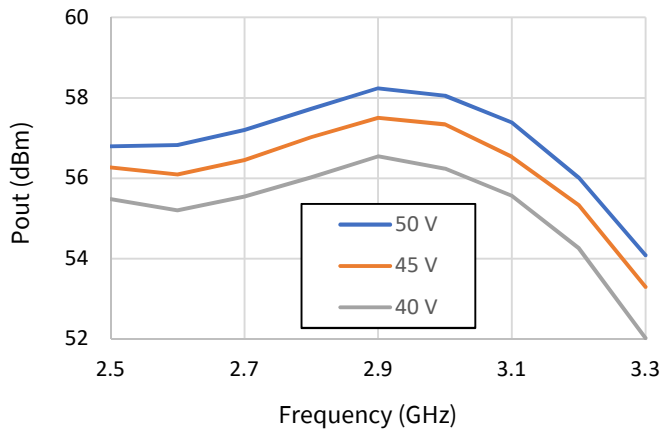


Figure 9: DE v. Frequency v. Vd

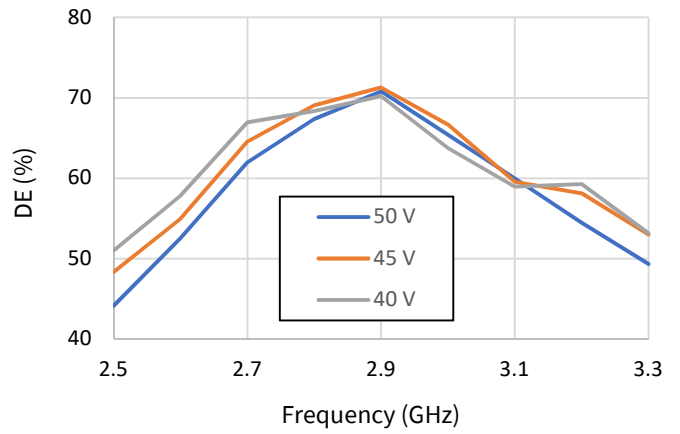


Figure 10: Id v. Frequency v. Vd

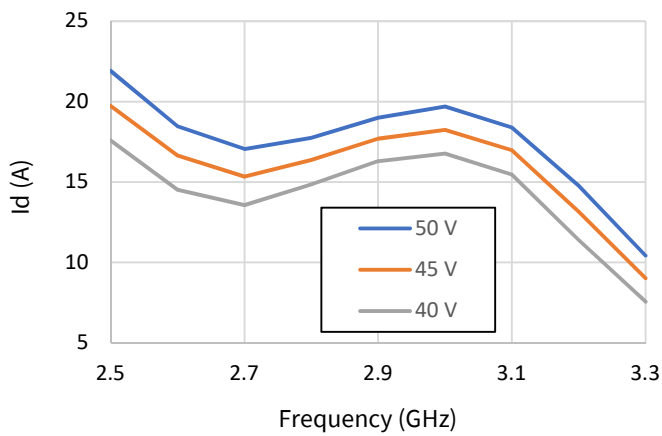


Figure 11: Ig v. Frequency v. Vd

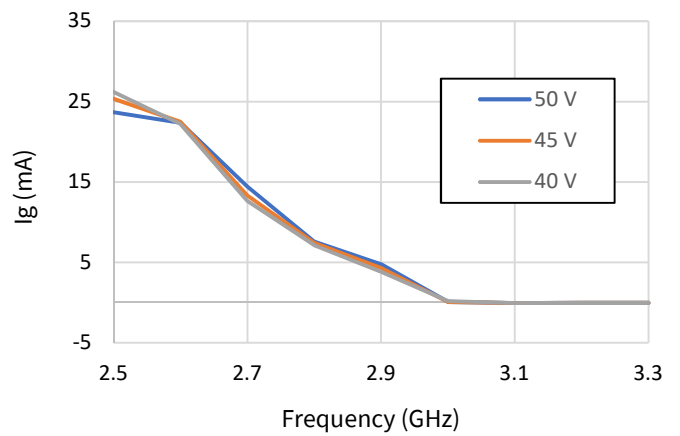
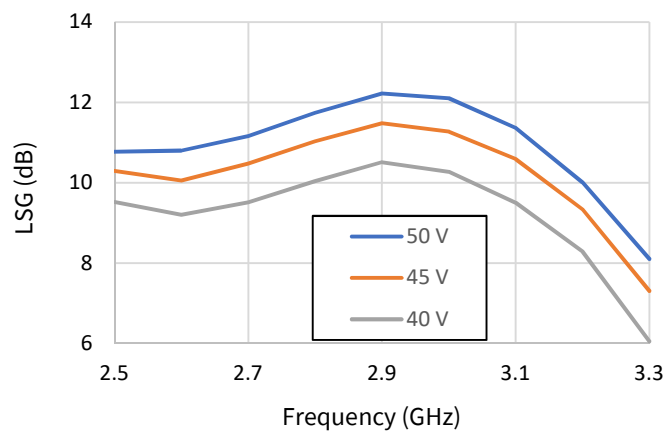


Figure 12: LSG v. Frequency v. Vd



Test conditions unless otherwise noted: Vd=50V, Idq= 500mA, PW=100uS, DC=10%, Pin =46dBm, T_{base}=25°C, Frequency = 2.9 GHz

Figure 13: Pout v. Frequency v. Idq

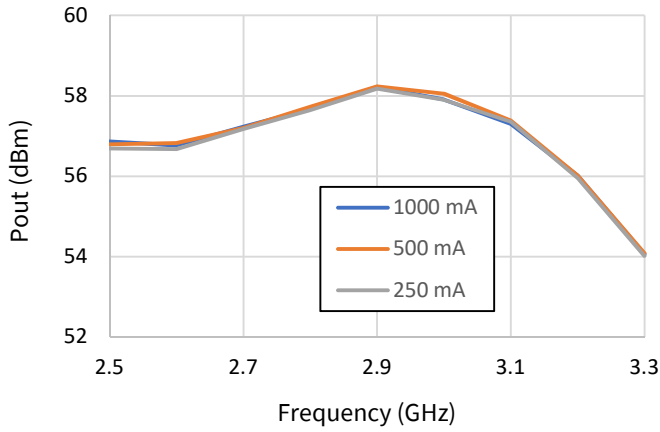


Figure 14: DE v. Frequency v. Idq

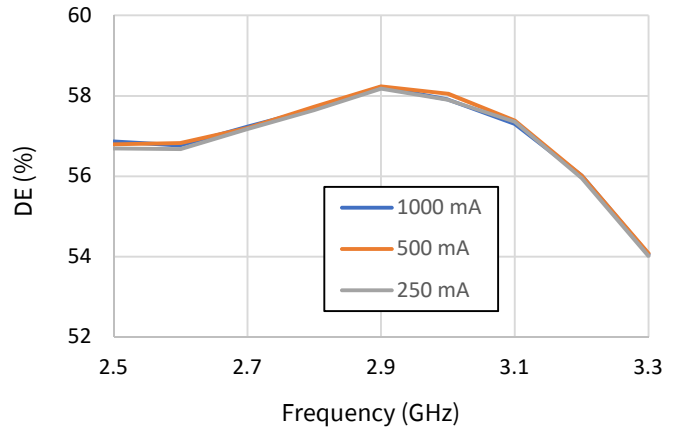


Figure 15: Id v. Frequency v. Idq

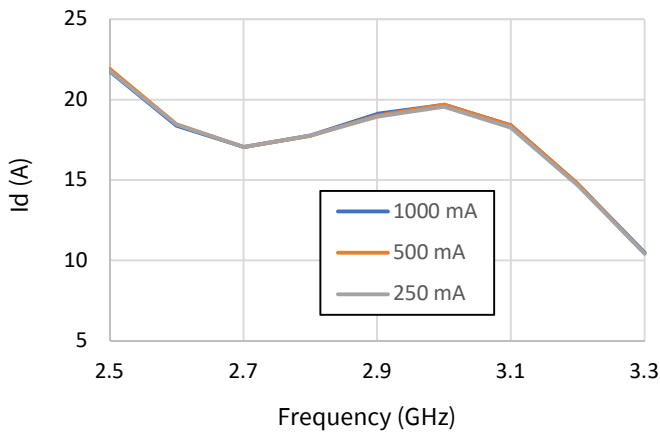


Figure 16: Ig v. Frequency v. Idq

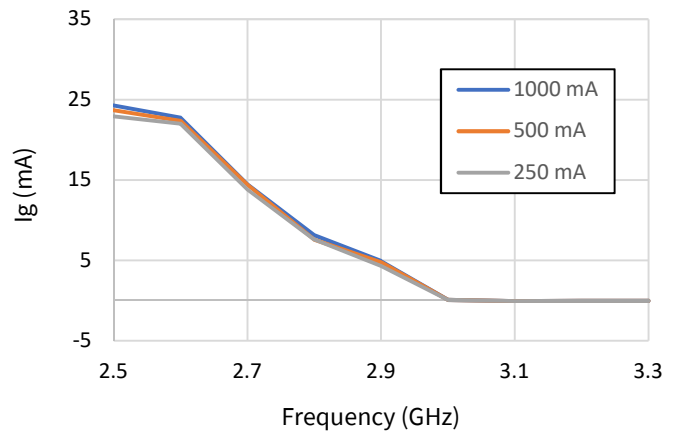
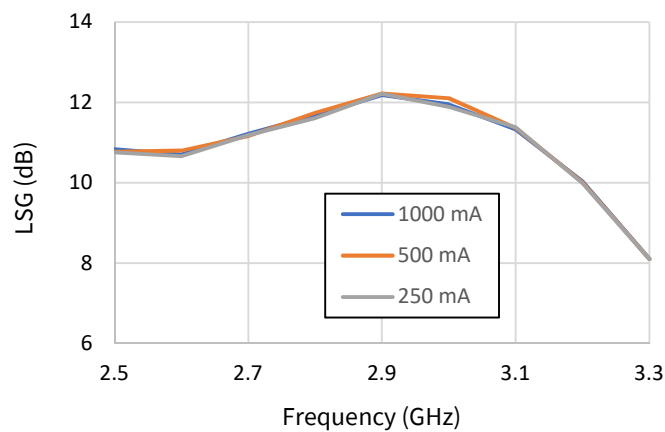


Figure 17: LSG v. Frequency v. Idq



Test conditions unless otherwise noted: $V_d=50V$, $I_{dQ}=500mA$, $PW=100\mu S$, $DC=10\%$, $P_{in}=46dBm$, $T_{base}=25^\circ C$, Frequency = 2.9 GHz

Figure 18: Pout v. Pin v. Frequency

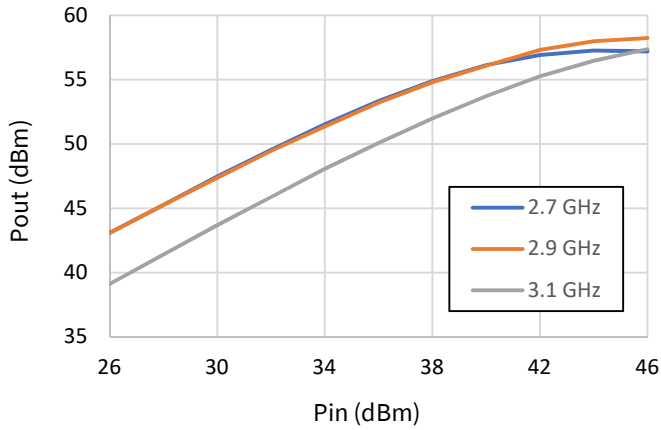


Figure 19: DE v. Pin v. Frequency

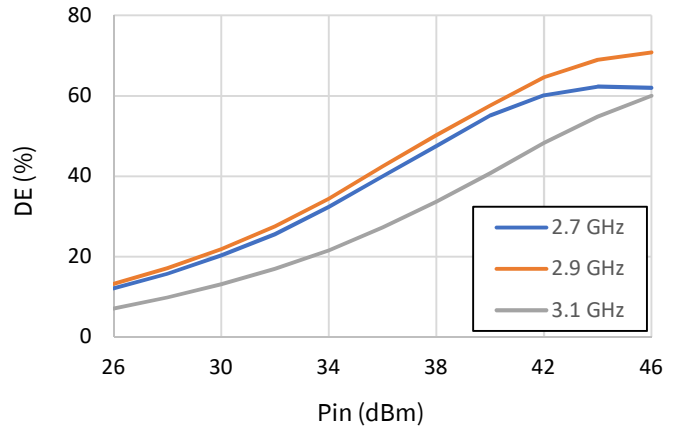


Figure 20: Id v. Pin v. Frequency

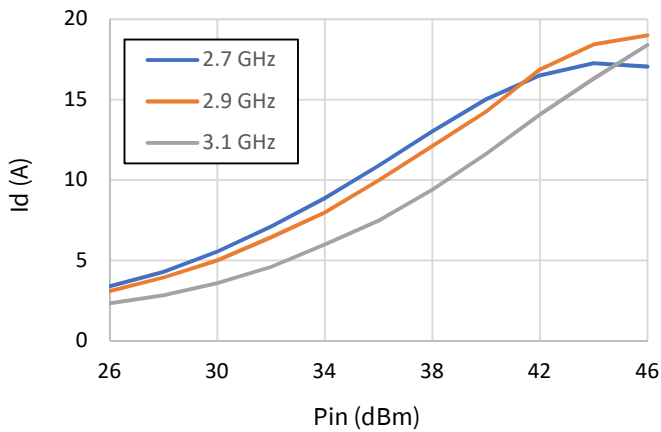


Figure 21: Ig v. Pin v. Frequency

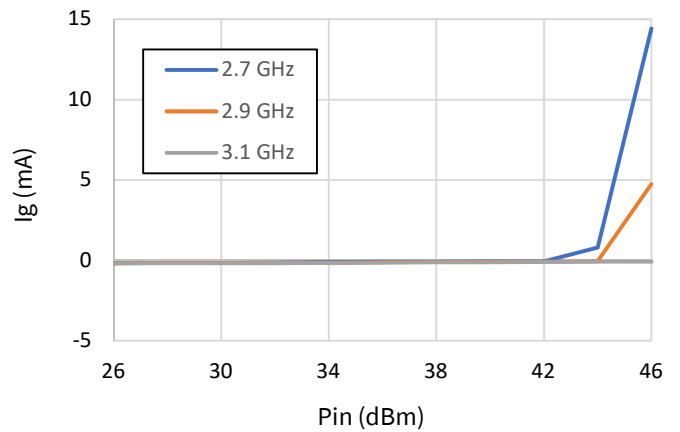
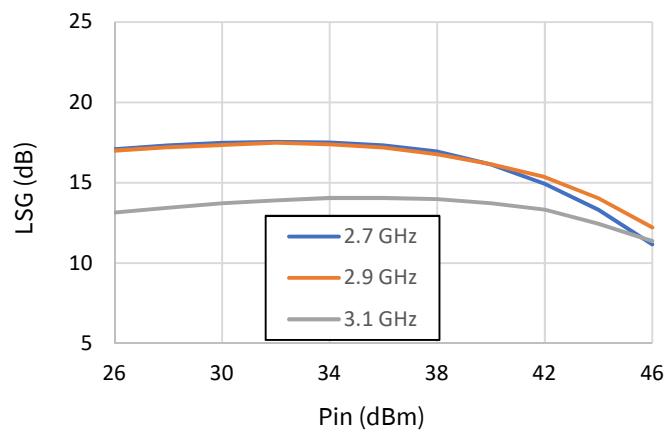


Figure 22: Gain v. Pin v. Frequency



Test conditions unless otherwise noted: $V_d=50V$, $I_{dq}=500mA$, $PW=100\mu s$, $DC=10\%$, $P_{in}=46dBm$, $T_{base}=25^\circ C$, Frequency = 2.9 GHz

Figure 23: Pout v. Pin v. Temperature

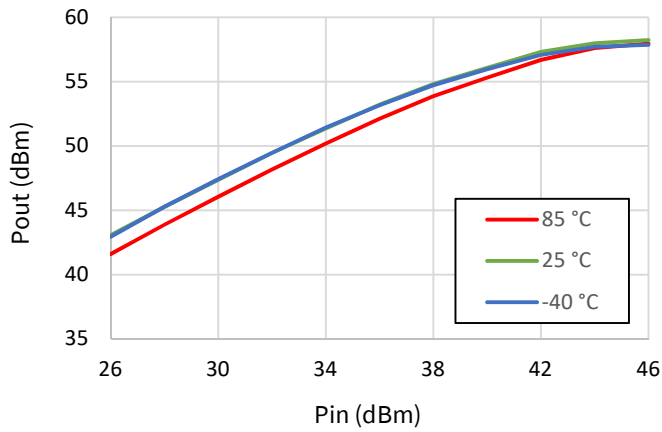


Figure 24: DE v. Pin v. Temperature

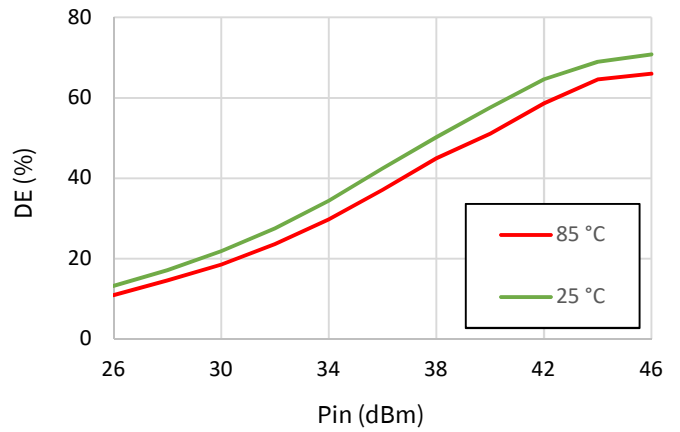


Figure 25: Id v. Pin v. Temperature

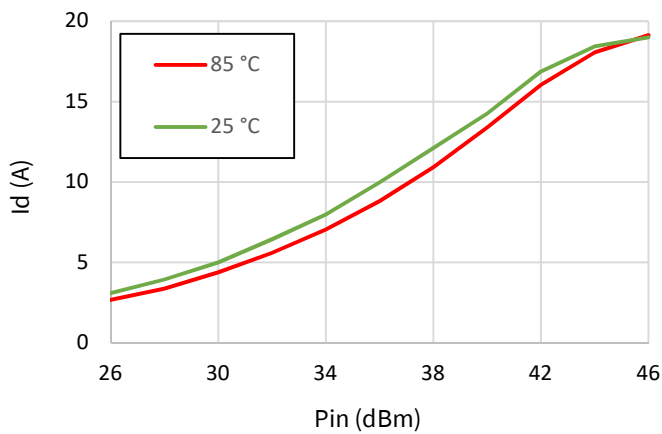


Figure 26: Ig v. Pin v. Temperature

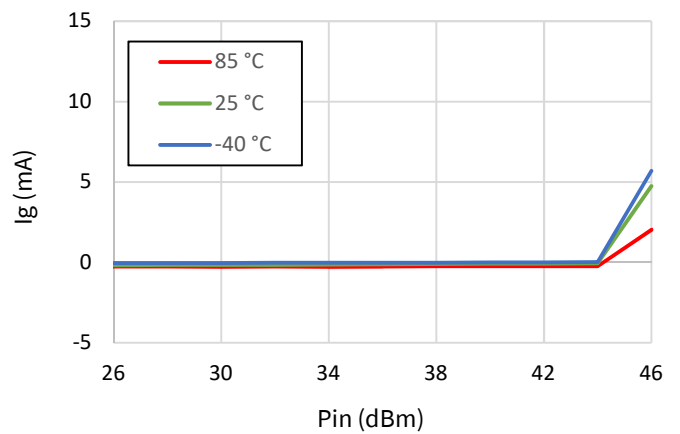
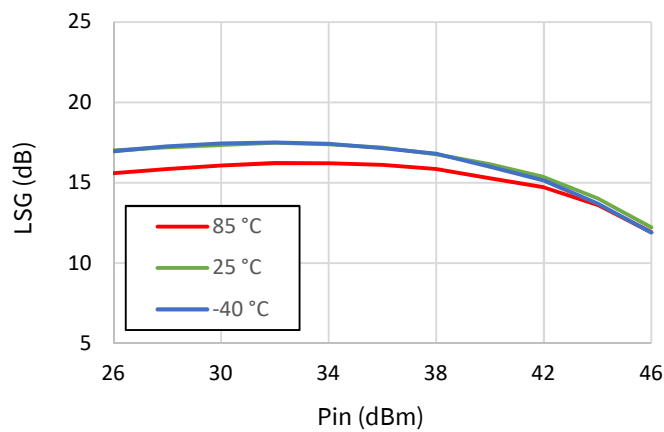


Figure 27: Gain v. Pin v. Temperature



Test conditions unless otherwise noted: Vd=50V, Idq= 500mA, PW=100uS, DC=10%, Pin =46dBm, T_{base}=25°C, Frequency = 2.9 GHz

Figure 28: Pout v. Pin v. Vd

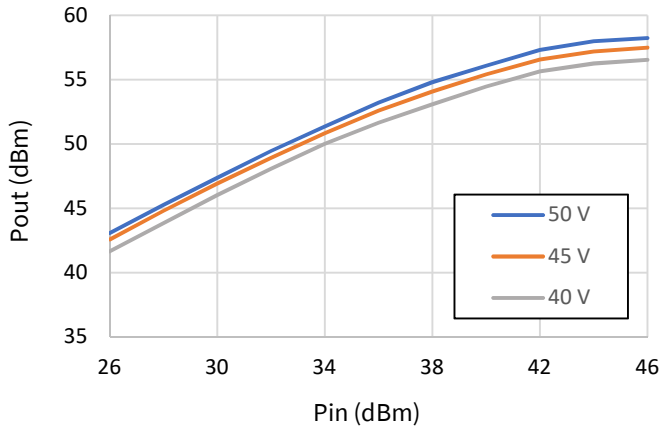


Figure 29: DE v. Pin v. Vd

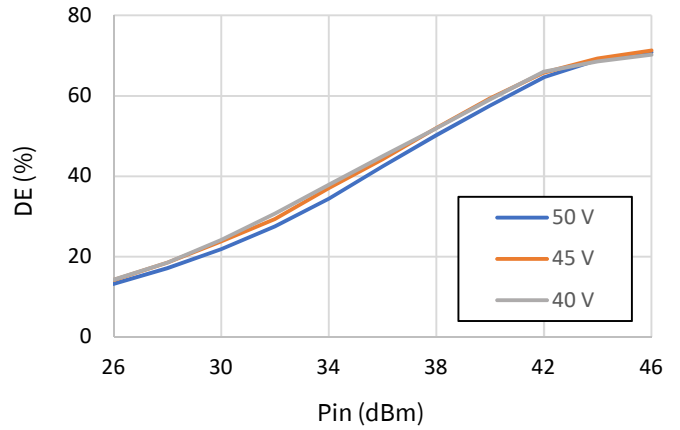


Figure 30: Id v. Pin v. Vd

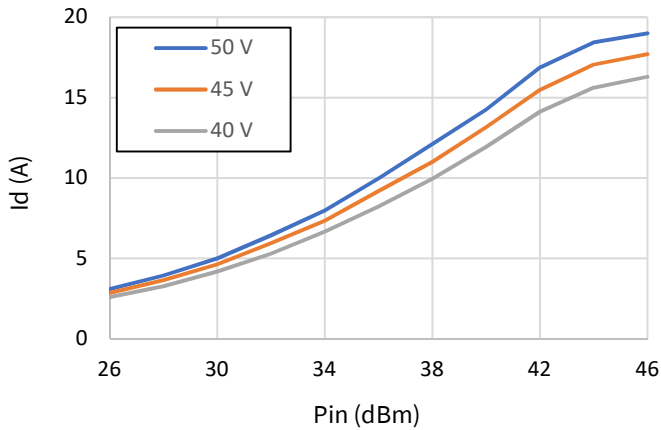


Figure 31: Ig v. Pin v. Vd

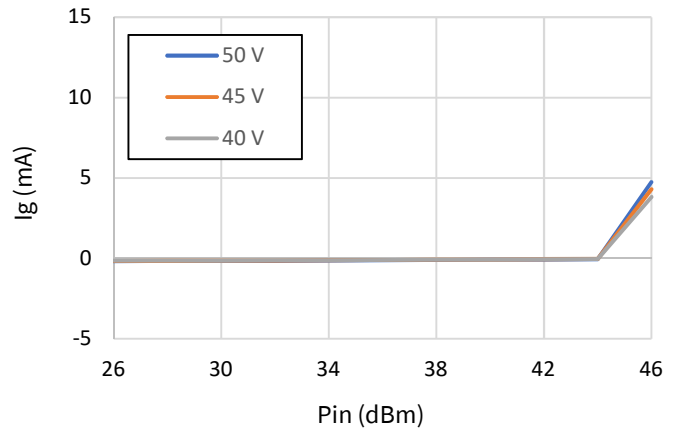
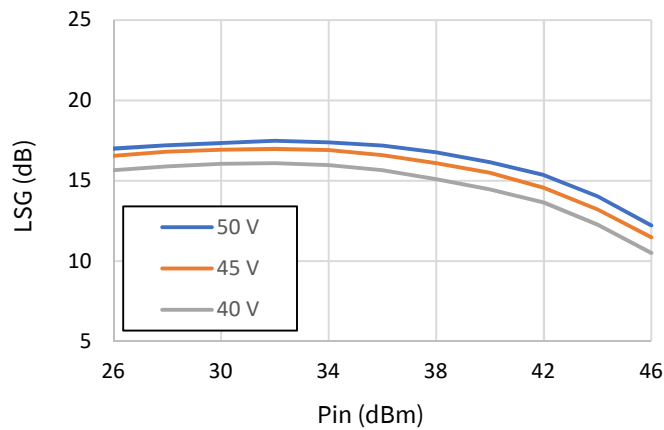


Figure 32: Gain v. Pin v. Vd



Test conditions unless otherwise noted: Vd=50V, Idq= 500mA, PW=100uS, DC=10%, Pin =46dBm, T_{base}=25°C, Frequency = 2.9 GHz

Figure 33: Pout v. Pin v. Idq

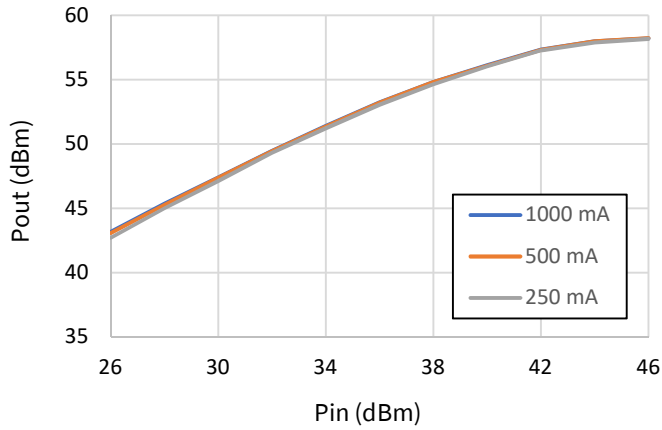


Figure 34: DE v. Pin v. Idq

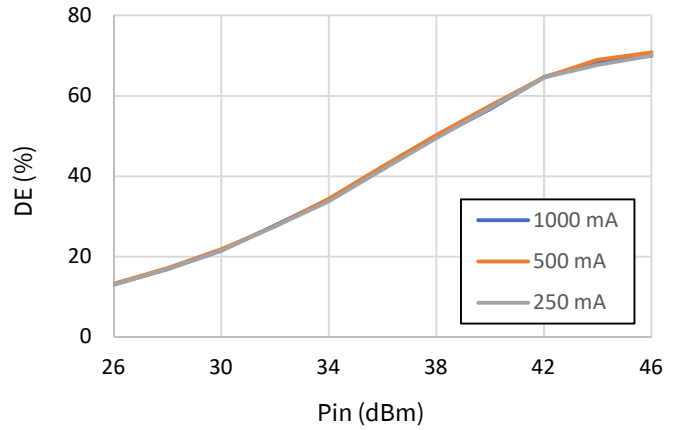


Figure 35: Id v. Pin v. Idq

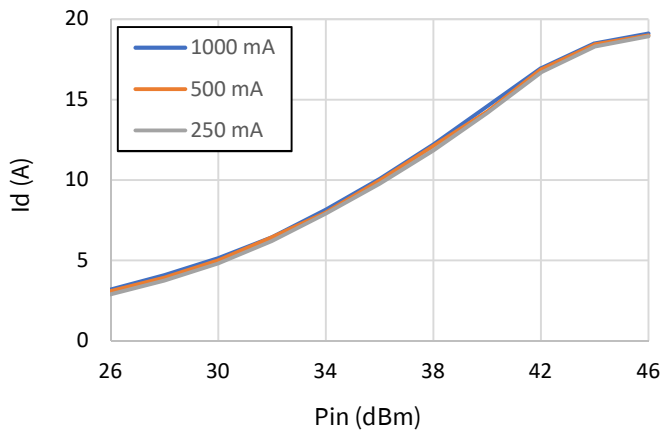


Figure 36: Ig v. Pin v. Idq

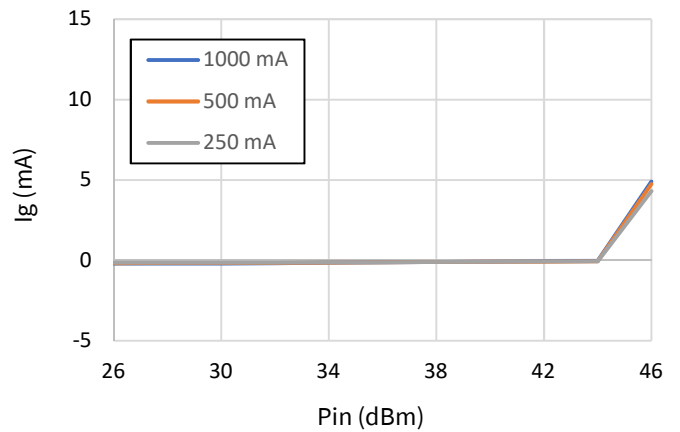
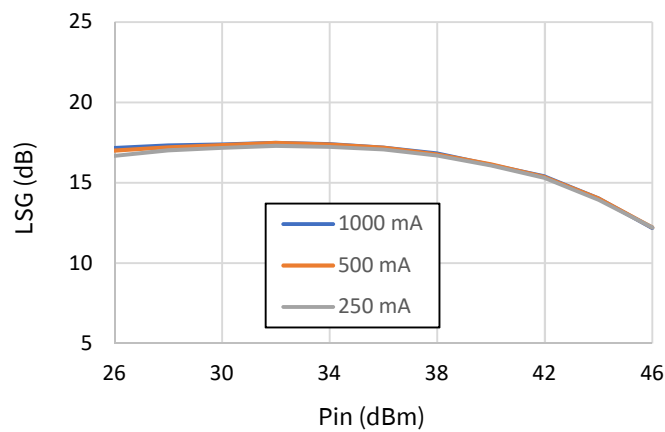


Figure 37: Gain v. Pin v. Idq



Test conditions unless otherwise noted: $V_d=50V$, $I_{dq}=500mA$, $PW=2000\mu s$, $DC=20\%$, $P_{in}=46dBm$, $T_{base}=25^\circ C$, Frequency = 2.9 GHz

Figure 38: Pout v. Frequency v. Temperature

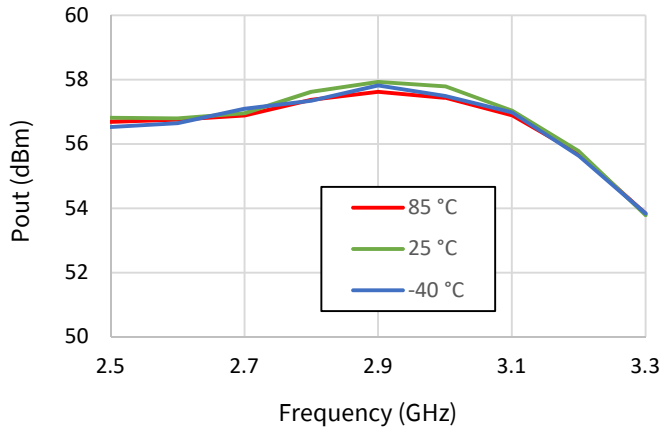


Figure 39: DE v. Frequency v. Temperature

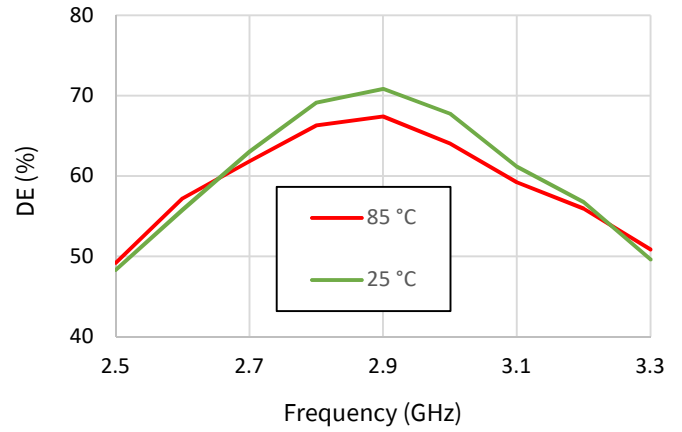


Figure 40: Id v. Frequency v. Temperature

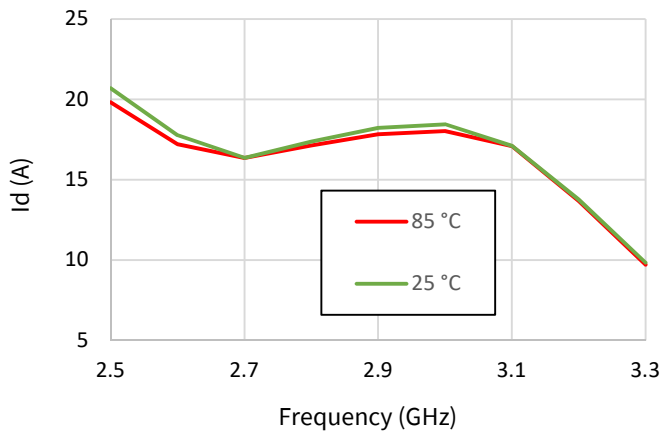


Figure 41: Ig v. Frequency v. Temperature

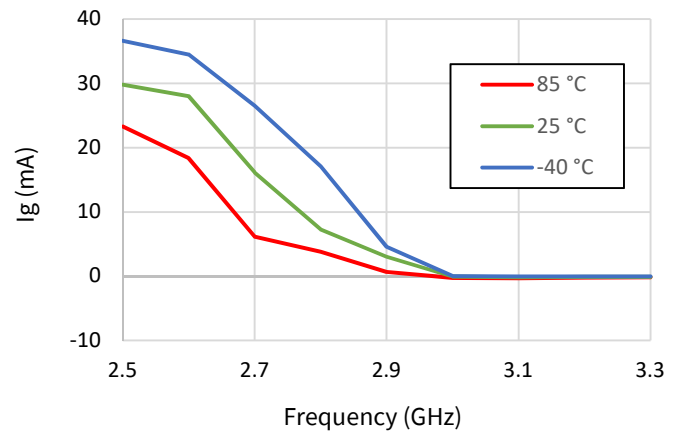
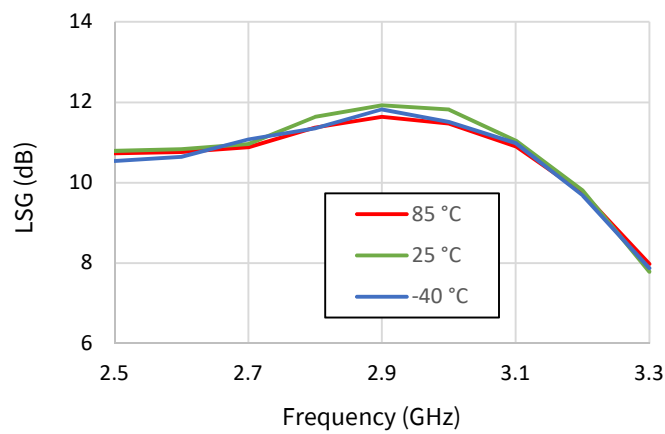


Figure 42: LSG v. Frequency v. Temperature



Test conditions unless otherwise noted: Vd=50V, Idq= 500mA, PW=2000uS, DC=20%, Pin = 46dBm, T_{base}=25 °C, Frequency =2.9 GHz

Figure 43: Pout v. Frequency v. Vd

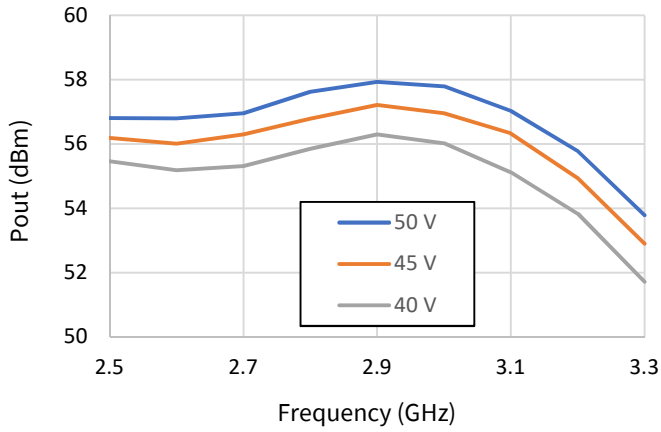


Figure 44: DE v. Frequency v. Vd

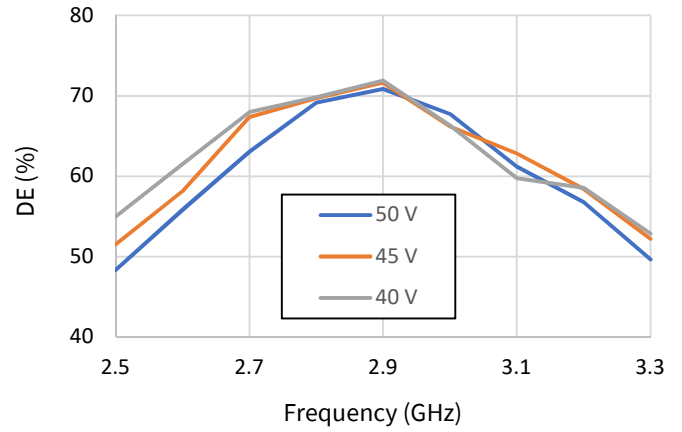


Figure 45: Id v. Frequency v. Vd

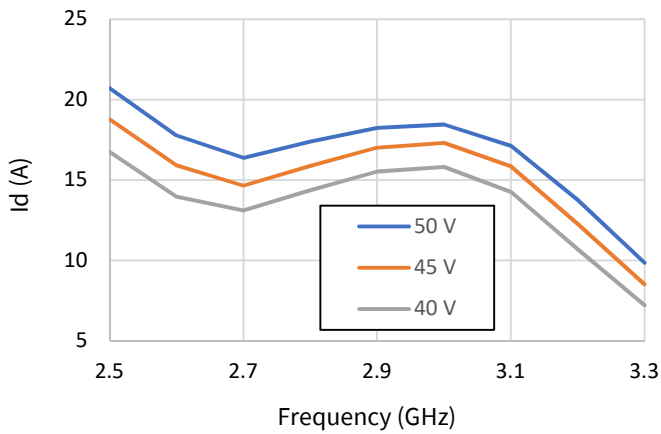


Figure 46: Ig v. Frequency v. Vd

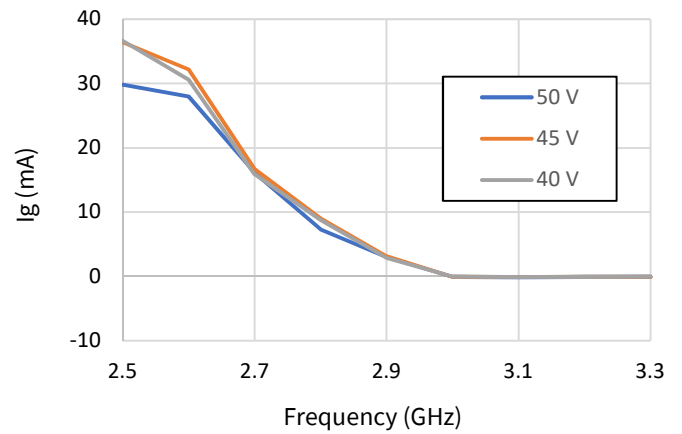
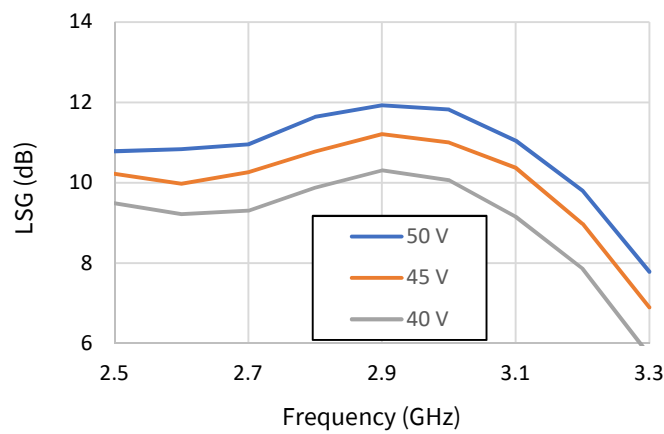


Figure 47: LSG v. Frequency v. Vd



Test conditions unless otherwise noted: Vd=50V, Idq= 500mA, PW=2000uS, DC=20%, Pin = 46dBm, T_{base}=25 °C, Frequency =2.9 GHz

Figure 48: Pout v. Frequency v. Idq

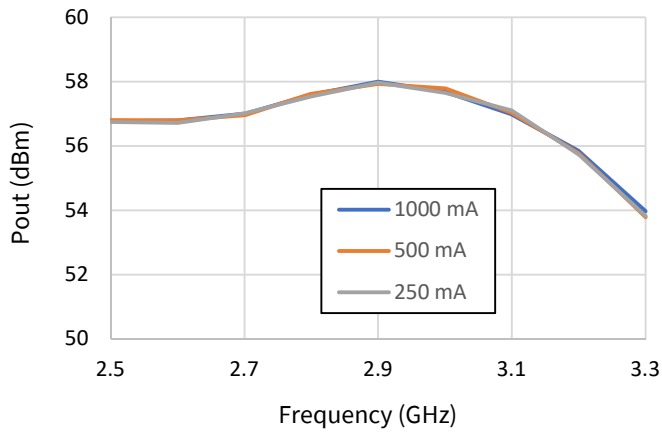


Figure 49: DE v. Frequency v. Idq

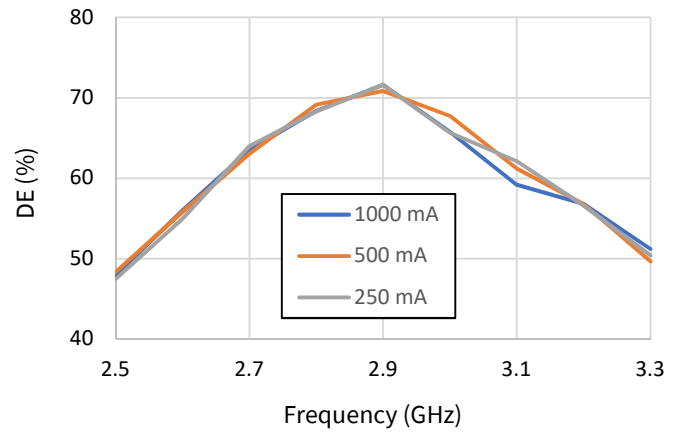


Figure 50: Id v. Frequency v. Idq

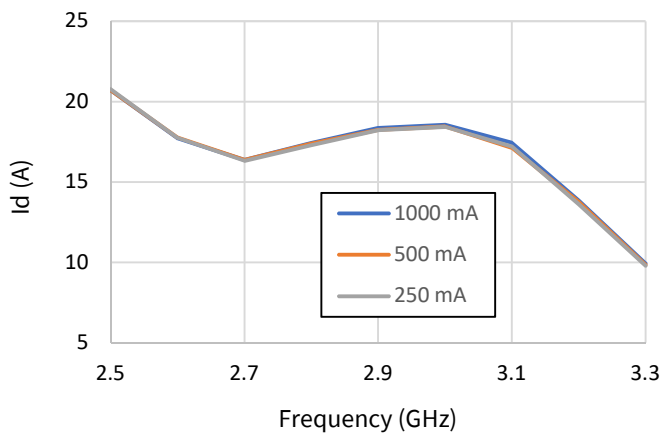


Figure 51: Ig v. Frequency v. Idq

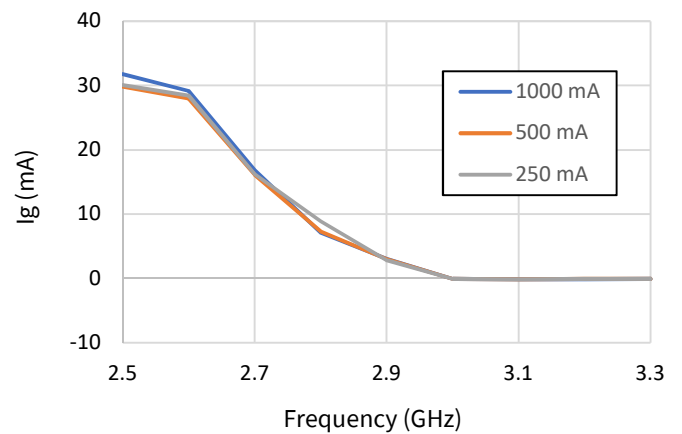
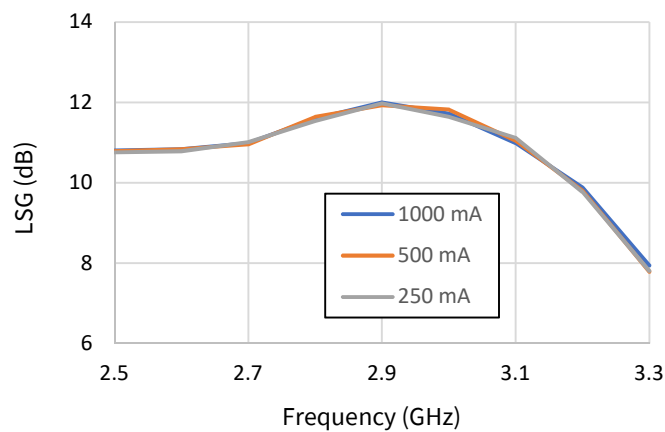


Figure 52: LSG v. Frequency v. Idq



Test conditions unless otherwise noted: $V_d=50V$, $I_{dq}=500mA$, $PW=2000\mu s$, $DC=20\%$, $P_{in}=46dBm$, $T_{base}=25^\circ C$, Frequency = 2.9 GHz

Figure 53: Pout v. Pin v. Frequency

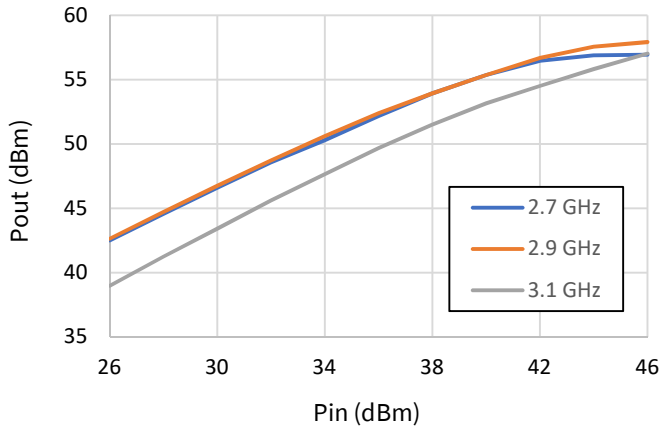


Figure 54: DE v. Pin v. Frequency

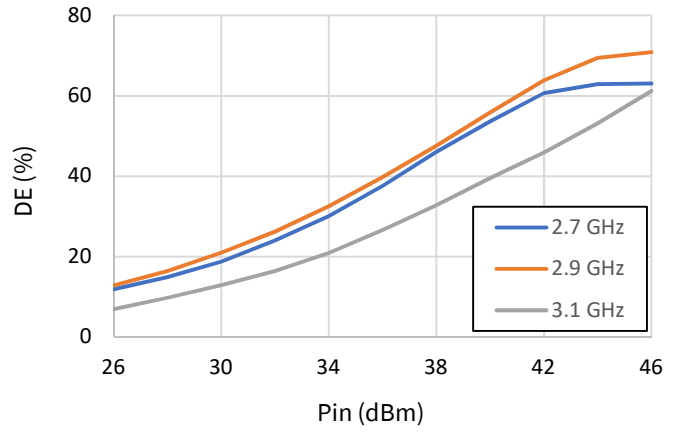


Figure 55: Id v. Pin v. Frequency

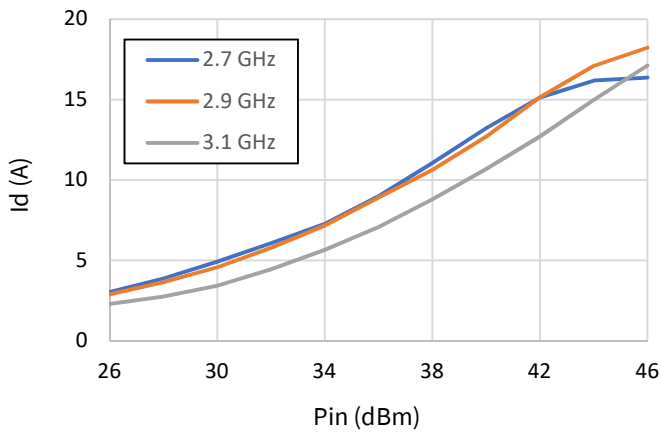


Figure 56: Ig v. Pin v. Frequency

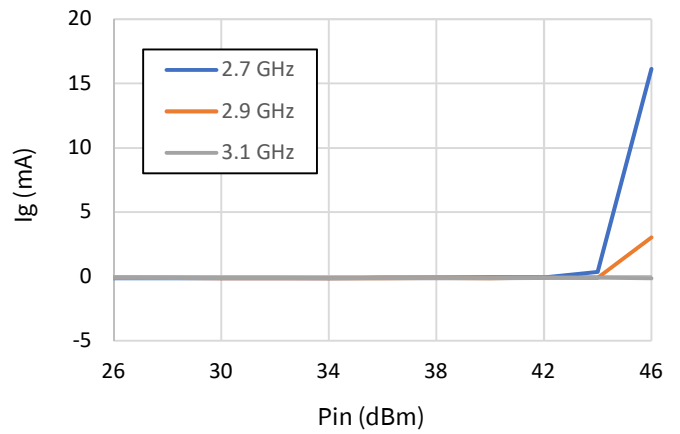
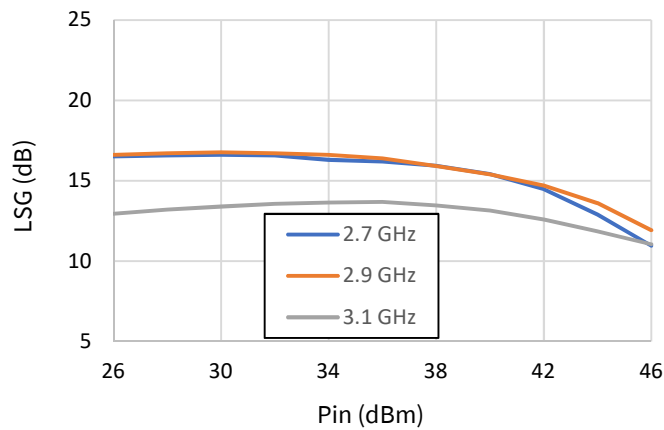


Figure 57: Gain v. Pin v. Frequency



Test conditions unless otherwise noted: $V_d=50V$, $I_{dQ}=500mA$, $PW=2000\mu s$, $DC=20\%$, $P_{in}=46dBm$, $T_{base}=25^\circ C$, Frequency = 2.9 GHz

Figure 58: Pout v. Pin v. Temperature

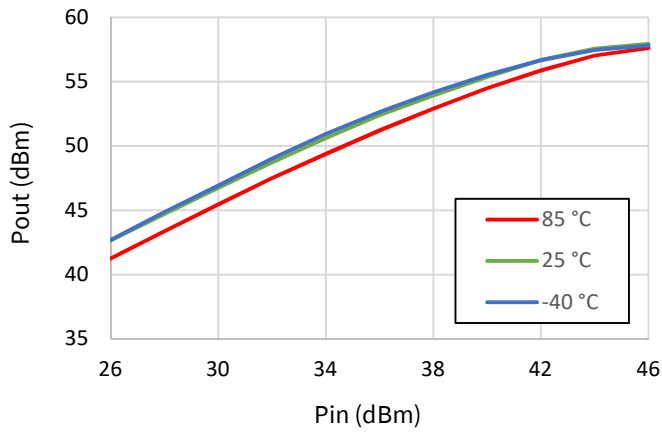


Figure 59: DE v. Pin v. Temperature

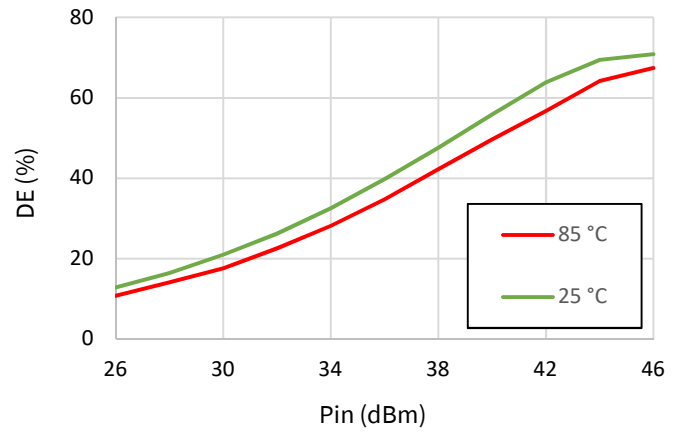


Figure 60: Id v. Pin v. Temperature

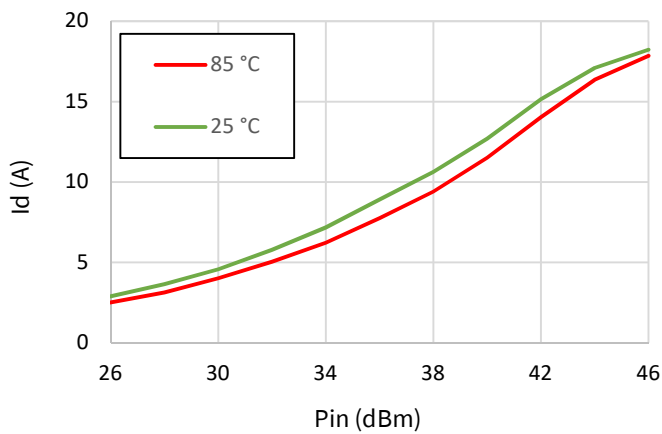


Figure 61: Ig v. Pin v. Temperature

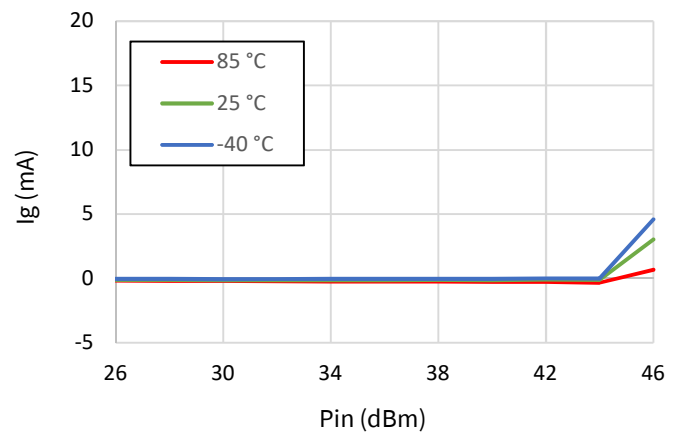
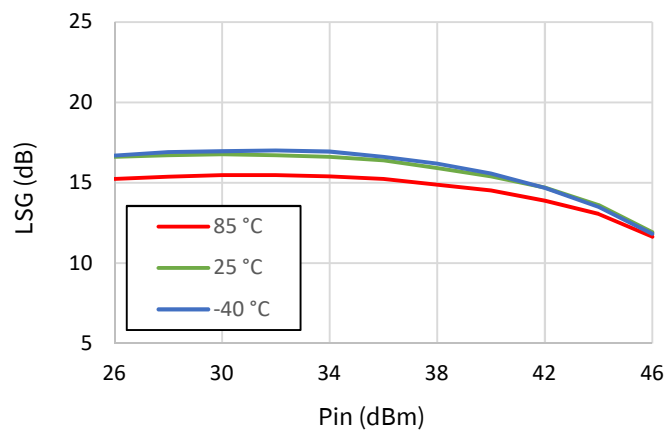


Figure 62: Gain v. Pin v. Temperature



Test conditions unless otherwise noted: Vd=50V, Idq= 500mA, PW=2000uS, DC=20%, Pin = 46dBm, T_{base}=25 °C, Frequency =2.9 GHz

Figure 63: Pout v. Pin v. Vd

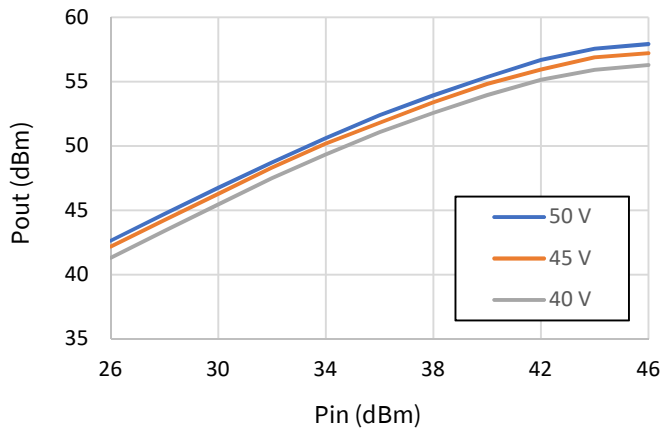


Figure 64: DE v. Pin v. Vd

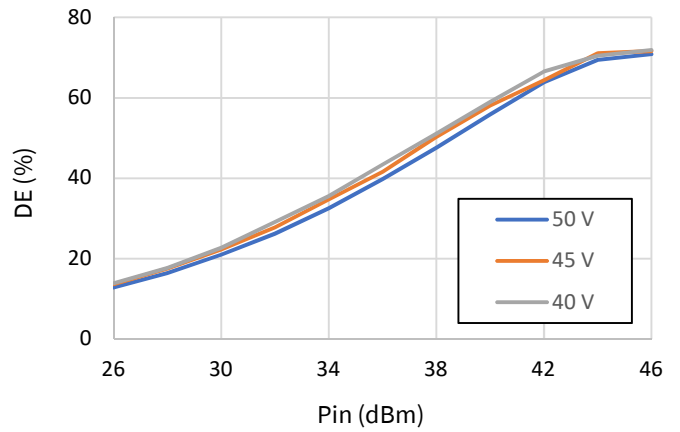


Figure 65: Id v. Pin v. Vd

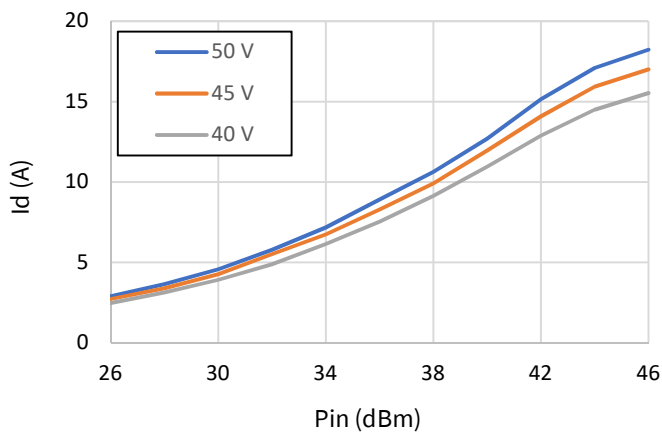


Figure 66: Ig v. Pin v. Vd

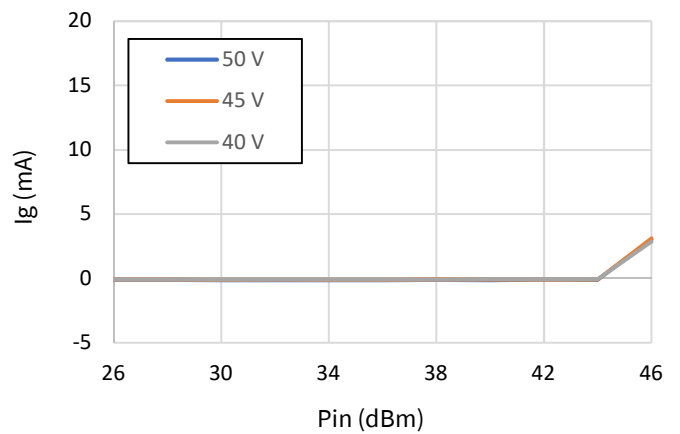
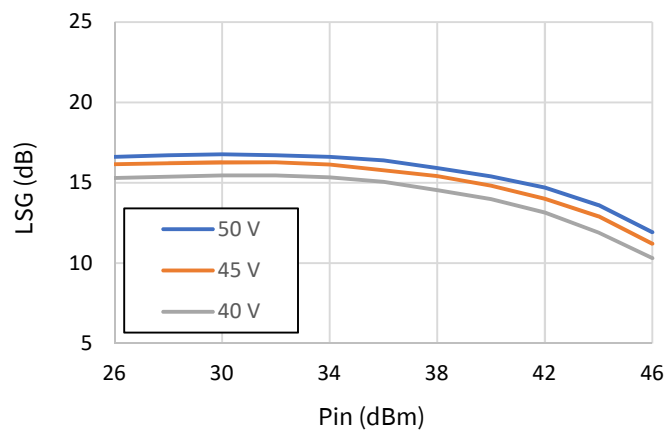


Figure 67: Gain v. Pin v. Vd



Test conditions unless otherwise noted: Vd=50V, Idq= 500mA, PW=2000uS, DC=20%, Pin = 46dBm, T_{base}=25°C, Frequency =2.9 GHz

Figure 68: Pout v. Pin v. Idq

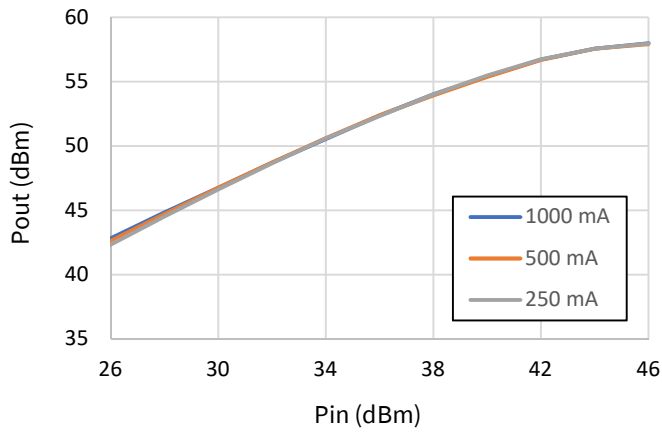


Figure 69: DE v. Pin v. Idq

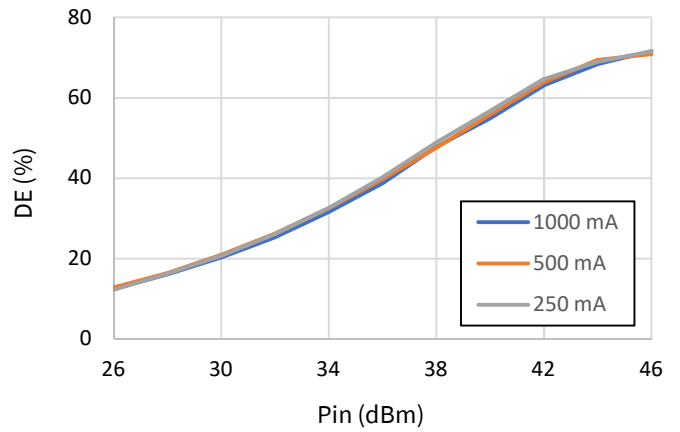


Figure 70: Id v. Pin v. Idq

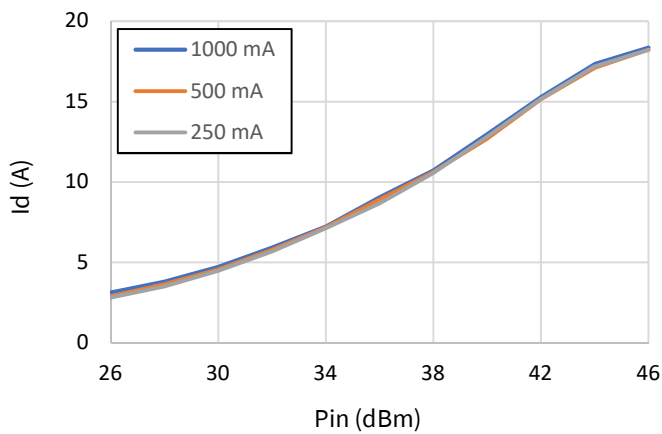


Figure 71: Ig v. Pin v. Idq

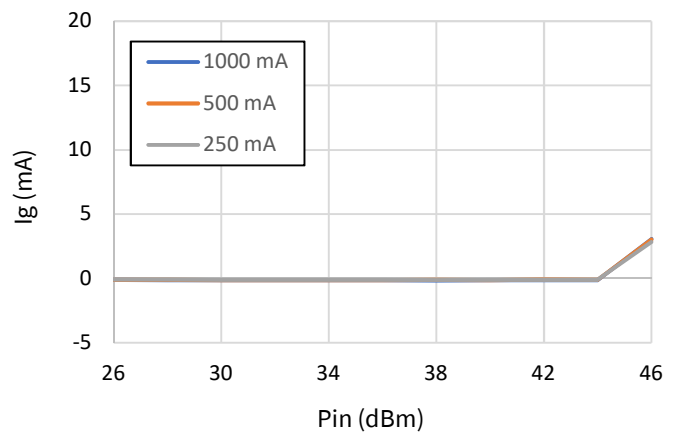
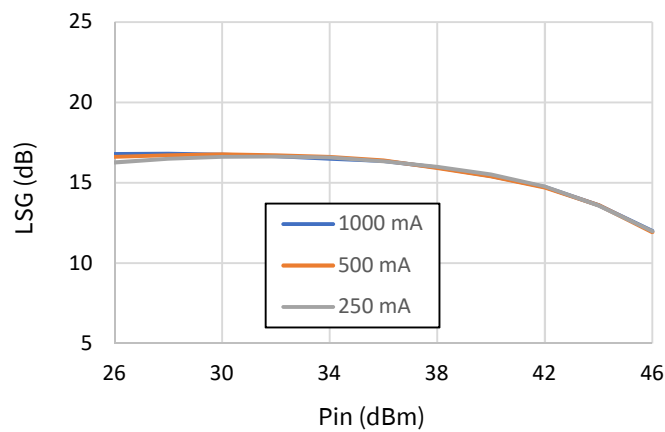


Figure 72: Gain v. Pin v. Idq



Test conditions unless otherwise noted: $V_d=50V$, $I_{dq}= 500mA$, $P_{in} = -20 \text{ dBm}$, $T_{base}=25^\circ\text{C}$

Figure 73: S21 v. Frequency v. Temperature

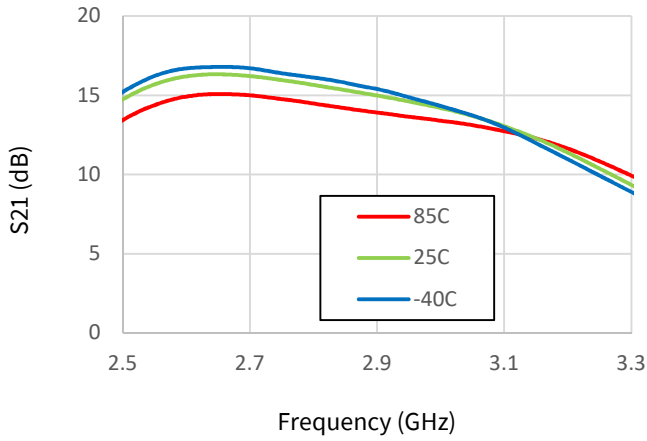


Figure 74: S21 v. Frequency v. Vd

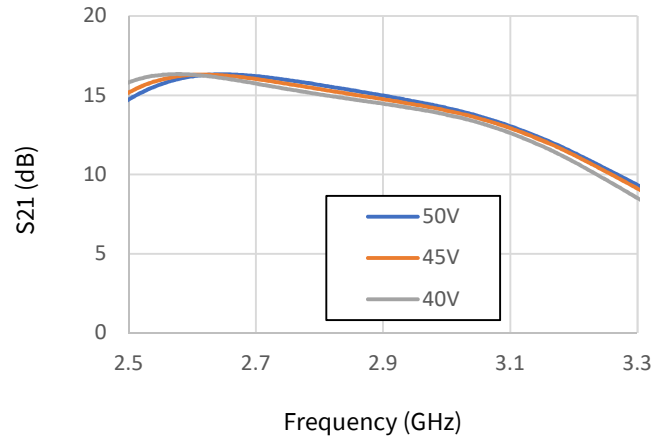


Figure 75: S11 v. Frequency v. Temperature

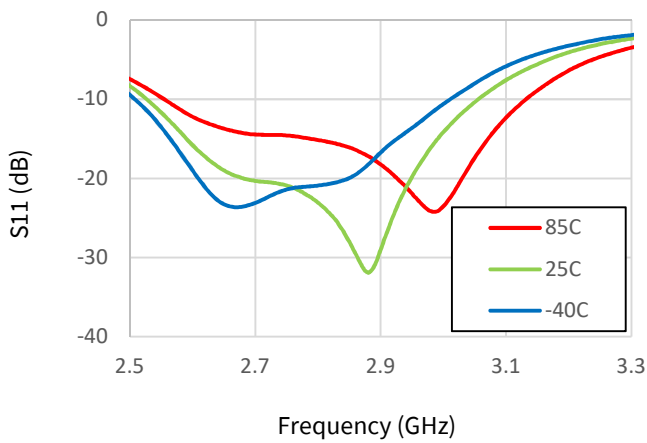


Figure 76: S11 v. Frequency v. Vd

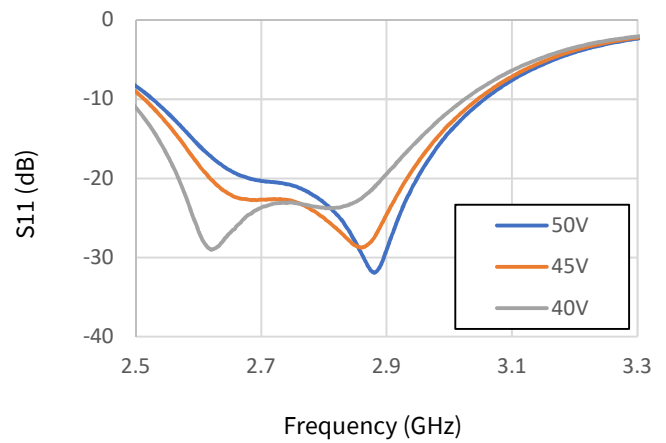


Figure 77: S22 v. Frequency v. Temperature

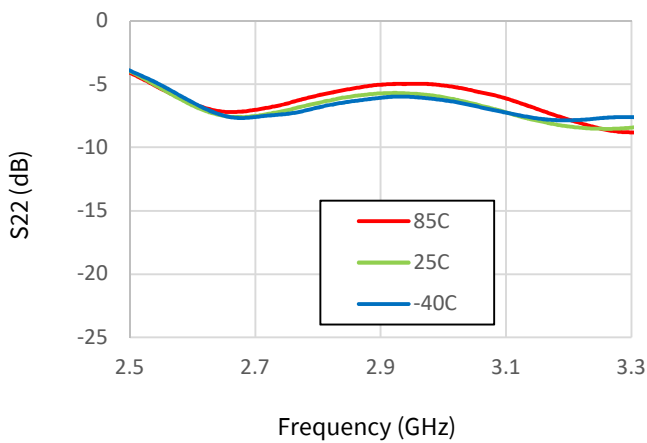
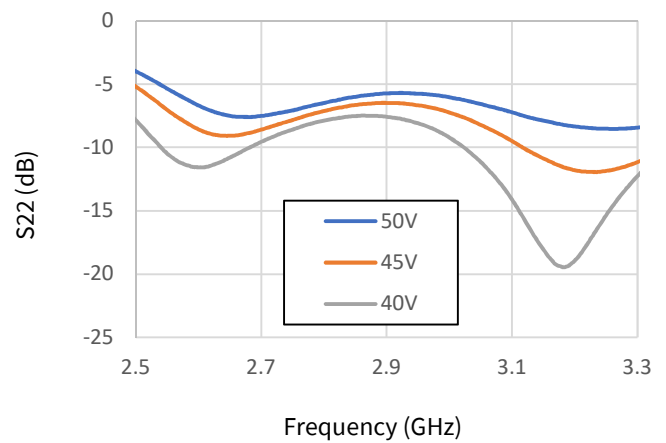


Figure 78: S22 v. Frequency v. Vd



Test conditions unless otherwise noted: $V_d=50V$, $I_{dq}=500mA$, $P_{in} = -20\text{ dBm}$, $T_{base}=25^\circ C$

Figure 79: S21 v. Frequency v. Idq

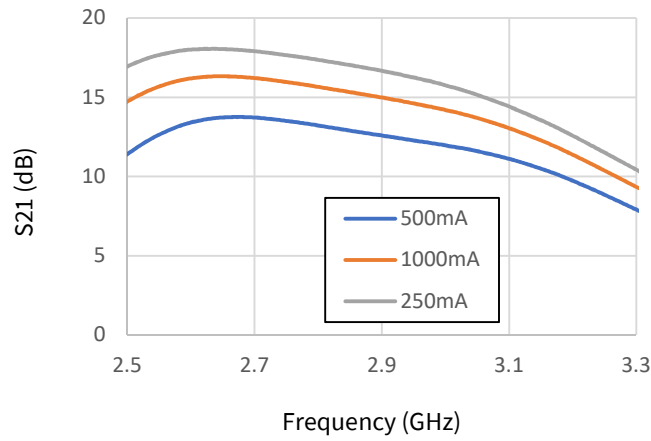


Figure 80: S11 v. Frequency v. Idq

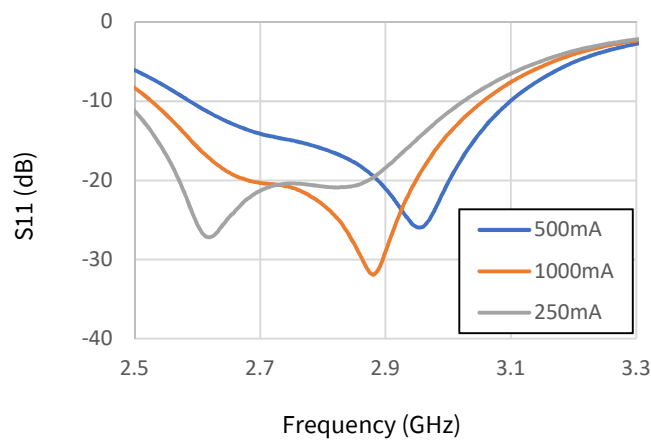
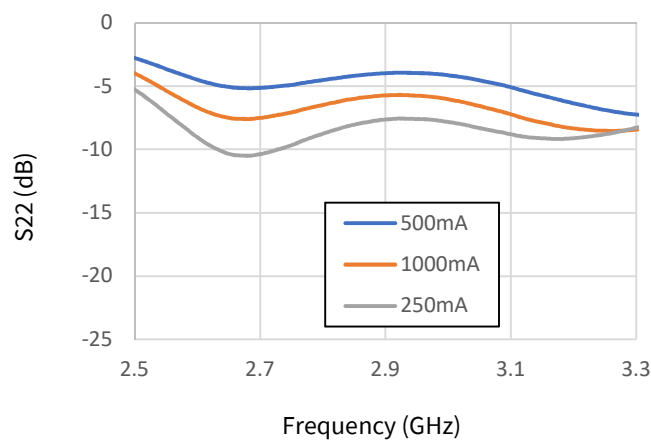


Figure 81: S22 v. Frequency v. Idq



Test conditions unless otherwise noted: $V_d=50V$, $I_{dq}=500mA$, $PW=2000\mu S$, $DC=20\%$, $P_{in}=46dBm$, Frequency 1= 2.7 GHz, Frequency 2 = 2.9 GHz, Frequency 3 = 3.1 GHz, $T_{base}=25^\circ C$

Figure 82: 2f v. Pout v. Temperature, F1

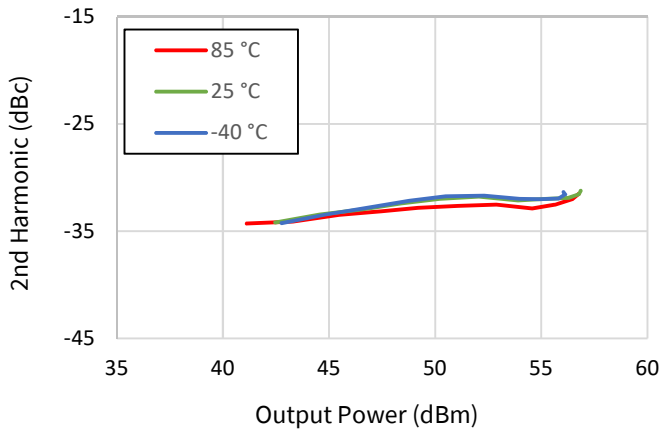


Figure 83: 2f v. Pout v. Vd, F1

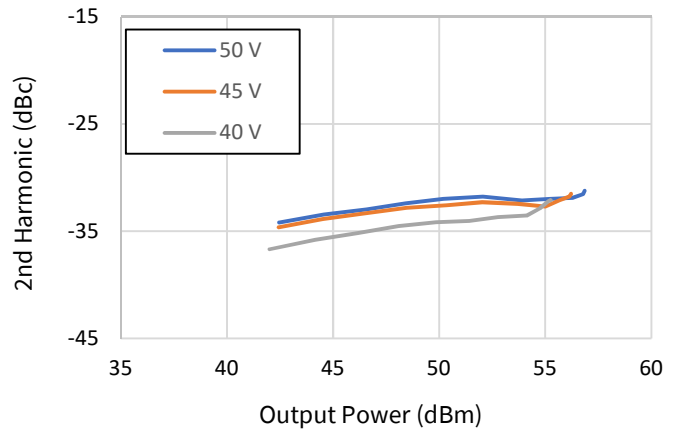


Figure 84: 2f v. Pout v. Temperature, F2

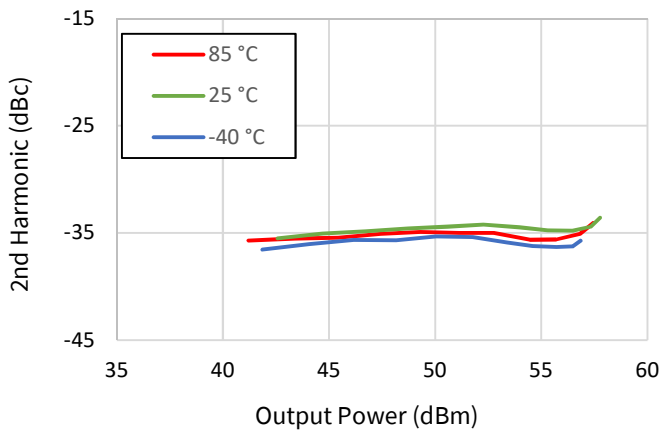


Figure 85: 2f v. Pout v. Vd, F2

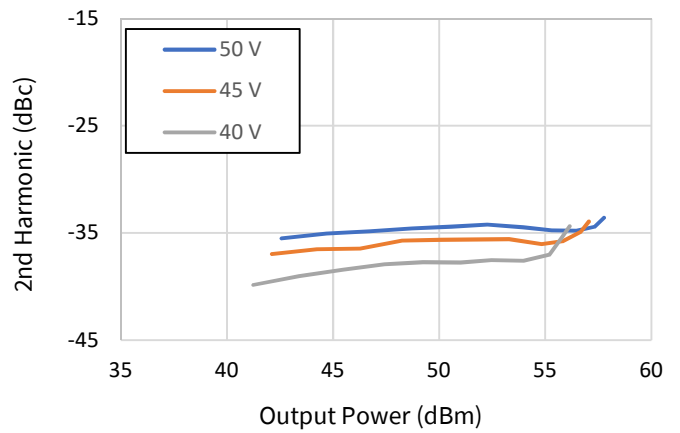


Figure 86: 2f v. Pout v. Temperature, F3

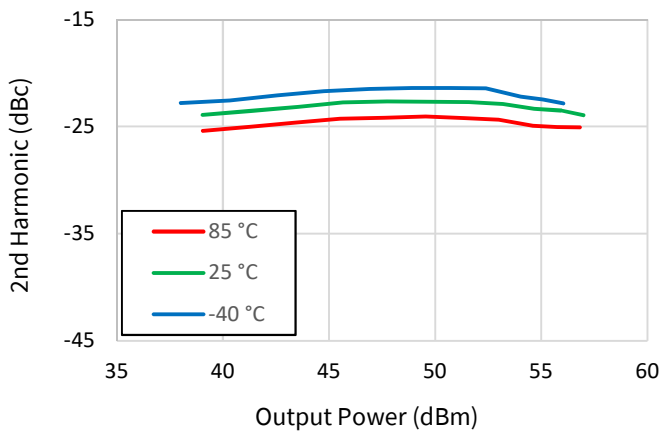
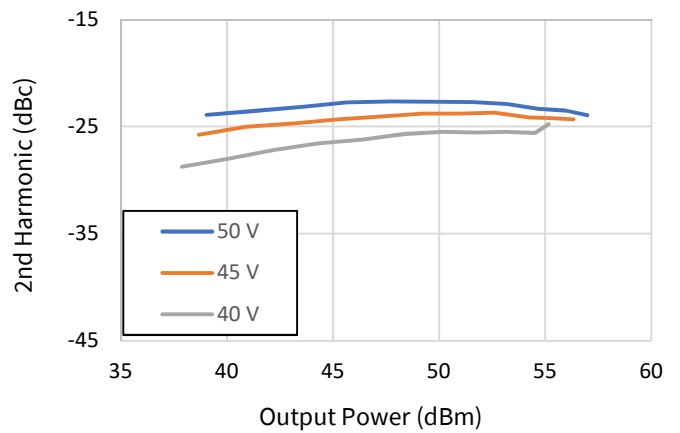


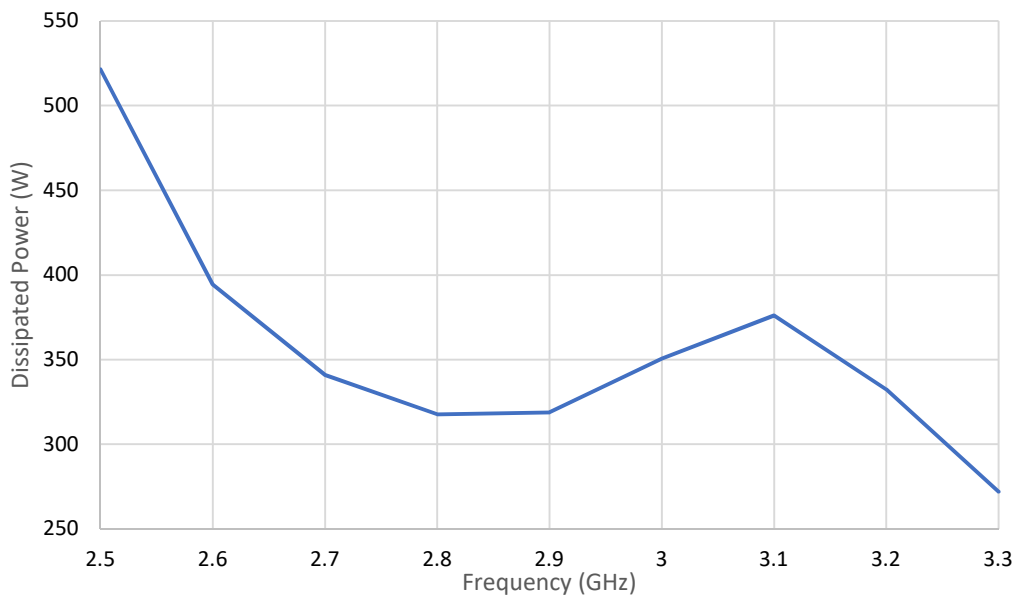
Figure 87: 2f v. Pout v. Vd, F3



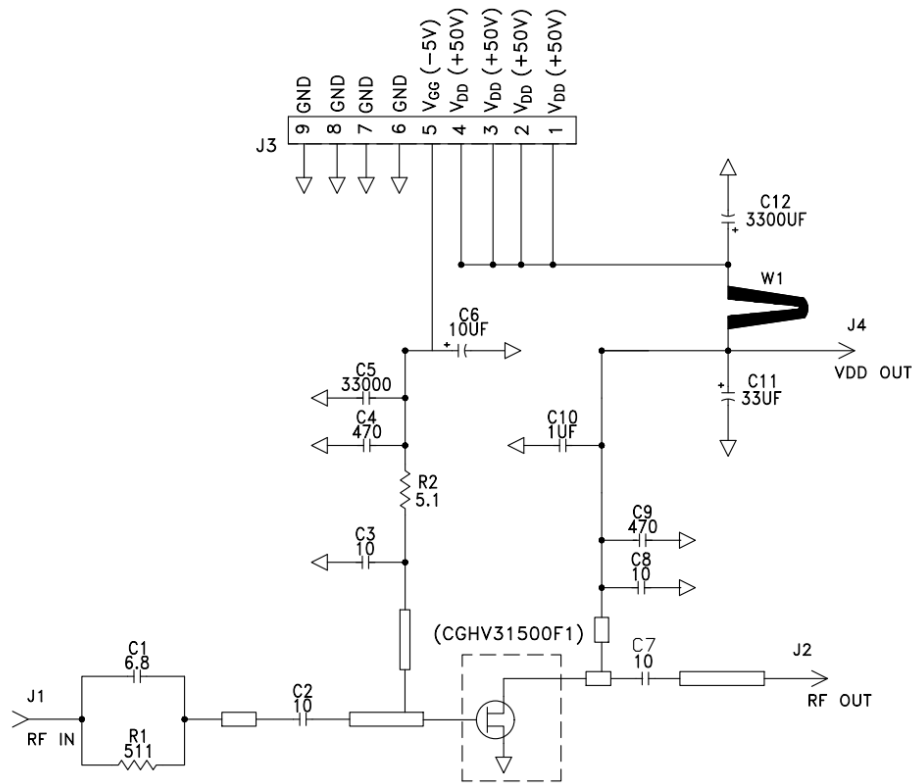
Thermal Characteristics

Parameter	Symbol	Value	Operating Conditions
Operating Junction Temperature	T_J	212	Freq = 2.9 GHz, $V_d = 50$ V, $I_{dq} = 500$ mA, $I_{drive} = 18.2$ A , $P_{in} = 46$ dBm, $P_{out} = 57.9$ dBm, $P_{diss} = 319$ W, $T_{case} = 85$ C, PW = 2000 μ S, DC = 20%
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.4	

Power Dissipation v. Frequency (Tcase = 85C)



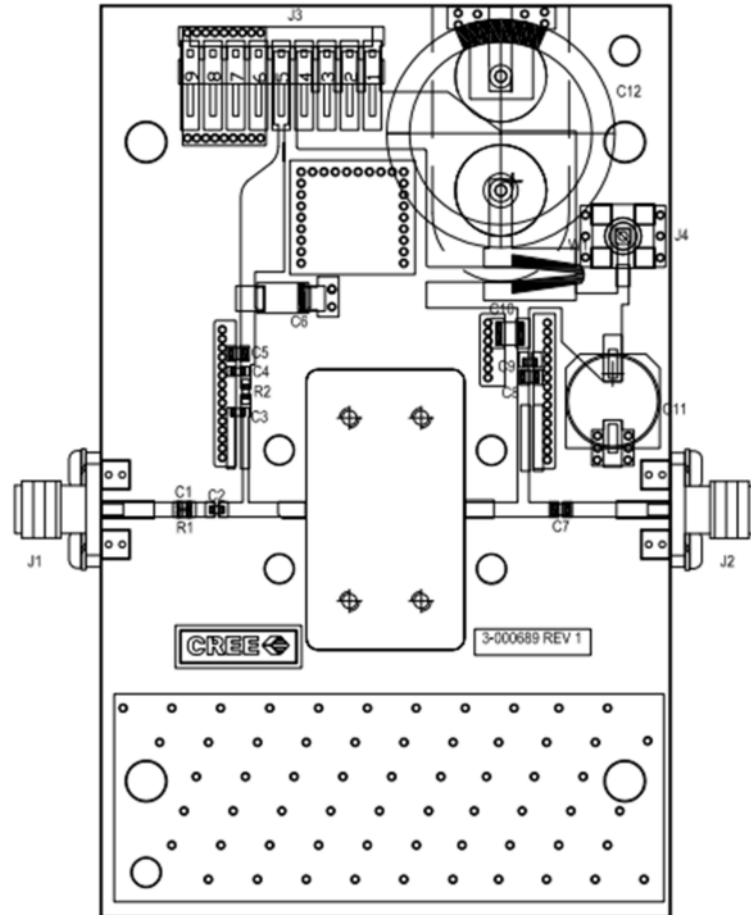
CGHV31500F1-AMP Schematic Drawing



CGHV31500F1-AMP Bill of Materials

Reference Designator	Description	Qty
R1	RES, 511, OHM, +/- 1%, 1/16W, 0603	1
R2	RES, 5.1, OHM, +/- 1%, 1/16W, 0603	1
C1	CAP, 6.8pF, +/-0.25%, 250V, 0603	1
C2, C7, C8	CAP, 10.0pF, +/-1%, 250V, 0805	3
C3	CAP, 10.0pF, +/-5%, 250V, 0603	1
C4, C9	CAP, 470pF, 5%, 100V, 0603, X	2
C5	CAP, 33000 pF, 0805, 100V, X7R	1
C6	CAP, 10uF 16V TANTALUM	1
C10	CAP, 1.0uF, 100V, 10%, X7R, 1210	1
C11	CAP, 33uF, 20%, G CASE	1
C12	CAP, 3300uF, +/-20%, 100V, ELECTROLYTIC	1
J1, J2	CONN, SMA, PANEL MOUNT JACK, FL	2
J3	HEADER, RT>PLZ, 0.1CEN LK 9POS	1
J4	CONNECTOR; SMB, Straight, JACK, SMD	1
W1	CABLE, 18 AWG, 4.2	1
	PCB, RO4350, 2.5 X 4.0 X 0.030	1
Q1	CGHV31500F1	1

CGHV31500F1-AMP Evaluation Board Assembly Drawing



Bias On Sequence

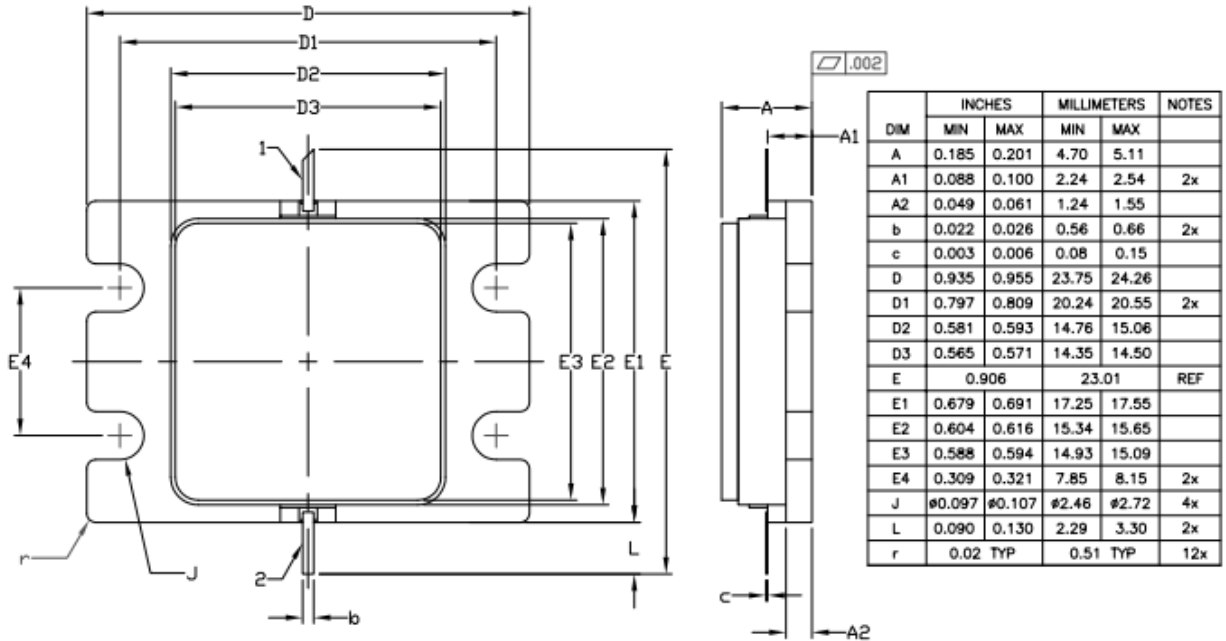
1. Ensure RF is turned-off
2. Apply pinch-off voltage of -5 V to the gate (V_g)
3. Apply nominal drain voltage (V_d)
4. Adjust V_g to obtain desired quiescent drain current (I_{dq})
5. Apply RF

Bias Off Sequence

1. Turn RF off
2. Apply pinch-off to the gate ($V_g = -5V$)
3. Turn off drain voltage (V_d)
4. Turn off gate voltage (V_g)

Product Dimensions (Package 440226)

- NOTES: (UNLESS OTHERWISE SPECIFIED)
1. INTERPRET DRAWING IN ACCORDANCE WITH ANSI Y14.5M-2009
 2. ADHESIVE FROM LID MAY EXTEND A MAXIMUM OF .020 BEYOND EDGE OF LID
 3. LID MAY BE MISALIGNED TO THE BODY OF PACKAGE BY A MAXIMUM OF .008 IN ANY DIRECTION
 4. ALL PLATED SURFACES ARE GOLD OVER NICKEL





PIN	DESC.
1	GATE/RFIN
2	DRAIN/RFOUT
3	SOURCE/FLANGE

Electrostatic Discharge (ESD) Classification

Parameter	Symbol	Class	Test Methodology
Human body Model	HBM		JEDEC JESD22 A114-D
Charge Device Model	CDM		JEDEC JESD22 C101-C

Product Ordering Information

Part Number	Description	MOQ Increment	Image
CGHV31500F1	Packaged GaN HEMT	1 Each	
CGHV31500F1-AMP	Evaluation Board w/ GaN HEMT	1 Each	

For more information, please contact:

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