

● **Electrical characteristics** ($T_a = 25^\circ\text{C}$)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	-	-	± 10	μA	$V_{GS}=\pm 8\text{V}, V_{DS}=0\text{V}$
Drain-source breakdown voltage	$V_{(BR)DSS}$	50	-	-	V	$I_D=1\text{mA}, V_{GS}=0\text{V}$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS}=50\text{V}, V_{GS}=0\text{V}$
Gate threshold voltage	$V_{GS(th)}$	0.3	-	0.8	V	$V_{DS}=10\text{V}, I_D=1\text{mA}$
Static drain-source on-state resistance	$R_{DS(on)}^*$	-	1.6	2.2	Ω	$I_D=200\text{mA}, V_{GS}=4.5\text{V}$
		-	1.7	2.4		$I_D=200\text{mA}, V_{GS}=2.5\text{V}$
		-	2.0	2.8		$I_D=200\text{mA}, V_{GS}=1.5\text{V}$
		-	2.2	3.3		$I_D=100\text{mA}, V_{GS}=1.2\text{V}$
		-	3.0	9.0		$I_D=10\text{mA}, V_{GS}=0.9\text{V}$
Forward transfer admittance	$ Y_{fs} ^*$	0.2	-	-	S	$I_D=200\text{mA}, V_{DS}=10\text{V}$
Input capacitance	C_{iss}	-	26	-	pF	$V_{DS}=10\text{V}$
Output capacitance	C_{oss}	-	6	-	pF	$V_{GS}=0\text{V}$
Reverse transfer capacitance	C_{rss}	-	3	-	pF	$f=1\text{MHz}$
Turn-on delay time	$t_{d(on)}^*$	-	5	-	ns	$I_D=100\text{mA}, V_{DD}=25\text{V}$
Rise time	t_r^*	-	8	-	ns	$V_{GS}=4.5\text{V}$
Turn-off delay time	$t_{d(off)}^*$	-	17	-	ns	$R_L=250\Omega$
Fall time	t_f^*	-	43	-	ns	$R_G=10\Omega$

*Pulsed

● **Body diode characteristics** (Source-Drain) ($T_a = 25^\circ\text{C}$)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward Voltage	V_{SD}^*	-	-	1.2	V	$I_S=200\text{mA}, V_{GS}=0\text{V}$

*Pulsed

● Electrical characteristics curves

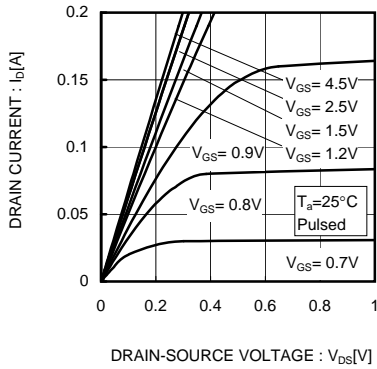


Fig.1 Typical Output Characteristics(I)

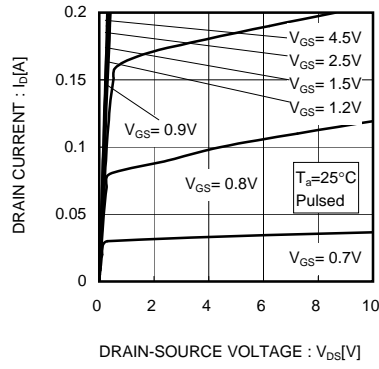


Fig.2 Typical Output Characteristics(II)

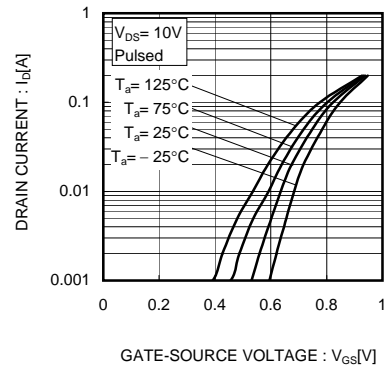


Fig.3 Typical Transfer Characteristics

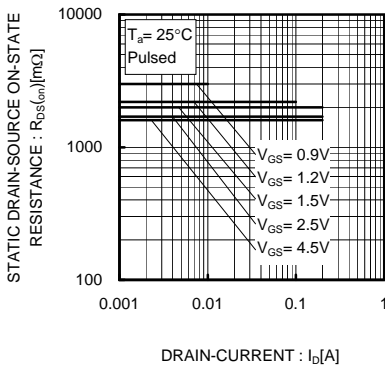


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current(I)

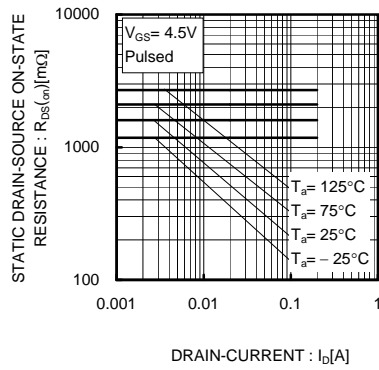


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current(II)

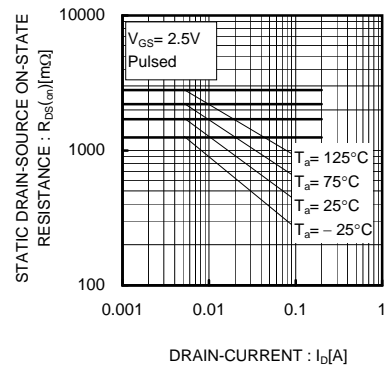


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current(III)

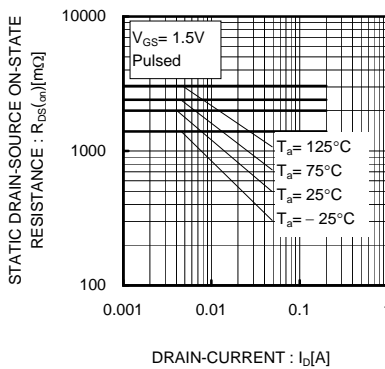


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current(IV)

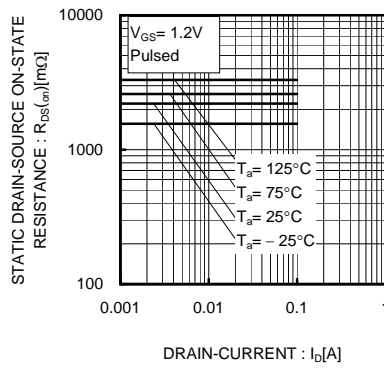


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current(V)

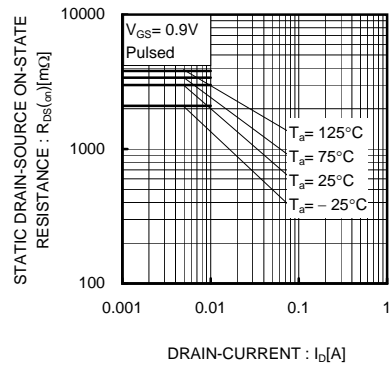


Fig.9 Static Drain-Source On-State Resistance vs. Drain Current(VI)

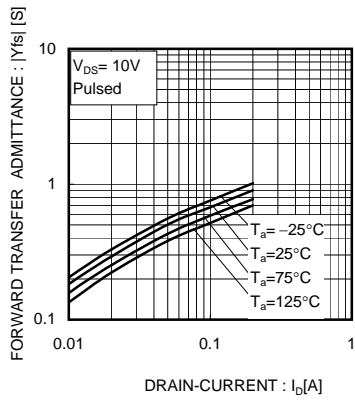


Fig.10 Forward Transfer Admittance vs. Drain Current

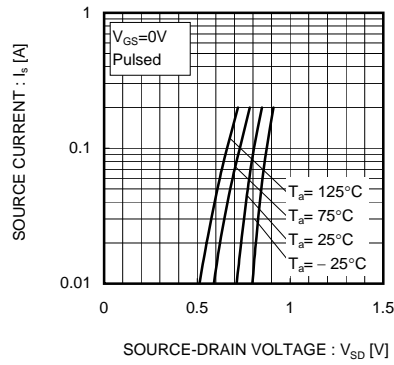


Fig.11 Reverse Drain Current vs. Source-Drain Voltage

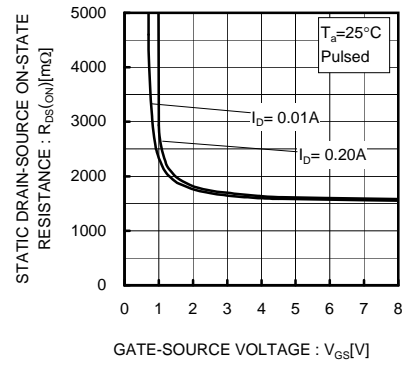


Fig.12 Static Drain-Source On-State Resistance vs. Gate Source Voltage

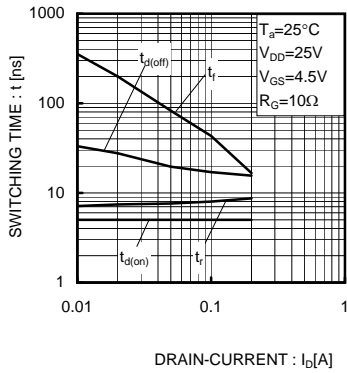


Fig.13 Switching Characteristics

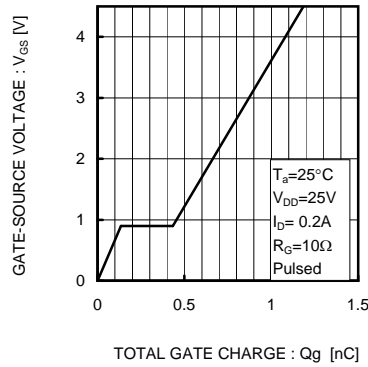


Fig.14 Typical Capacitance vs. Drain-Source Voltage

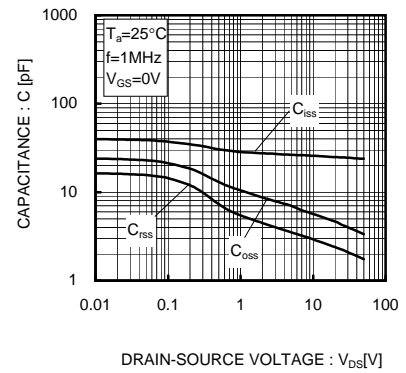


Fig.15 Typical Capacitance vs. Drain-Source Voltage

● Measurement circuits

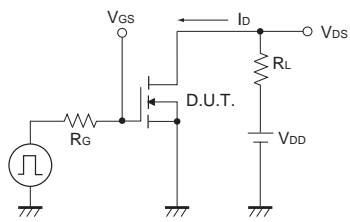


Fig.1-1 Switching Time Measurement Circuit

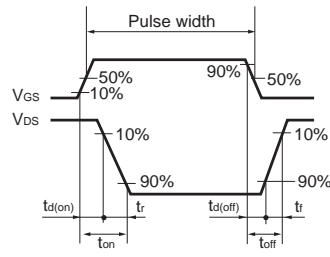


Fig.1-2 Switching Waveforms

● Notice

This product might cause chip aging and breakdown under the large electrified environment. Please consider to design ESD protection circuit.

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