Voltage Regulator – Adjustable Output, Positive

1.5 A

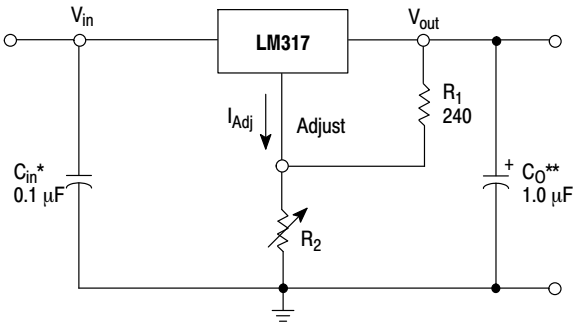
LM317, NCV317

The LM317 is an adjustable 3−terminal positive voltage regulator capable of supplying in excess of 1.5 A over an output voltage range of 1.2 V to 37 V. This voltage regulator is exceptionally easy to use and requires only two external resistors to set the output voltage. Further, it employs internal current limiting, thermal shutdown and safe area compensation, making it essentially blow−out proof.

The LM317 serves a wide variety of applications including local, on card regulation. This device can also be used to make a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM317 can be used as a precision current regulator.

Features

- Output Current in Excess of 1.5 A
- Output Adjustable between 1.2 V and 37 V
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting Constant with Temperature
- Output Transistor Safe−Area Compensation
- Floating Operation for High Voltage Applications
- Eliminates Stocking many Fixed Voltages
- Available in Surface Mount D^{2}PAK−3, and Standard 3−Lead Transistor Package
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

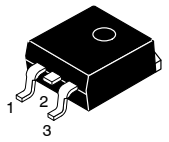


* C_{in} is required if regulator is located an appreciable distance from power supply filter.
** C_O is not needed for stability, however, it does improve transient response.

$$V_{out} = 1.25\ V\left(1 + \frac{R_2}{R_1}\right) + I_{Adj}R_2$$

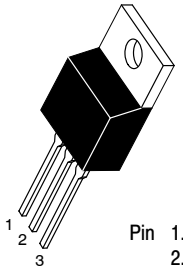
Since I_{Adj} is controlled to less than 100 μA, the error associated with this term is negligible in most applications.

Figure 1. Standard Application



D^{2}PAK−3
D2T SUFFIX
CASE 936

Heatsink surface (shown as terminal 4 in case outline drawing) is connected to Pin 2.



TO−220
T SUFFIX
CASE 221AB

Pin 1. Adjust
2. V_{out}
3. V_{in}

Heatsink surface connected to Pin 2.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 10 of this data sheet.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input−Output Voltage Differential	V_I-V_O	−0.3 to 40	Vdc
Power Dissipation			
Case 221A			
T_A = +25°C	P_D	Internally Limited	W
Thermal Resistance, Junction−to−Ambient	θ_{JA}	65	°C/W
Thermal Resistance, Junction−to−Case	θ_{JC}	5.0	°C/W
Case 936 (D^2PAK−3)			
T_A = +25°C	P_D	Internally Limited	W
Thermal Resistance, Junction−to−Ambient	θ_{JA}	70	°C/W
Thermal Resistance, Junction−to−Case	θ_{JC}	5.0	°C/W
Operating Junction Temperature Range	T_J	−55 to +150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ELECTRICAL CHARACTERISTICS

(V_I-V_O = 5.0 V; I_O = 0.5 A for D2T and T packages; $T_J = T_{low}$ to T_{high} (Note 1); I_{max} and P_{max} (Note 2); unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Line Regulation (Note 3), T_A = +25°C, 3.0 V ≤ V_I-V_O ≤ 40 V	1	Reg_{line}	–	0.01	0.04	%/V
Load Regulation (Note 3), T_A = +25°C, 10 mA ≤ I_O ≤ I_{max}	2	Reg_{load}				
V_O ≤ 5.0 V			–	5.0	25	mV
V_O ≥ 5.0 V			–	0.1	0.5	% V_O
Thermal Regulation, T_A = +25°C (Note 4), 20 ms Pulse	–	Reg_{therm}	–	0.03	0.07	% V_O/W
Adjustment Pin Current	3	I_{Adj}	–	50	100	μA
Adjustment Pin Current Change, 2.5 V ≤ V_I-V_O ≤ 40 V, 10 mA ≤ I_L ≤ I_{max}, P_D ≤ P_{max}	1, 2	ΔI_{Adj}	–	0.2	5.0	μA
Reference Voltage, 3.0 V ≤ V_I-V_O ≤ 40 V, 10 mA ≤ I_O ≤ I_{max}, P_D ≤ P_{max}	3	V_{ref}	1.2	1.25	1.3	V
Line Regulation (Note 3), 3.0 V ≤ V_I-V_O ≤ 40 V	1	Reg_{line}	–	0.02	0.07	%/V
Load Regulation (Note 3), 10 mA ≤ I_O ≤ I_{max}	2	Reg_{load}				
V_O ≤ 5.0 V			–	20	70	mV
V_O ≥ 5.0 V			–	0.3	1.5	% V_O
Temperature Stability (T_{low} ≤ T_J ≤ T_{high})	3	T_S	–	0.7	–	% V_O
Minimum Load Current to Maintain Regulation (V_I-V_O = 40 V)	3	I_{Lmin}	–	3.5	10	mA
Maximum Output Current	3	I_{max}				A
V_I-V_O ≤ 15 V, P_D ≤ P_{max}, T Package			1.5	2.2	–	
V_I-V_O = 40 V, P_D ≤ P_{max}, T_A = +25°C, T Package			0.15	0.4	–	
RMS Noise, % of V_O, T_A = +25°C, 10 Hz ≤ f ≤ 10 kHz	–	N	–	0.003	–	% V_O
Ripple Rejection, V_O = 10 V, f = 120 Hz (Note 5)	4	RR				dB
Without C_{Adj}			–	65	–	
C_{Adj} = 10 μF			66	80	–	
Thermal Shutdown (Note 6)	–	–	–	180	–	°C
Long−Term Stability, $T_J = T_{high}$ (Note 7), T_A = +25°C for Endpoint Measurements	3	S	–	0.3	1.0	%/1.0 kHrs.
Thermal Resistance Junction−to−Case, T Package	–	$R_{\theta JC}$	–	5.0	–	°C/W

1. T_{low} to T_{high} = 0° to +125°C, for LM317T, D2T. T_{low} to T_{high} = −40° to +125°C, for LM317BT, BD2T, T_{low} to T_{high} = −55° to +150°C, for NCV317BT, BD2T.
2. I_{max} = 1.5 A, P_{max} = 20 W
3. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.
4. Power dissipation within an IC voltage regulator produces a temperature gradient on the die, affecting individual IC components on the die. These effects can be minimized by proper integrated circuit design and layout techniques. Thermal Regulation is the effect of these temperature gradients on the output voltage and is expressed in percentage of output change per watt of power change in a specified time.
5. C_{Adj}, when used, is connected between the adjustment pin and ground.
6. Thermal characteristics are not subject to production test.
7. Since Long−Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.

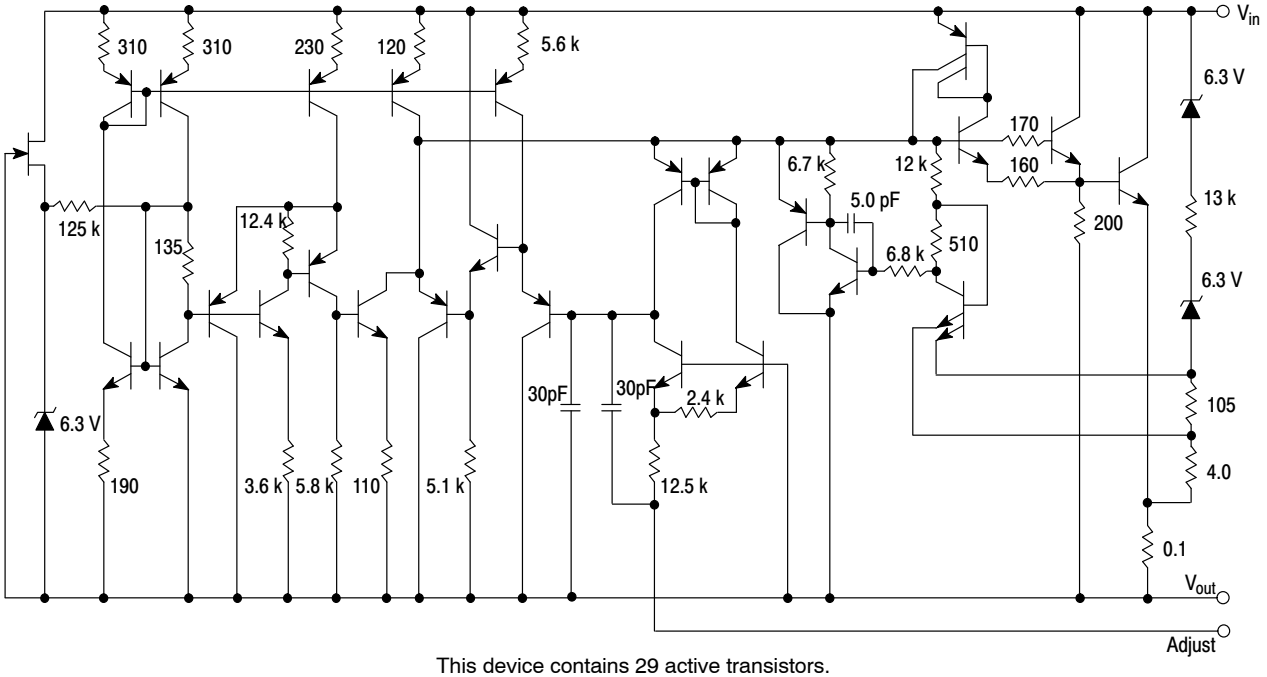


Figure 2. Representative Schematic Diagram

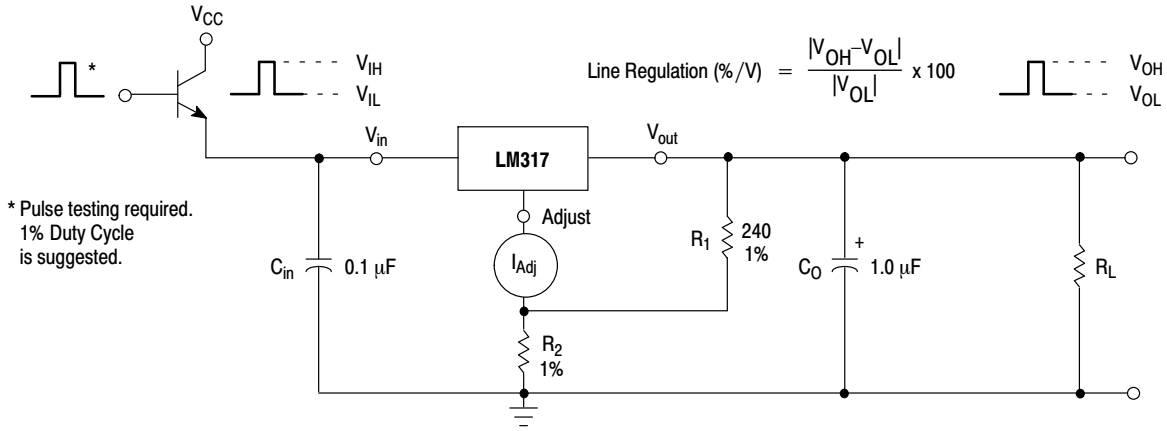


Figure 3. Line Regulation and ΔI_{Adj}/Line Test Circuit

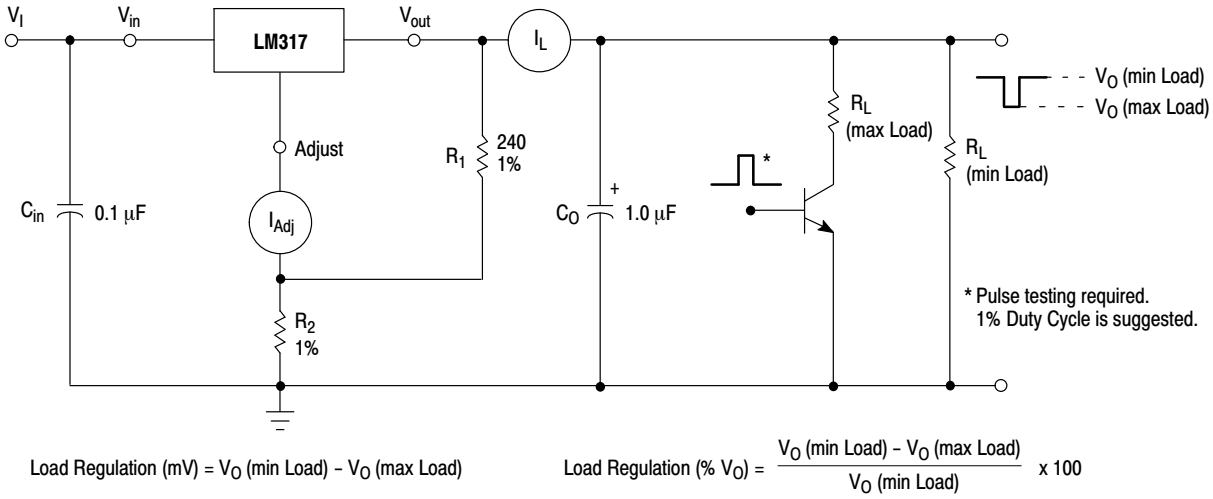


Figure 4. Load Regulation and ΔI_{Adj}/Load Test Circuit

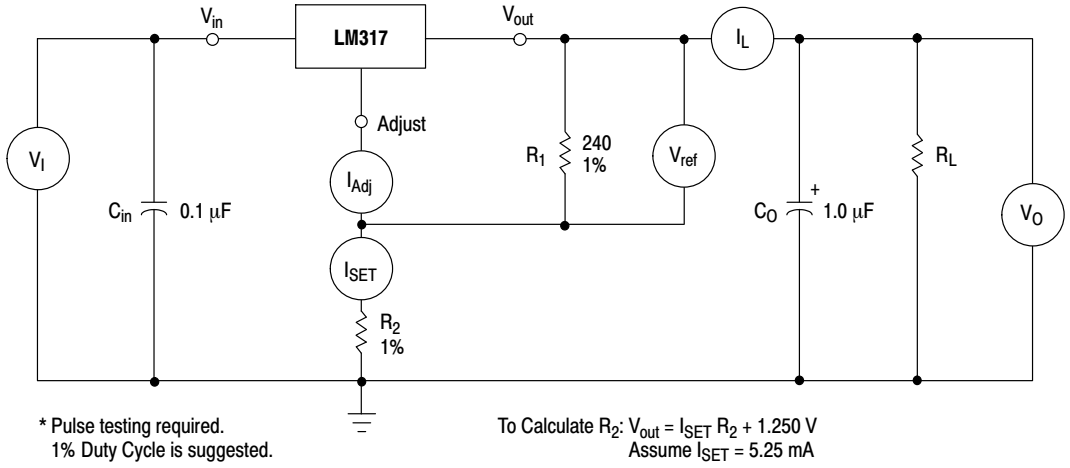


Figure 5. Standard Test Circuit

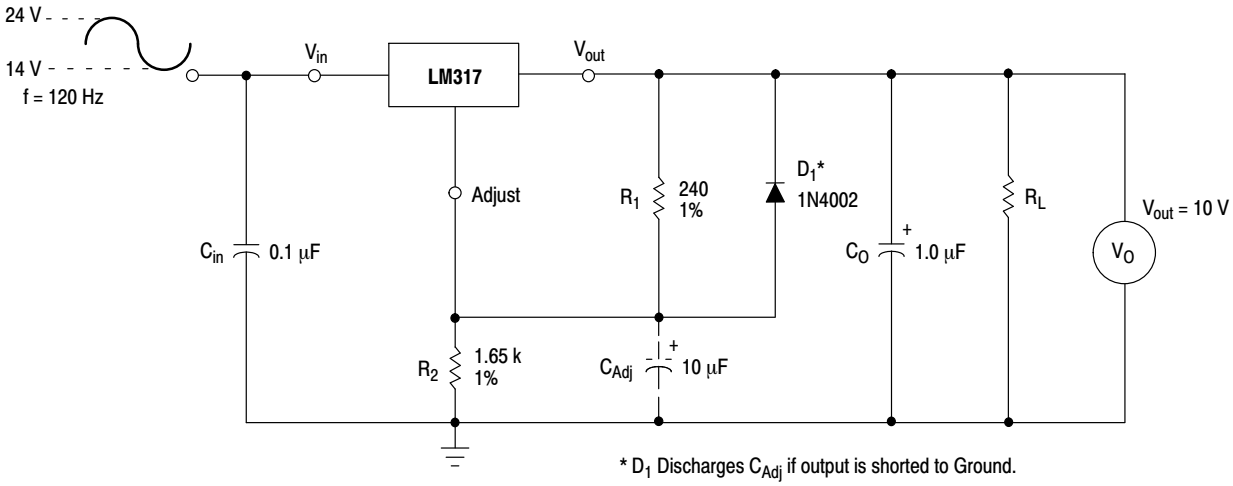


Figure 6. Ripple Rejection Test Circuit

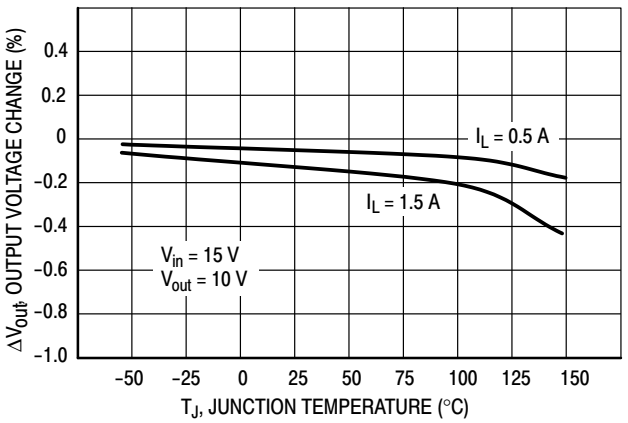


Figure 7. Load Regulation

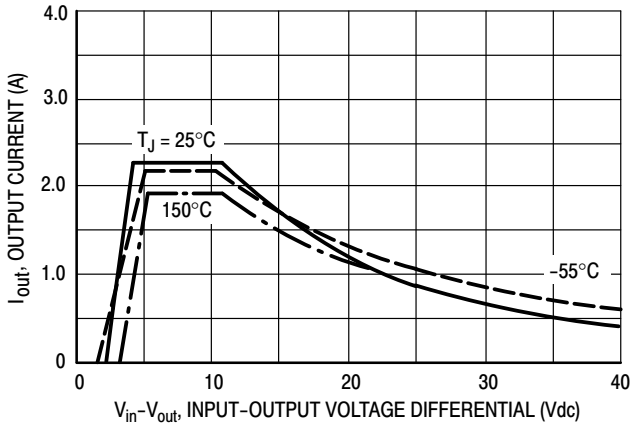


Figure 8. Current Limit

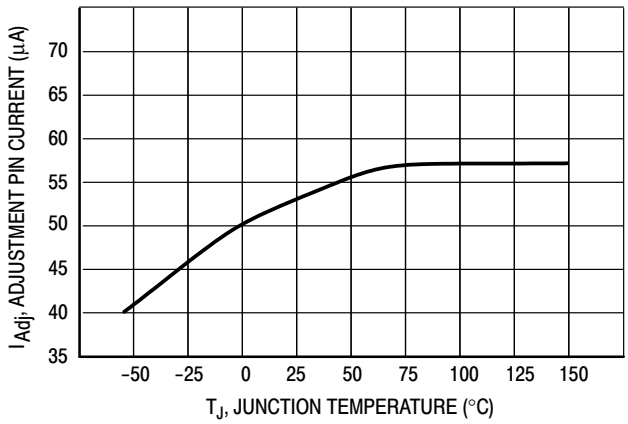


Figure 9. Adjustment Pin Current

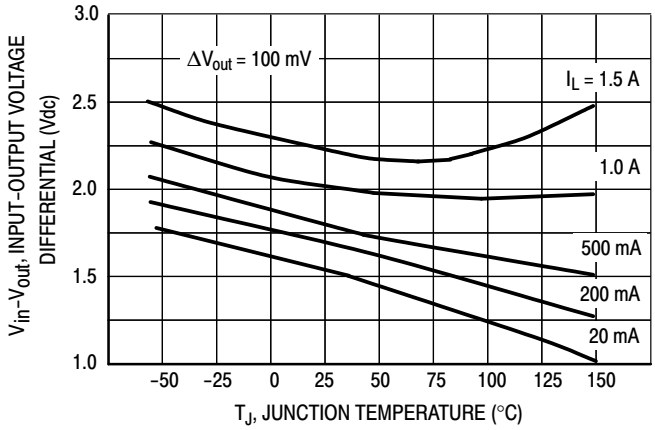


Figure 10. Dropout Voltage

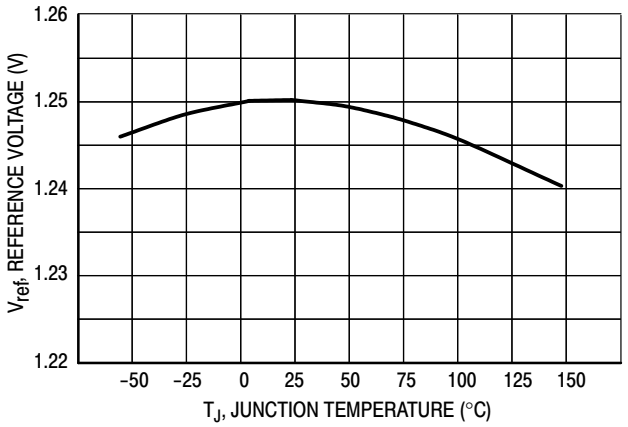


Figure 11. Temperature Stability

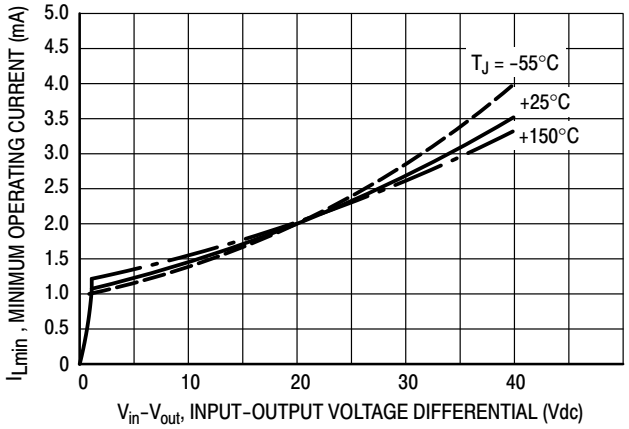


Figure 12. Minimum Operating Current

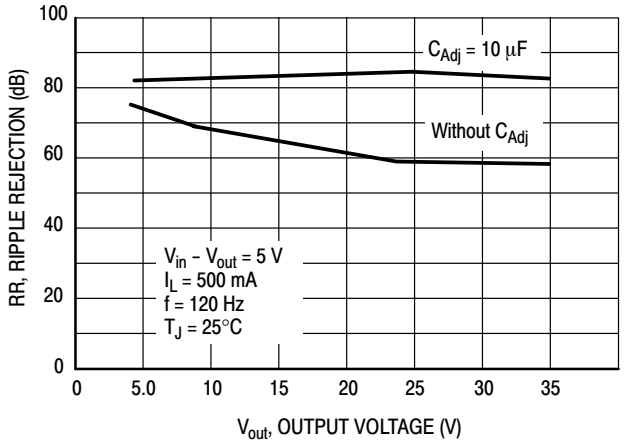


Figure 13. Ripple Rejection versus Output Voltage

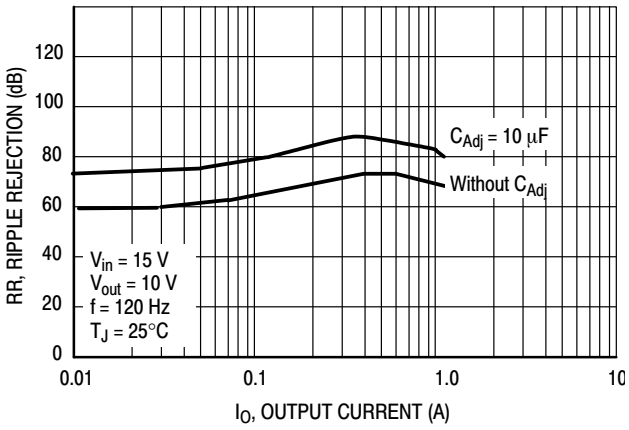


Figure 14. Ripple Rejection versus Output Current

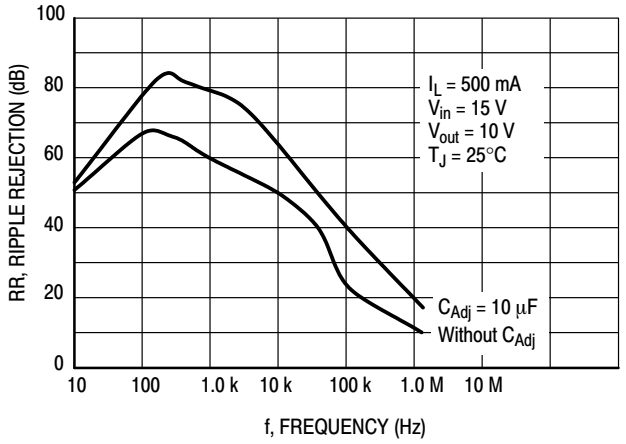


Figure 15. Ripple Rejection versus Frequency

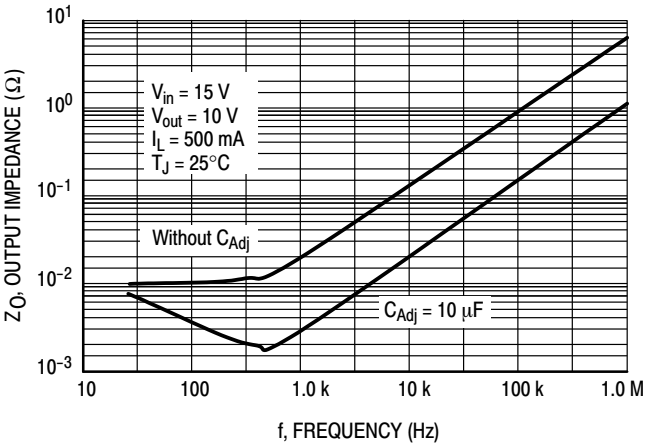


Figure 16. Output Impedance

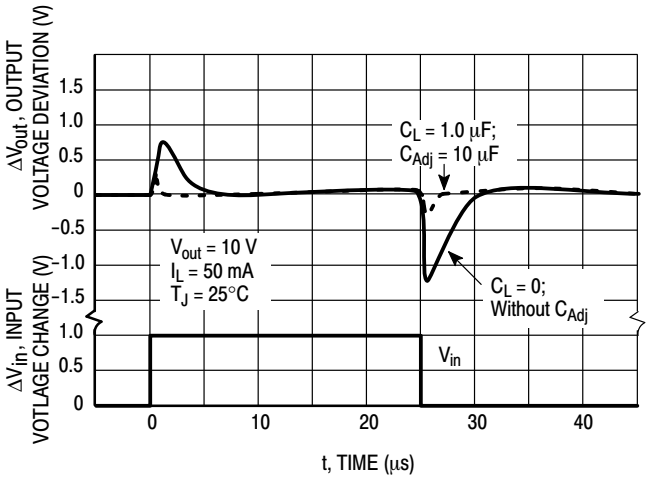


Figure 17. Line Transient Response

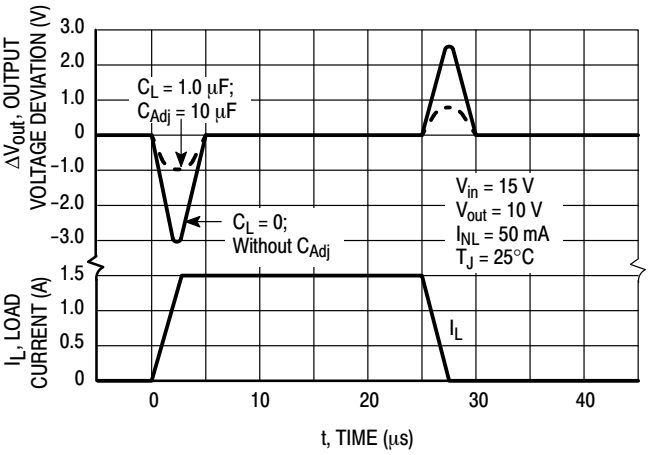


Figure 18. Load Transient Response

APPLICATIONS INFORMATION

Basic Circuit Operation

The LM317 is a 3−terminal floating regulator. In operation, the LM317 develops and maintains a nominal 1.25 V reference (V_{ref}) between its output and adjustment terminals. This reference voltage is converted to a programming current (I_{PROG}) by R_1 (see Figure 17), and this constant current flows through R_2 to ground.

The regulated output voltage is given by:

$$V_{out} = V_{ref}\left(1 + \frac{R_2}{R_1}\right) + I_{Adj}R_2$$

Since the current from the adjustment terminal (I_{Adj}) represents an error term in the equation, the LM317 was designed to control I_{Adj} to less than 100 μA and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will rise.

Since the LM317 is a floating regulator, it is only the voltage differential across the circuit which is important to performance, and operation at high voltages with respect to ground is possible.

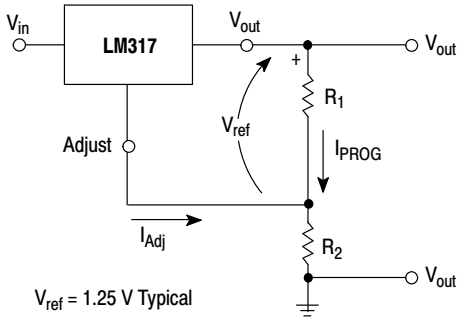


Figure 19. Basic Circuit Configuration

Load Regulation

The LM317 is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R_1) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R_2 can be returned near the load ground to provide remote ground sensing and improve load regulation.

External Capacitors

A 0.1 μF disc or 1.0 μF tantalum input bypass capacitor (C_{in}) is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor (C_{Adj}) prevents ripple from being amplified as the output voltage is increased. A 10 μF capacitor should improve ripple rejection about 15 dB at 120 Hz in a 10 V application.

Although the LM317 is stable with no output capacitance, like any feedback circuit, certain values of external capacitance can cause excessive ringing. An output capacitance (C_O) in the form of a 1.0 μF tantalum or 25 μF aluminum electrolytic capacitor on the output swamps this effect and insures stability.

Protection Diodes

When external capacitors are used with any IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 18 shows the LM317 with the recommended protection diodes for output voltages in excess of 25 V or high capacitance values (C_O > 25 μF, C_{Adj} > 10 μF). Diode D_1 prevents C_O from discharging thru the IC during an input short circuit. Diode D_2 protects against capacitor C_{Adj} discharging through the IC during an output short circuit. The combination of diodes D_1 and D_2 prevents C_{Adj} from discharging through the IC during an input short circuit.

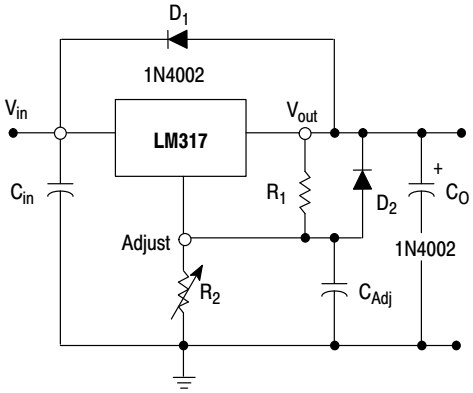


Figure 20. Voltage Regulator with Protection Diodes

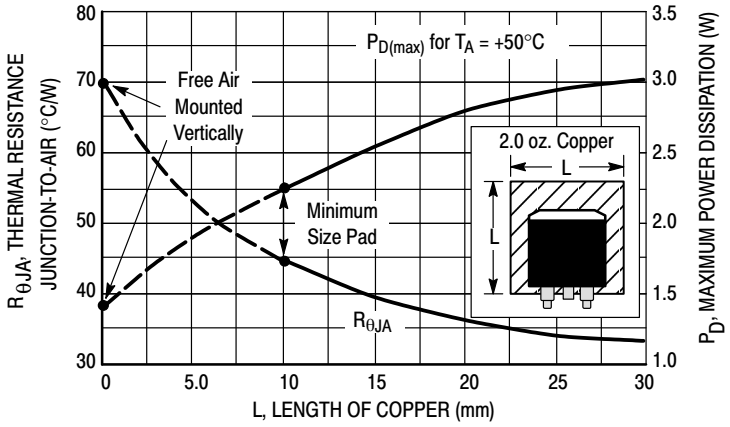


Figure 21. D²PAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

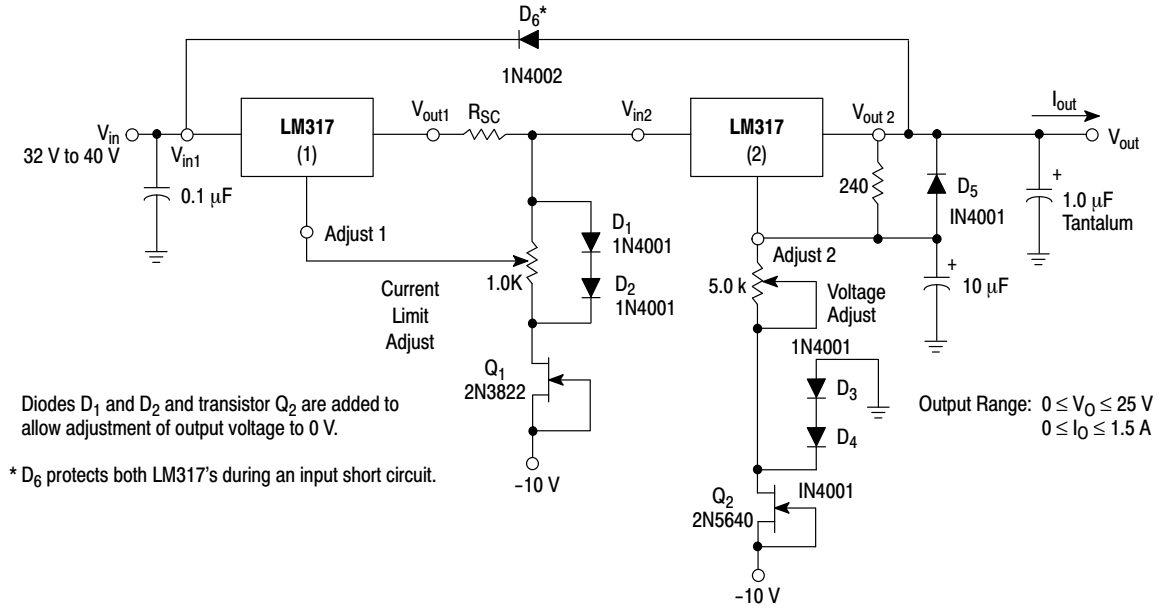


Figure 22. "Laboratory" Power Supply with Adjustable Current Limit and Output Voltage

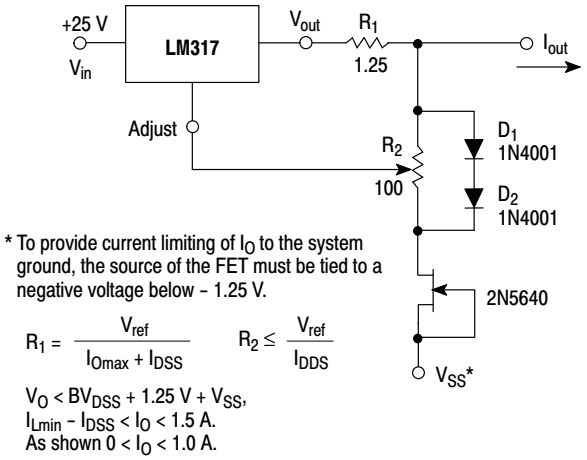


Figure 23. Adjustable Current Limiter

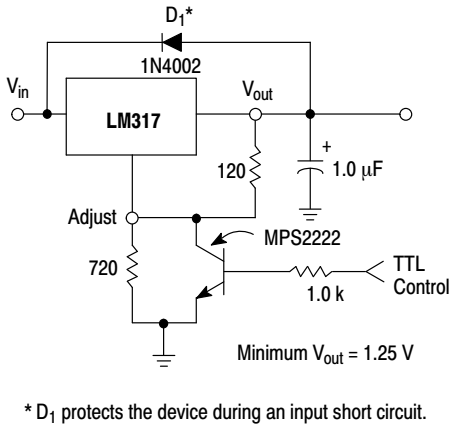


Figure 24. 5.0 V Electronic Shutdown Regulator

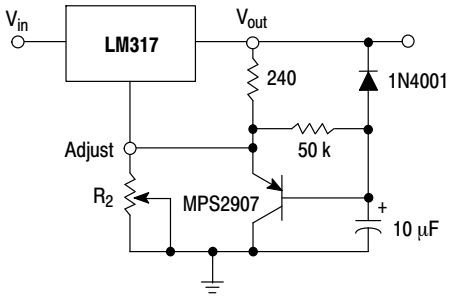


Figure 25. Slow Turn−On Regulator

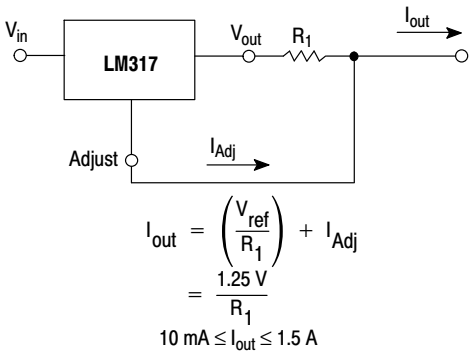


Figure 26. Current Regulator

ORDERING INFORMATION

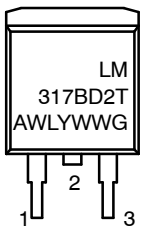
Device	Operating Temperature Range	Package	Shipping†
LM317BD2TG	T_J = −40° to +125°C	D^2PAK−3 (Pb−Free)	50 Units / Rail
LM317BD2TR4G		D^2PAK−3 (Pb−Free)	800 Tape & Reel
LM317BTG		TO−220 (Pb−Free)	50 Units / Rail
LM317D2TG	T_J = 0° to +125°C	D^2PAK−3 (Pb−Free)	50 Units / Rail
LM317D2TR4G		D^2PAK−3 (Pb−Free)	800 Tape & Reel
LM317TG		TO−220 (Pb−Free)	50 Units / Rail
NCV317BD2TG*	T_J = −55° to +150°C	D^2PAK−3 (Pb−Free)	50 Units / Rail
NCV317BD2TR4G*		D^2PAK−3 (Pb−Free)	800 Tape & Reel
NCV317BTG*		TO−220 (Pb−Free)	50 Units / Rail

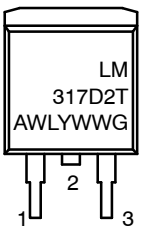
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

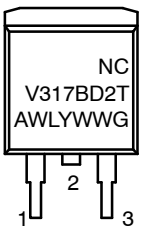
*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

MARKING DIAGRAMS

D^2PAK−3
D2T SUFFIX
CASE 936







TO−220
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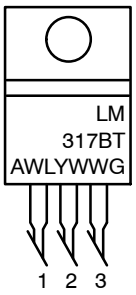
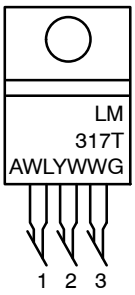
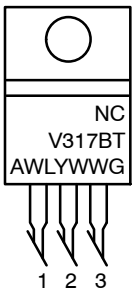
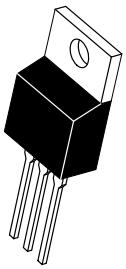
CASE 221A







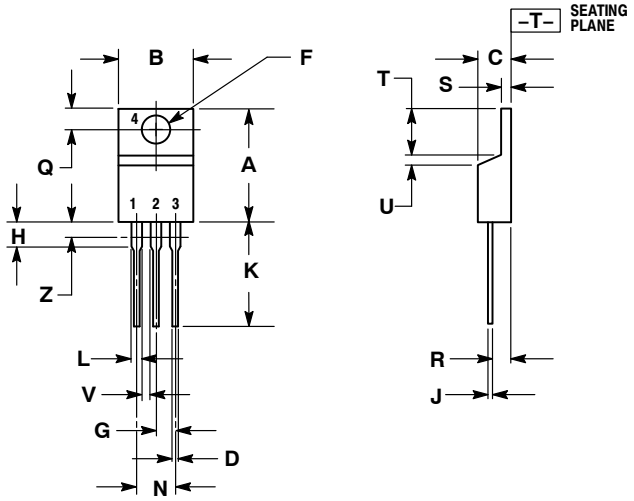
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package



SCALE 1:1

TO−220, SINGLE GAUGE
CASE 221AB−01
ISSUE A

DATE 16 NOV 2010



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.
4. PRODUCT SHIPPED PRIOR TO 2008 HAD DIMENSIONS S = 0.045 − 0.055 INCHES (1.143 − 1.397 MM)

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.020	0.024	0.508	0.61
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR
4. EMITTER

STYLE 3:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 4:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 6:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 7:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

STYLE 8:
PIN 1. CATHODE
2. ANODE
3. EXTERNAL TRIP/DELAY
4. ANODE

STYLE 9:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 10:
PIN 1. GATE
2. SOURCE
3. DRAIN
4. SOURCE

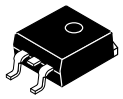
STYLE 11:
PIN 1. DRAIN
2. SOURCE
3. GATE
4. SOURCE

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

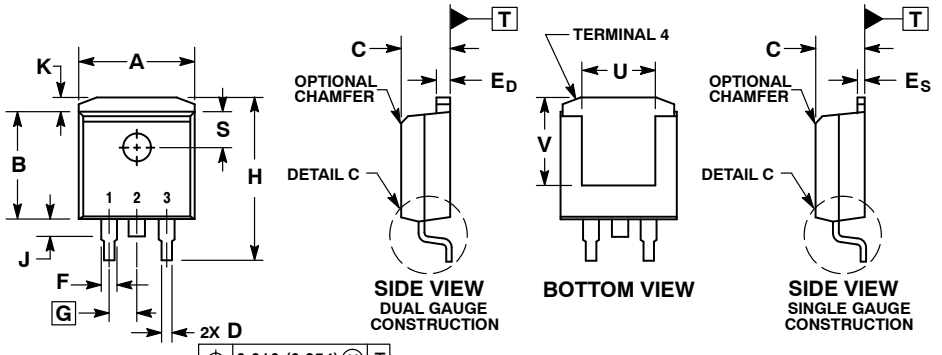
ON Semiconductor®

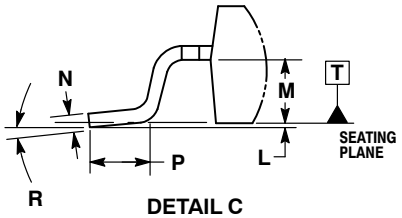
D²PAK
CASE 936−03
ISSUE E

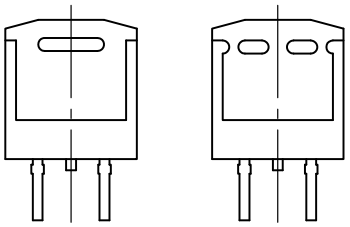
DATE 29 SEP 2015



SCALE 1:1





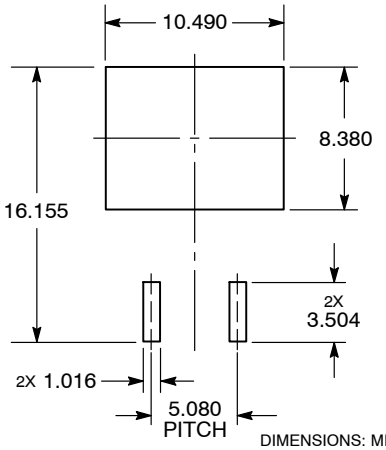


BOTTOM VIEW
OPTIONAL CONSTRUCTIONS

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCHES.
3. TAB CONTOUR OPTIONAL WITHIN DIMENSIONS A AND K.
4. DIMENSIONS U AND V ESTABLISH A MINIMUM MOUNTING SURFACE FOR TERMINAL 4.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.025 (0.635) MAXIMUM.
6. SINGLE GAUGE DESIGN WILL BE SHIPPED AFTER FPCN EXPIRATION IN OCTOBER 2011.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.386	0.403	9.804	10.236
B	0.356	0.368	9.042	9.347
C	0.170	0.180	4.318	4.572
D	0.026	0.036	0.660	0.914
E_D	0.045	0.055	1.143	1.397
E_S	0.018	0.026	0.457	0.660
F	0.051 REF		1.295 REF	
G	0.100 BSC		2.540 BSC	
H	0.539	0.579	13.691	14.707
J	0.125 MAX		3.175 MAX	
K	0.050 REF		1.270 REF	
L	0.000	0.010	0.000	0.254
M	0.088	0.102	2.235	2.591
N	0.018	0.026	0.457	0.660
P	0.058	0.078	1.473	1.981
R	0°	8°	0°	8°
S	0.116 REF		2.946 REF	
U	0.200 MIN		5.080 MIN	
V	0.250 MIN		6.350 MIN	

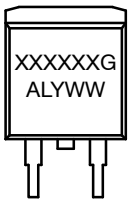
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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