

**FEATURES:**

- Enhanced N channel FET with no inherent diode to Vcc
- 5Ω bidirectional switches connect inputs to outputs
- Zero propagation delay, zero added ground bounce
- Ultra low power with 0.2μA typical Icc
- Undershoot clamp diodes on all switch and control inputs
- Two enables control five bits each
- Available in QSOP and TSSOP packages

**APPLICATIONS:**

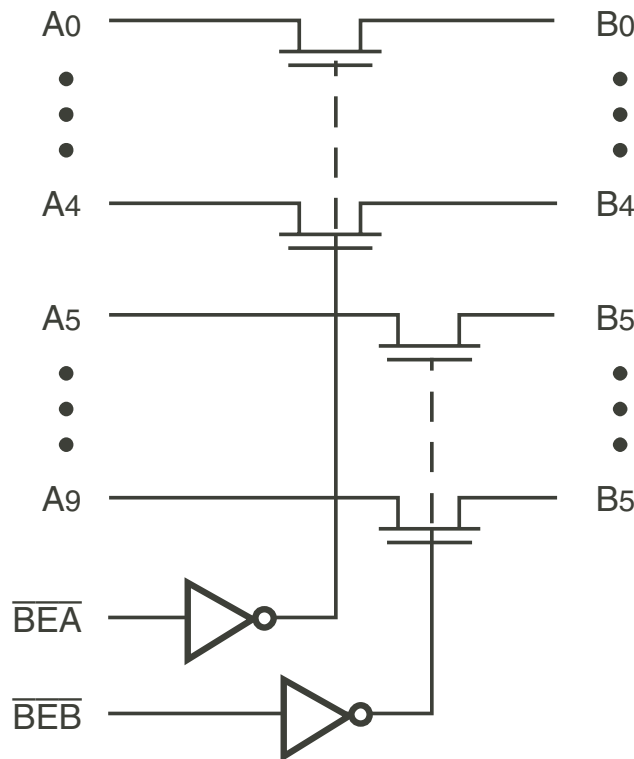
- Hot-swapping, hot-docking
- Voltage translation (5V to 3.3V)
- Power Conservation
- Capacitance reduction and isolation
- Bus Isolation
- Clock Gating

**DESCRIPTION:**

The QS3L384 provides a set of ten high-speed CMOS TTL-compatible bus switches. The low ON resistance of the QS3L384 allows inputs to be connected to outputs without adding propagation delay and without generating additional ground bounce noise. The Bus Enable ( $\overline{BE}$ ) signals turn the switches on. Two bus enable signals are provided, one for each of the upper and lower five bits of the two 10-bit buses.

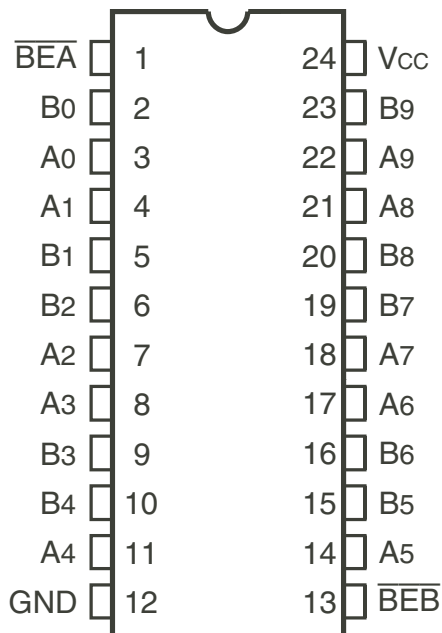
The QS3L384 is characterized for operation at -40°C to +85°C.

**FUNCTIONAL BLOCK DIAGRAM**



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## PIN CONFIGURATION



QSOP/TSSOP  
TOP VIEW

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Description	Max	Unit
VTERM <sup>(2)</sup>	Supply Voltage to Ground	-0.5 to +7	V
VTERM <sup>(3)</sup>	DC Switch Voltage V <sub>s</sub>	-0.5 to +7	V
VTERM <sup>(3)</sup>	DC Input Voltage V <sub>IN</sub>	-0.5 to +7	V
VAC	AC Input Voltage (pulse width ≤20ns)	-3	V
I <sub>OUT</sub>	DC Output Current	120	mA
P <sub>MAX</sub>	Maximum Power Dissipation (T <sub>A</sub> = 85°C)	0.5	W
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C

### NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V<sub>CC</sub> terminals.
- All terminals except V<sub>CC</sub>.

## CAPACITANCE (T<sub>A</sub> = +25°C, f = 1MHz, V<sub>IN</sub> = 0V, V<sub>OUT</sub> = 0V)

Pins	Typ.	Max. <sup>(1)</sup>	Unit
Control Inputs	3	5	pF
Quickswitch Channels (Switch OFF)	5	7	pF

### NOTE:

- This parameter is guaranteed but not production tested.

## PIN DESCRIPTION

Pin Names	I/O	Description
A <sub>0</sub> - A <sub>9</sub>	I/O	Bus A
B <sub>0</sub> - B <sub>9</sub>	I/O	Bus B
$\overline{\text{BEA}}$ , $\overline{\text{BEB}}$	I	Bus Switch Enable

## FUNCTION TABLE<sup>(1)</sup>

$\overline{\text{BEA}}$	$\overline{\text{BEB}}$	B <sub>0</sub> - A <sub>4</sub>	B <sub>5</sub> - B <sub>9</sub>	Function
H	H	Hi-Z	Hi-Z	Disconnect
L	H	A <sub>0</sub> - A <sub>4</sub>	Hi-Z	Connect
H	L	Hi-Z	A <sub>5</sub> - A <sub>9</sub>	Connect
L	L	A <sub>0</sub> - A <sub>4</sub>	A <sub>5</sub> - A <sub>9</sub>	Connect

### NOTE:

- H = HIGH Voltage Level  
L = LOW Voltage Level  
Z = High-Impedance

### DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

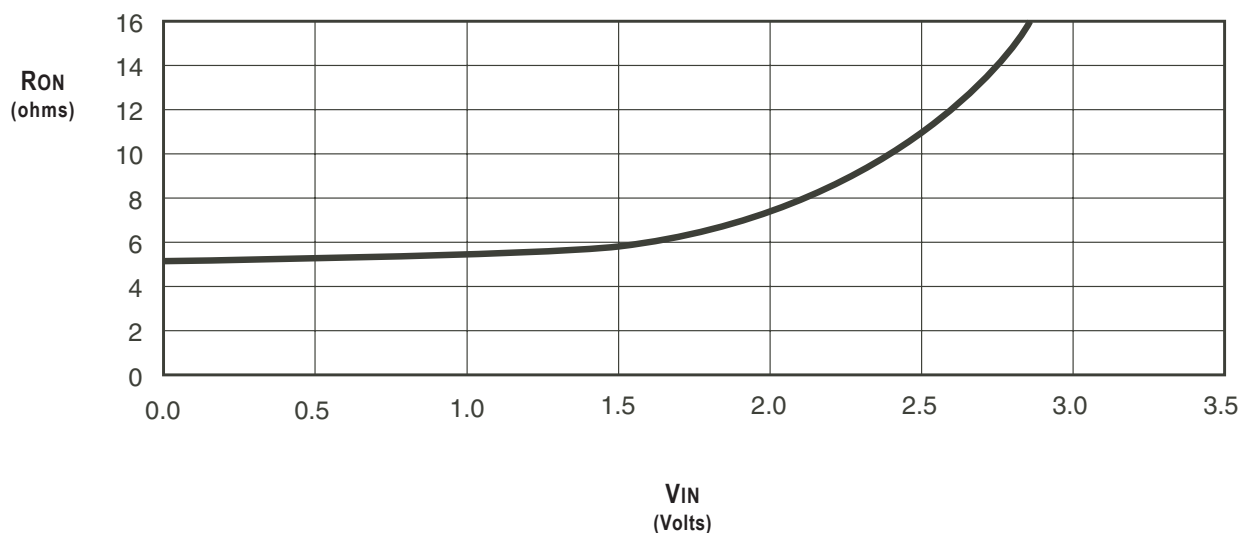
Industrial:  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = 5\text{V} \pm 5\%$

Symbol	Parameter	Test Conditions	Min.	Typ. <sup>(1)</sup>	Max.	Unit
$V_{IH}$	Input HIGH Voltage	Guaranteed Logic HIGH for Control Pins	2	—	—	V
$V_{IL}$	Input LOW Voltage	Guaranteed Logic LOW for Control Pins	—	—	0.8	V
$I_{IN}$	Input Leakage Current (Control Inputs)	$0\text{V} \leq V_{IN} \leq V_{CC}$	—	—	$\pm 1$	$\mu\text{A}$
$I_{OZ}$	Off-State Current (Hi-Z)	$0\text{V} \leq V_{OUT} \leq V_{CC}$	—	$\pm 0.01$	$\pm 1$	$\mu\text{A}$
RON	Switch ON Resistance	$V_{CC} = \text{Min.}, V_{IN} = 0\text{V}, I_{ON} = 30\text{mA}$	—	5	7	$\Omega$
		$V_{CC} = \text{Min.}, V_{IN} = 2.4\text{V}, I_{ON} = 15\text{mA}$	—	10	15	
VP	Pass Voltage <sup>(2)</sup>	$V_{IN} = V_{CC} = 5\text{V}, I_{OUT} = -5\mu\text{A}$	3.7	4	4.2	V

**NOTES:**

1. Typical values are at  $V_{CC} = 5\text{V}$  and  $T_A = 25^{\circ}\text{C}$ .
2. Pass voltage is guaranteed but not production tested.

### TYPICAL ON RESISTANCE vs VIN AT VCC = 5V



## POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Typ.	Max.	Unit
I <sub>CCQ</sub>	Quiescent Power Supply Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = GND or V <sub>CC</sub> , f = 0	0.2	3	μA
ΔI <sub>CC</sub>	Power Supply Current per Input HIGH <sup>(2)</sup>	V <sub>CC</sub> = Max., V <sub>IN</sub> = 3.4V, f = 0	—	1.5	mA
I <sub>CCD</sub>	Dynamic Power Supply Current per MHz <sup>(3)</sup>	V <sub>CC</sub> = Max., A and B Pins Open, Control Inputs Toggling @ 50% Duty Cycle	—	0.25	mA/MHz

### NOTES:

- For conditions shown as Min. or Max., use the appropriate values specified under DC Electrical Characteristics.
- Per TTL-driven input (V<sub>IN</sub> = 3.4V, control inputs only). A and B pins do not contribute to ΔI<sub>CC</sub>.
- This current applies to the control inputs only and represents the current required to switch internal capacitance at the specified frequency. The A and B inputs generate no significant AC or DC currents as they transition. This parameter is guaranteed but not production tested.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

T<sub>A</sub> = -40°C to +85°C, V<sub>CC</sub> = 5V ± 5%

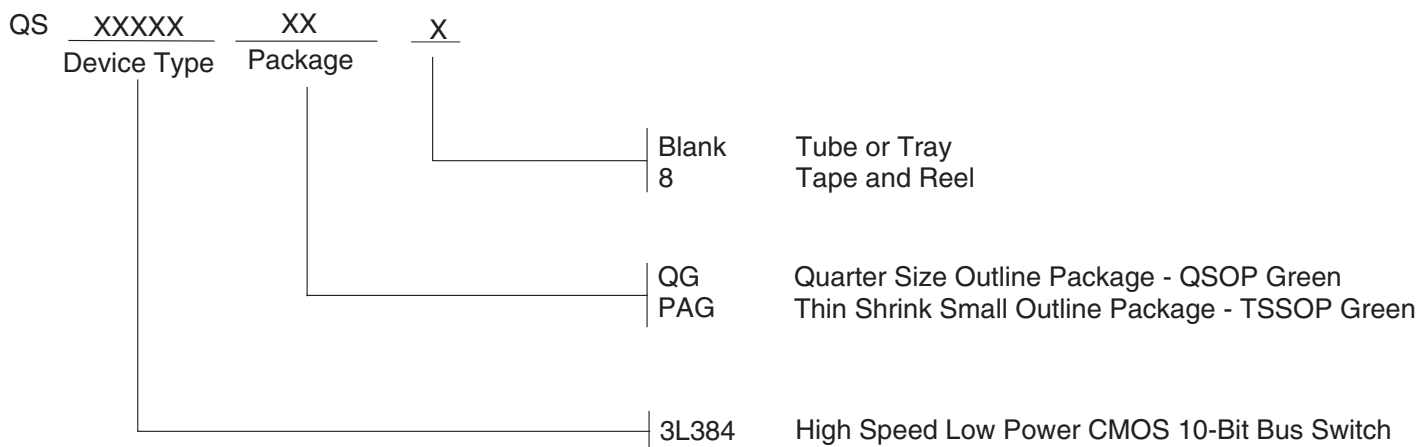
C<sub>LOAD</sub> = 50pF, R<sub>LOAD</sub> = 500Ω unless otherwise noted.

Symbol	Parameter	Min. <sup>(1)</sup>	Typ.	Max.	Unit
t <sub>PLH</sub> t <sub>PHL</sub>	Data Propagation Delay <sup>(2)</sup> Ax to Bx, Bx to Ax	—	—	0.25 <sup>(3)</sup>	ns
t <sub>PZL</sub> t <sub>PZH</sub>	Switch Turn-On Delay BEA, BEB to Ax, Bx	1.5	—	6.5	ns
t <sub>PLZ</sub> t <sub>PHZ</sub>	Switch Turn-Off Delay <sup>(2)</sup> BEA, BEB to Ax, Bx	1.5	—	5.5	ns

### NOTES:

- Minimums are guaranteed but not production tested.
- This parameter is guaranteed but not production tested.
- The bus switch contributes no propagation delay other than the RC delay of the ON resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25ns at C<sub>L</sub> = 50pF. Since this time constant is much smaller than the rise and fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch, when used in a system, is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

## ORDERING INFORMATION



## Datasheet Document History

01/28/13

Pg. 1, 5

Updated the Ordering Information by removing non green package version, the "IDT" notation and Adding Tape and Reel information.

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### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

### Contact Information

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