



## 400mA LOW NOISE, HIGH PSRR LINEAR VOLTAGE REGULATOR

### Typical Applications

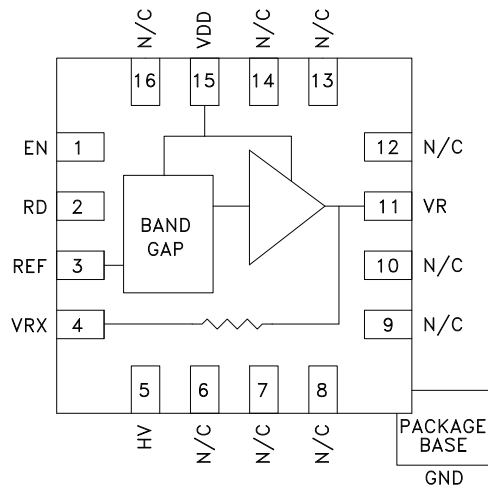
The HMC976LP3E is ideal for:

- Test Instrumentation
- Military Radios, Radar and ECM
- Basestation Infrastructure
- Ultra Low Noise Frequency Generation
- Fractional-N Synthesizer Supply
- Microwave VCO Supply
- Mixed-Signal Circuit Supply
- Low Noise Baseband Circuit Supply

### Features

- High Output Current: 400mA
- Low Dropout: 300mV at 400mA Output and  $V_R > 3V$
- Ultra Low Noise:  $3nV/\sqrt{Hz}$  at 10 kHz,  $6nV/\sqrt{Hz}$  at 1 kHz
- High Power Supply Rejection Ratio (PSRR):
  - <-60 dB at 1 kHz, <-30 dB at 1 MHz
- Adjustable Voltage Output:  $V_R$  1.8 to 5V at 400mA
- Designed to work with low ESR ceramic capacitors
- Low Power-Down Current: <1  $\mu A$
- Thermal Protection
- 16 Lead 3x3 mm SMT Package: 9mm<sup>2</sup>

### Functional Diagram



### General Description

The HMC976LP3E is a BiCMOS ultra low noise linear voltage regulator. The high Power Supply Rejection Ratio (PSRR) in the 0.1 MHz to 10 MHz range provides excellent rejection of any preceding switching regulator or other power supply noise. The voltage output is ideal for frequency generation subsystems including Hittite's broad line of PLLs with integrated VCOs.

The output voltage can be adjusted lower than the default value by using one external resistor. The output can be set to 5V by grounding the HV pin. The regulator can be powered down by the TTL-compatible Enable input. The HMC976LP3E is housed in a 3x3mm QFN SMT package.

**Table 1. Electrical Specifications,  $T_A = +25^\circ C$**

| Parameter                         | Conditions   | Min | Typ | Max | Units |
|-----------------------------------|--|-----|-----|-----|-------|
| Output Voltage $V_R$ (Default)    | $V_{dd} = 5.5V$ ; Maximum load current                         | 4.7 | 4.8 | 4.9 | V     |
| Output Voltage $V_R$ (5V setting) | $V_{dd} = 5.5V$ ; Maximum load current                         | 4.9 | 5   | 5.1 | V     |
| Output Voltage Tolerance          | $V_{dd} = 5.5V$ ; Maximum load current; Default and 5V setting |     |     | 2   | %     |
| Input Voltage Range (Default)     | Default output voltage configuration                           | 5.1 |     | 5.5 | V     |
| Input Voltage Range               | For $V_R > 3V^{[1]}$ $V_{DD} > V_R + 0.3V$                     | 3.3 |     | 5.5 | V     |
| Output Voltage Range $V_R$        | Set by external resistors.                                     | 1.8 |     | 5.1 | V     |

[1] See Absolute Maximum Ratings Table "Absolute Maximum Ratings"

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**Table 1. Electrical Specifications (Continued)**

| Parameter  | Conditions  | Min | Typ                                    | Max          | Units            |
|--|---|-----|--|--------------|------------------|
| Reference Voltage VREF   | Vdd = 5.5V; REF cannot source/sink external current   |     | 1.17                                   |              | V                |
| Output Current VR <sup>[1]</sup>   | T <sub>A</sub> = -40°C to +85°C   |     |  | 400          | mA               |
| Output Noise Spectral Density<br>10 Hz<br>100 Hz<br>1 kHz<br>10 kHz<br>100 kHz         | Vdd = 5.5V; VR = 5.0V<br>Measured on Application Schematic <sup>[3]</sup><br>Maximum Load Current |     | 4000<br>120<br>6<br>3<br>3             |              | nV/rtHz          |
| Integrated Output Noise 100 Hz to 100 kHz  | Vdd = 5.5V; VR = 5.0V <sup>[3]</sup>  |     | 1.5                                    |              | μVrms            |
| Load Regulation, VR  | Vdd = 5.5V; VR=5.0V   |     |  | 0.01         | % / mA           |
| PSRR<br>1 kHz<br>10 kHz<br>100 kHz<br>1 MHz<br>10 MHz<br>50 MHz                        | Vdd = 5.5V; VR=5.0V<br>Maximum load current   |     | -70<br>-65<br>-45<br>-35<br>-30<br>-20 |              | dB               |
| Output Voltage Variation vs. Package Base Temperature<br>25°C to 85°C<br>-40°C to 25°C | Vdd = 5.5V; VR=5.0V<br>Maximum load current   |     | 0.005<br>0.005                         | 0.01<br>0.01 | % / °C<br>% / °C |
| Current Consumption (I <sub>GND</sub> )  | Ven = Vdd = 5.5V;<br>Maximum Load Current   |     | 1.1                                    | 1.5          | mA               |
| Power Down Current   | Vdd = 5.5V; EN = Low; Output is floating (high - impedance) in Power-Down mode                    |     |  | 1            | μA               |
| Start-Up Transient Time  | 0 to 90% of final voltage<br>Vdd = 5.5V <sup>[3]</sup>  |     |  | 200          | ms               |
| Enable Input EN High Level   | Vdd ≥ VEN   | 2   |  | Vdd          | V                |
| Enable Input EN Low Level  | Vdd ≥ VEN   | 0   |  | 0.8          | V                |
| Output Load Capacitance <sup>[2]</sup>   | To guarantee stability, noise and PSRR performance <sup>[3]</sup>                                 | 4.7 |  |              | μF               |
| Thermal Protection Threshold Junction Temperature <sup>[4]</sup>                       | Junction Temperature Rising   | 115 | 130                                    |              | °C               |
| Thermal Protection Hysteresis  |   |     | 10                                     |              | °C               |

[1] The regulator does not include short-circuit protection circuitry. The outputs will withstand short-circuit conditions for a duration <10s. The thermal protection is not intended to be used as a short circuit protection

[2] HMC976LP3E was designed to work with low ESR ceramic capacitors connected to pin 4 VRX.

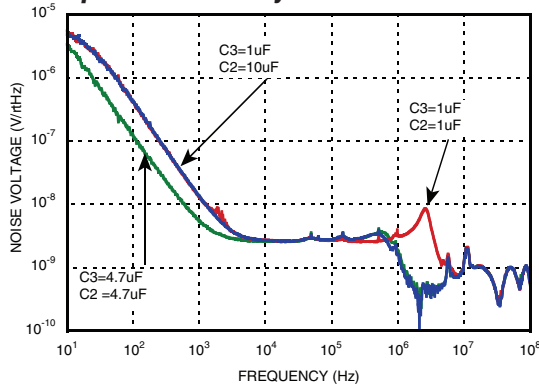
[3] See HMC976LP3E 5.0V User Application Schematic herein

[4] See figures 14,15, and 16

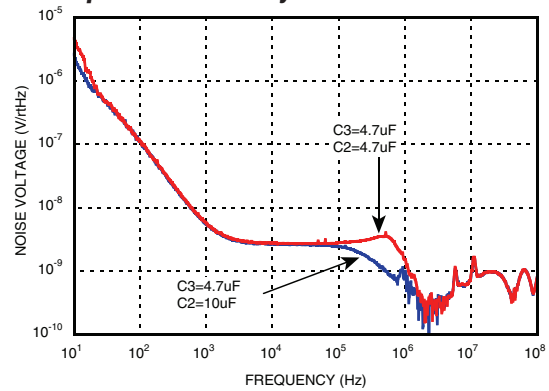


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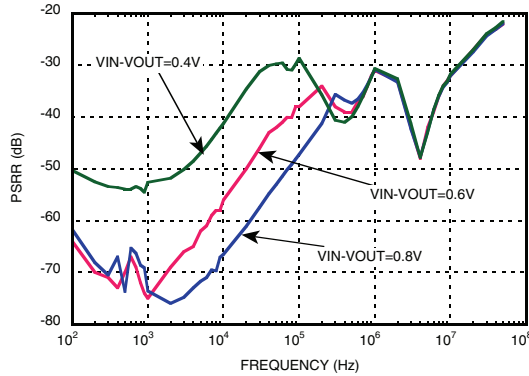
**Figure 1. Vout=5V Output Noise Spectral Density [1]**



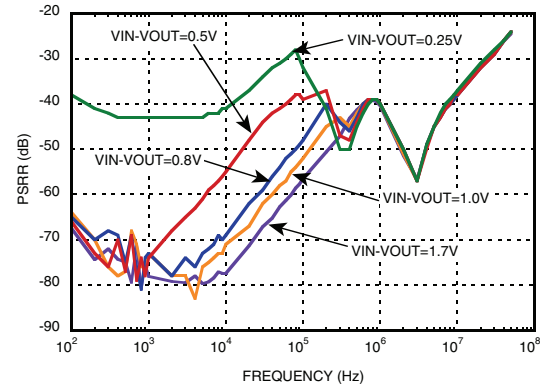
**Figure 2. Vout=3.3V Output Noise Spectral Density [2]**



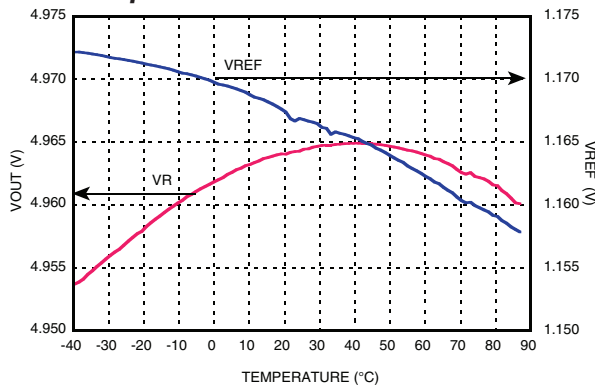
**Figure 3. Vout 4.8V PSRR vs. Vin-Vout [3]**



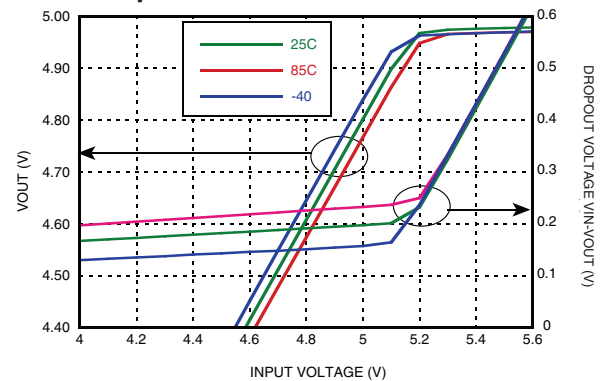
**Figure 4. Vout=3.3V PSRR vs. Vin-Vout [2]**



**Figure 5. Vout=5V and Vref vs. Temperature [1,4]**



**Figure 6. Vout=5V and Vref vs. Temperature [1,4]**



[1] VDD=5.5V,400mA Load see ["HMC976LP3E 5V User Application Schematic"](#)

[2] VDD=5.0V,400mA Load see ["HMC976LP3E 3.3V User Application Schematic"](#)

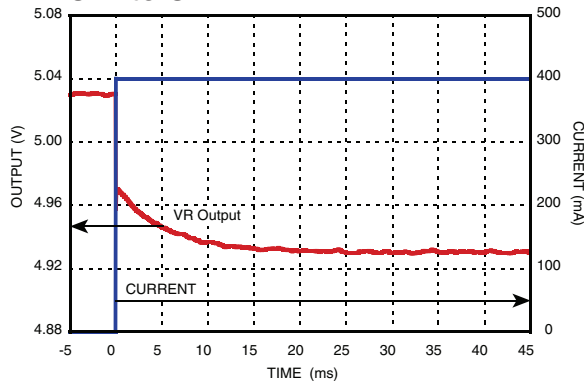
[3] VDD=5.5V,400mA Load see ["HMC976LP3E 4.8V User Application Schematic"](#)

[4] Temperature is the ambient temperature of the standard HMC976LP3E evaluation board, still air.

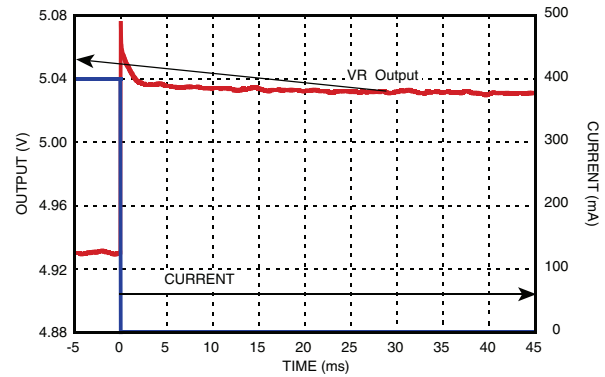


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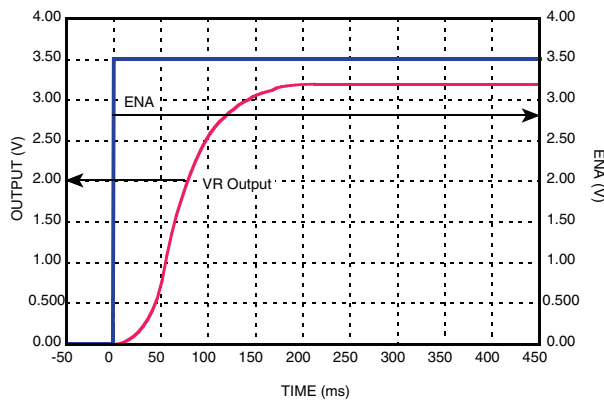
**Figure 7. Output Load Switched OFF to ON [1]**



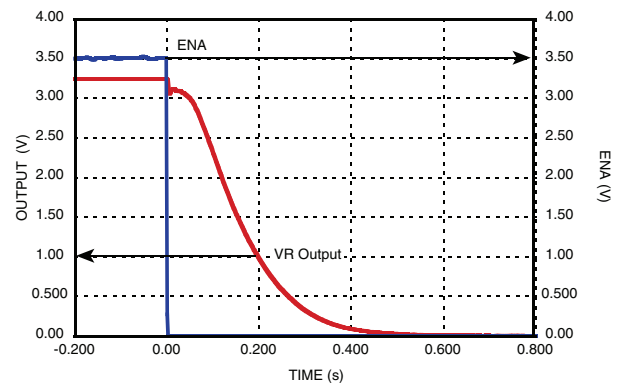
**Figure 8. Output Load Switched ON to OFF [1]**



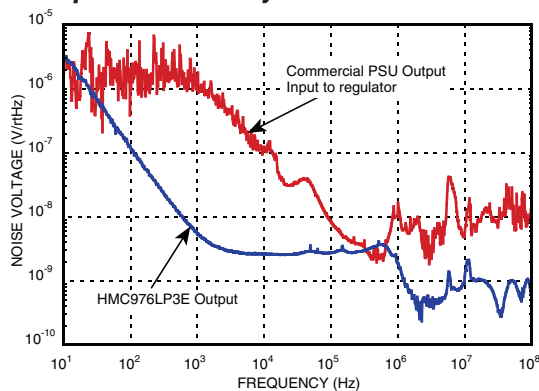
**Figure 9. Supply Turn-On Transient [2]**



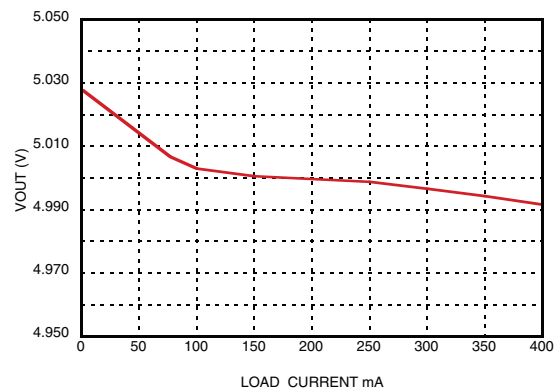
**Figure 10. Supply Turn-Off Transient [2]**



**Figure 11. HMC976LP3E Output Noise Spectral Density vs. Commercial PSU [1]**



**Figure 12. Vout vs. Load current [1]**



[1] VDD=5.5V, 400mA Load [“HMC976LP3E 5V User Application Schematic”](#).

[2] VDD=5.0V, 400mA Load [“HMC976LP3E 3.3V User Application Schematic”](#)

## 400mA LOW NOISE, HIGH PSRR LINEAR VOLTAGE REGULATOR



**Table 2. Absolute Maximum Ratings**

|  |                |
|--|----------------|
| Vdd to GND Voltage                                   | +5.8V / -0.3V  |
| EN to GND Voltage                                    | +5.8V / -0.3V  |
| RDx / HVx to GND Voltage                             | +5.8V / -0.3V  |
| Maximum Dissipation                                  | 780mW          |
| Thermal Resistance (Junction to Ambient)             | 51.5 °C/W [3]  |
| Thermal Resistance (Junction to Case, Ground Paddle) | 18 °C/W        |
| Maximum Junction Temperature                         | +150 °C        |
| Max Output Current                                   | 420 mA         |
| Storage Temperature                                  | -65 to +150 °C |
| ESD Sensitivity (HBM)                                | Class 1C       |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The absolute maximum ratings apply individually only, not in combination.

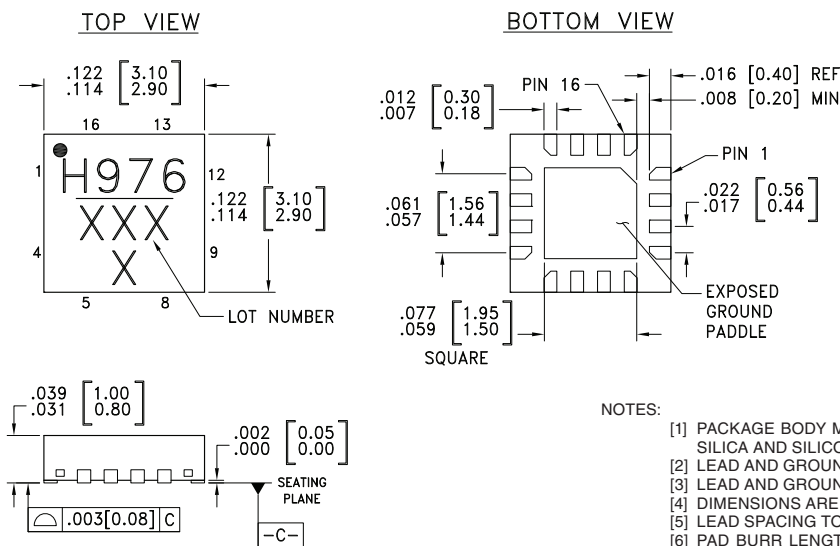


**ELECTROSTATIC SENSITIVE DEVICE  
OBSERVE HANDLING PRECAUTIONS**

**Table 3. Recommended Operating Condition**

| Parameter            | Condition | Min. | Typ. | Max. | Units |
|----------------------|-----------|------|------|------|-------|
| Junction Temperature |           |      |      | 115  | °C    |
| Ambient Temperature  |           | -40  |      | 85   | °C    |

### Outline Drawing



**NOTES:**

- PACKAGE BODY MATERIAL: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
- LEAD AND GROUND PADDLE MATERIAL: COPPER ALLOY.
- LEAD AND GROUND PADDLE PLATING: 100% MATTE TIN.
- DIMENSIONS ARE IN INCHES [MILLIMETERS].
- LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
- PAD BURR LENGTH SHALL BE 0.15mm MAX. PAD BURR HEIGHT SHALL BE 0.25m MAX.
- PACKAGE WARP SHALL NOT EXCEED 0.05mm
- ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB GROUND.
- REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

**Table 4. Package Information**

| Part Number | Package Body Material                              | Lead Finish   | MSL Rating          | Package Marking <sup>[1]</sup> |
|-------------|--|---------------|---------------------|--------------------------------|
| HMC976LP3E  | RoHS-compliant Low Stress Injection Molded Plastic | 100% matte Sn | MSL1 <sup>[2]</sup> | 976<br>XXX<br>X                |

[1] 4-Digit lot number XXXX

[2] Max peak reflow temperature of 260 °C

[3] For standard HMC976LP3E evaluation board, no heat sink (HS) and no air flow, see figures 14, 15, and 16

## 400mA LOW NOISE, HIGH PSRR LINEAR VOLTAGE REGULATOR



**Table 5. Pin Descriptions**

| Pin Number         | Function | Description   | Interface Schematic |
|--------------------|----------|---|---------------------|
| 1                  | EN       | Enable Input, TTL Logic Level. The VR and VRX outputs are floating (high impedance) when EN = Low.  |                     |
| 2                  | RD       | Resistive feedback for VR, see "Output Voltage Adjust" section.                                     |                     |
| 3                  | REF      | Reference voltage (bandgap) output. Cannot be used to source/sink current to/from external circuits |                     |
| 4                  | VRX      | For Decoupling Capacitor<br>Cannot be used to source current to external circuits                   |                     |
| 11                 | VR       | Regulator Output VR 400mA   |                     |
| 5                  | HV       | Sets VR to 5V output when grounded  |                     |
| 6 - 10, 12 - 14,16 | N/C      | These pins can be left unconnected or connected to GND with no change in performance                |                     |
| 15                 | VDD      | Unregulated power supply input 5.5V max   |                     |
| Package Base       | GND      | Must contact PCB ground   |                     |

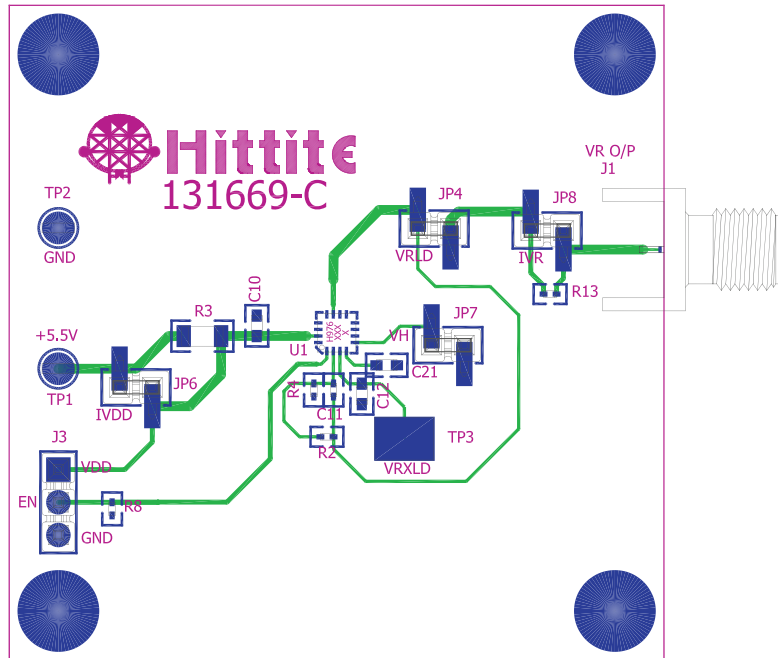
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LINEAR VOLTAGE REGULATOR**



**Evaluation PCB**



**Table 6. Ordering Information**

| Item           | Contents                  | Part Number       |
|----------------|---------------------------|-------------------|
| Evaluation PCB | HMC976LP3E Evaluation PCB | 131671-HMC976LP3E |

**Table 7. List of Materials for Evaluation PCB 131671**

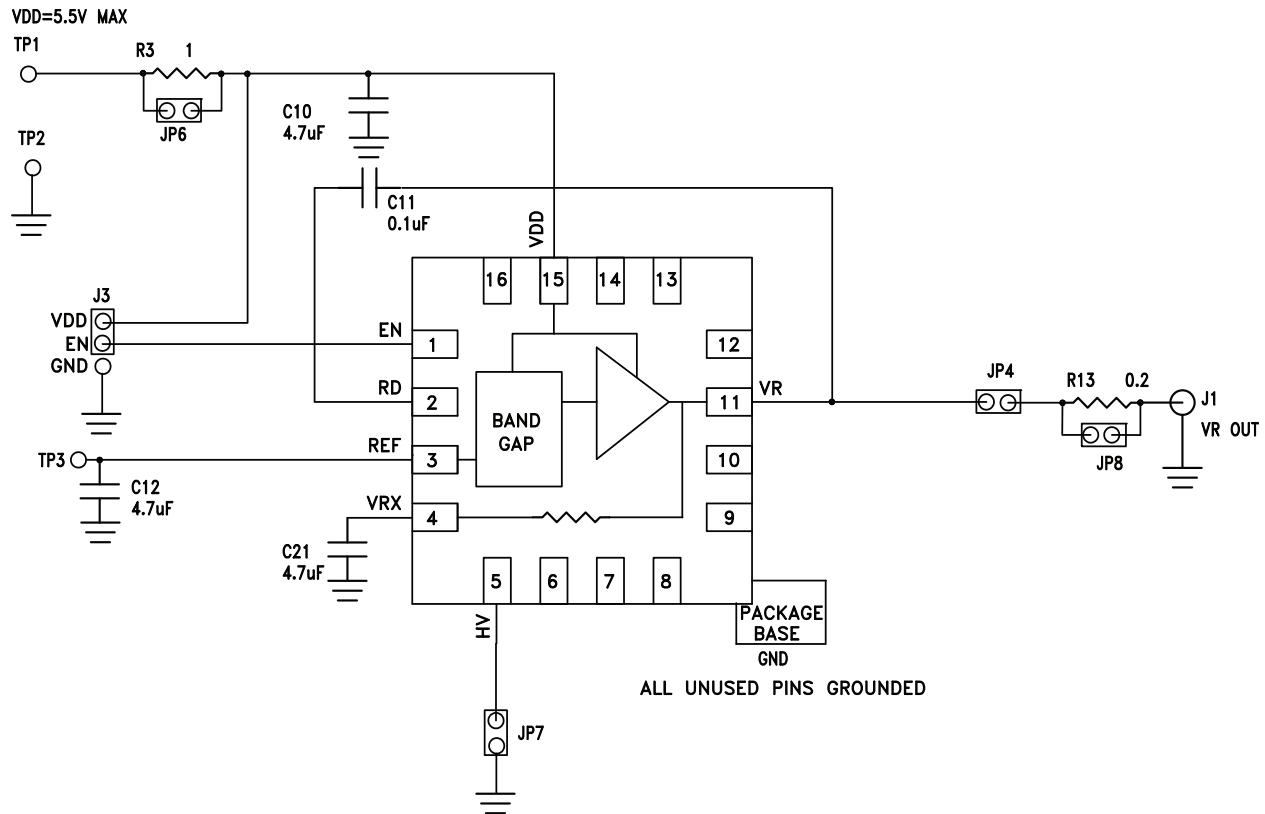
| Item                | Contents   |
|---------------------|--|
| J1                  | PCB Mount SMA connector  |
| J3                  | 3 Pin Header   |
| JP4, JP6, JP7, JP8, | 2 Pin Header and Jumper  |
| C10, C12, C21       | 4.7µF Capacitor 0603 Pkg.                                      |
| C11                 | 0.1µF Capacitor 0402 Pkg.                                      |
| R13                 | 0.2 Ohm Resistor 0402 Pkg.                                     |
| R3                  | 1 Ohm Resistor 0402 Pkg.                                       |
| R8                  | 100 kOhm Resistor 0402 Pkg.                                    |
| TP1, TP3            | Test Point PC Compact Red                                      |
| TP2                 | Test Point PC Compact Black                                    |
| U1                  | HMC976LP3E 400mA Low Noise, High PSRR Linear Voltage Regulator |
| PCB                 | 131669 Eval Board  |

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**Figure 13. Evaluation PCB Schematic**



### Operational Features

The recommended configuration is [“HMC976LP3E 4.8V User Application Schematic”](#). This is for the default output voltage of 4.8V nominal. The values shown are those recommended for optimum Noise Spectral density. For users requiring extremely low noise in the 1 MHz to 10 MHz range the largest output capacitor should be used: a 68uF takes the noise between 100 kHz and 1 MHz to below 2.5nV/√Hz.

### Load Capacitor Characteristics

The HMC976LP3E was designed to work with a low ESR ceramic load capacitor on the VRX pin (C21 in the schematic above). Low ESR ceramic capacitors are very small and best for eliminating high frequency noise. Ceramic capacitors can vary as much as 50% versus temperature and 60% versus voltage, dependant on the ceramic type e.g. Z5U, Y5V, X7R or X5R. There are no restrictions on ceramic type or minimum ESR, only that the user must guarantee that the minimum output capacitance over operating conditions is 4.7µF, smaller values can result in noise peaking or lower stability.



## 400mA LOW NOISE, HIGH PSRR LINEAR VOLTAGE REGULATOR



### Output Voltage Adjustment

The default output voltage is 4.8V this configuration "[HMC976LP3E 4.8V User Application Schematic](#)".

The output voltage can be set to 5V by a ground on HV pin 5 "[HMC976LP3E 5V User Application Schematic](#)".

The output voltage can be set from 1.8V to <4.8V by a resistor from pin 2 to the output pin 11 shown in "[HMC976LP3E 3.3V User Application Schematic](#)". The value of the resistor is given by the equation below.

$$R1 = \frac{\left( \left( \frac{V_{out}}{1.17} \right) - 1 \right) * 18.9}{1 - 0.32 * \left( \left( \frac{V_{out}}{1.17} \right) - 1 \right)} \quad (\text{Kohms})$$

If the temperature stability performance similar to that shown in the plot "[Vout=5V and Vref vs. Temperature](#)" is required, then any external resistor temperature coefficient is a critical parameter and should be better than 50ppm and 1% tolerance. Please note that the temperature coefficient of the internal resistor feedback divider is 270ppm/°C.

### Layout of PCB

The layout of the PCB should follow these guide lines, the PADDLE should be connected to ground with at least 5 vias directly under the paddle to the bottom side ground plane. To ensure the noise and PSRR specifications are met, the capacitors connecting to Pins 15, 11, 3 (see user application schematics), should be placed as close as possible to the relevant pin and the ground connection should be as short as possible. Trace widths and via sizes should be scaled to match the current drawn. The use of a large ground plane is recommended with a large number of ground vias near the device to carry the ground.

### Thermal Protection

The HMC976LP3E includes an integrated thermal protection circuit. If the junction temperature of the HMC976LP3E reaches the maximum operating junction temperature (115°C max, 130°C typical) then the thermal protection circuit temporarily disables the HMC976LP3E outputs (with ~500uA output current) until the junction temperature cools down by approximately 10°C.

A typical reason for the increase of the junction temperature is an unexpected increase in current draw. By disabling the outputs, the HMC976LP3E is in this case protecting the other devices on the PCB that it is supplying with current. The thermal protection circuitry will also indirectly protect against a short circuit at the output. After the overload or the fault condition is removed or changed, the regulator output returns to the nominal operation

For reliable long term operation the "[Recommended Operating Condition](#)" must be followed and the maximum junction temperature must not be exceeded. The junction temperature for a given dissipation can be calculated from the equation below:

$$T_j = T_a + \left( P_d \times \theta_{ja} \right)$$

Where T<sub>j</sub>=Junction Temperature (°C), T<sub>a</sub>=Ambient Temperature (°C), P<sub>d</sub>=Dissipated Power (W) θ<sub>ja</sub>=Thermal Resistivity Junction to Ambient (°C/W). Please refer to Table 2 for thermal resistance values.

## 400mA LOW NOISE, HIGH PSRR LINEAR VOLTAGE REGULATOR



Thermal dissipation should be taken into account at all times especially with large dropout voltages VDD-VR, i.e. if 1.8V output is required from 5.5V input voltage, then the output current must be restricted to <210mA, or VDD restricted to <3.75V for a 400mA load.

The exact maximum operating temperature before the thermal protection circuit activates is largely dependent on the customer PCB design. Below is an example for maximum ambient temperature calculation for the standard HMC976LP3E evaluation PCB with no heat sink and no air flow (fans). Customers should perform this calculation for their PCB layout and operating conditions.

$$V_{IN}=5.5V, V_{out}=5.0V, I_{out}=400mA$$

$$V_{dropout}=V_{IN}-V_{OUT}=0.5V$$

$$\text{Dissipated power on regulator } P_d=0.5V \times 0.4A=0.2W$$

$$\theta_{ja}=51.5^{\circ}C/W$$

Junction temperature increase using standard HMC976 board:  $DT_j=P_d \times \theta_{ja}=10.3^{\circ}C$ . Thermal shutdown junction temperature of regulator (absolute min)  $T_{sdwn}=+115^{\circ}C$ . Maximum corresponding ambient temperature  $T_{a\_max} = T_{sdwn} - DT_j = +104.7^{\circ}C$

The plots below show how the PCB ground copper area affects the HMC976LP3E junction temperature for different HMC976LP3E power dissipation conditions. The following cases are included in the plots:

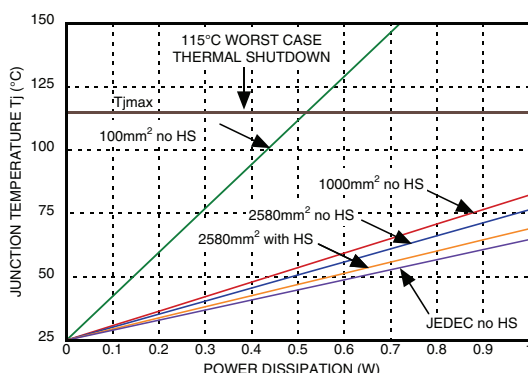
1. 100 mm<sup>2</sup> Copper Area
2. 1000 mm<sup>2</sup> Copper Area
3. 2580 mm<sup>2</sup> Copper Area HMC976LP3E Evaluation PCB No Heat Sink (HS)
4. 2580 mm<sup>2</sup> Copper Area HMC976LP3E Evaluation PCB with Heat Sink (HS)
5. JEDEC Board as per JESD51-3

The typical corresponding  $\theta_{ja}$  is shown in Table 8:

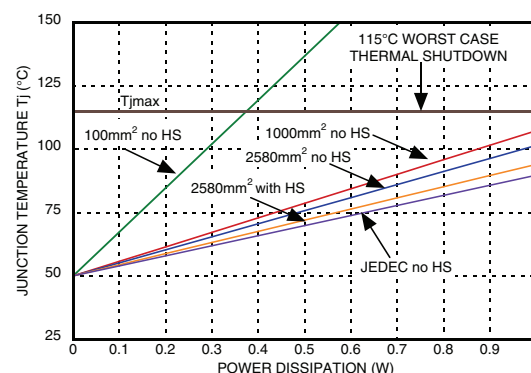
**Table 8. Typical  $\theta_{ja}$  for specified PCB Copper Sizes**

| Copper size (mm <sup>2</sup> ) | $\theta_{ja}$ (°C/W) |
|--------------------------------|----------------------|
| 100                            | 173.5                |
| 1000                           | 57.3                 |
| 2580 no HS                     | 51.5                 |
| 2580 with HS                   | 44                   |

**Figure 14. HMC976LP3E JUNCTION TEMPERATURE °C vs. TOTAL POWER DISSIPATION 25°C AMBIENT**



**Figure 15. HMC976LP3E JUNCTION TEMPERATURE °C vs. TOTAL POWER DISSIPATION 50°C AMBIENT**



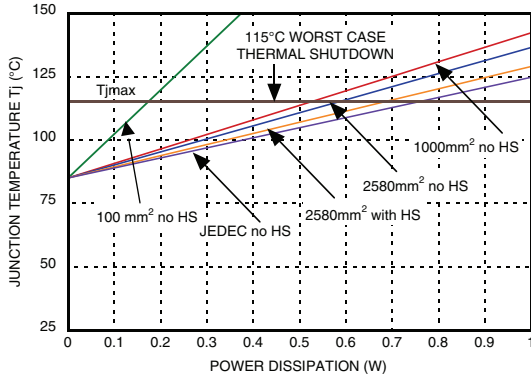
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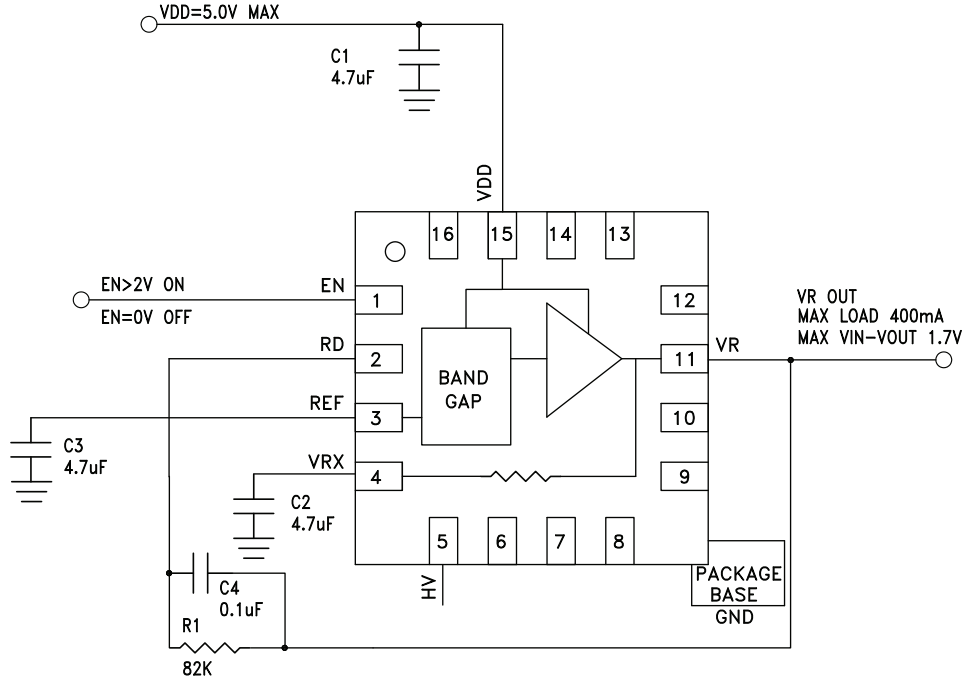
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**Figure 16. HMC976LP3E JUNCTION TEMPERATURE °C vs. TOTAL POWER DISSIPATION 85°C AMBIENT**

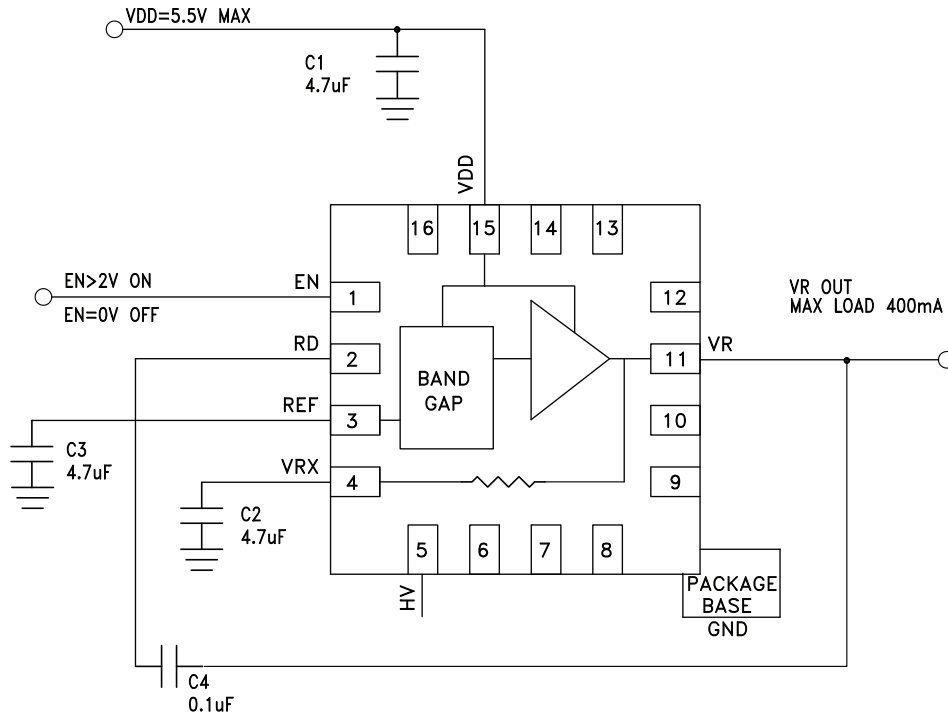


**Figure 17. HMC976LP3E 3.3V User Application Schematic**

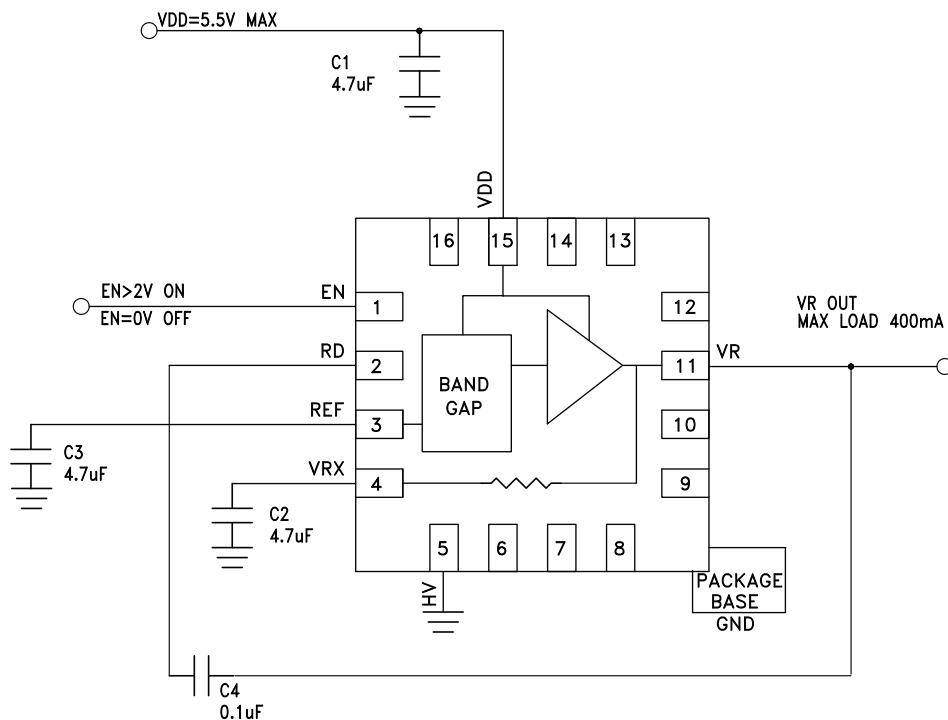




**Figure 18. HMC976LP3E 4.8V User Application Schematic**



**Figure 19. HMC976LP3E 5V User Application Schematic**



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