

# MOSFET

## 800V CoolMOS™ P7 Power Device

The latest 800V CoolMOS™ P7 series sets a new benchmark in 800V super junction technologies and combines best-in-class performance with state of the art ease-of-use, resulting from Infineon's over 18 years pioneering super junction technology innovation.

### Features

- Best-in-class FOM  $R_{DS(on)} * E_{oss}$ ; reduced  $Q_g$ ,  $C_{iss}$ , and  $C_{oss}$
- Best-in-class DPAK  $R_{DS(on)}$
- Best-in-class  $V_{(GS)th}$  of 3V and smallest  $V_{(GS)th}$  variation of  $\pm 0.5V$
- Integrated Zener Diode ESD protection
- Fully optimized portfolio

### Benefits

- Best-in-class performance
- Enabling higher power density designs, BOM savings and lower assembly costs
- Easy to drive and to parallel
- Better production yield by reducing ESD related failures
- Less production issues and reduced field returns
- Easy to select right parts for fine tuning of designs

### Potential applications

Recommended for hard and soft switching flyback topologies for LED Lighting, low power Chargers and Adapters, Audio, AUX power and Industrial power. Also suitable for PFC stage in Consumer applications and Solar.

### Product validation

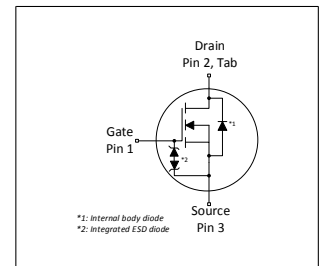
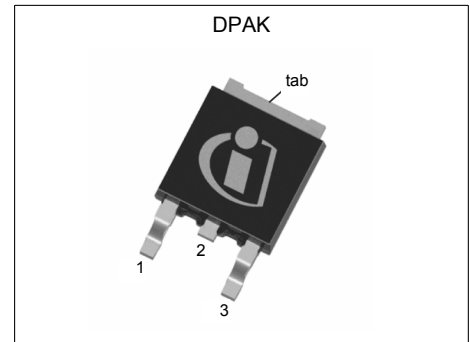
Fully qualified according to JEDEC for Industrial Applications

*Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.*

**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS} @ T_J=25^\circ C$	800	V
$R_{DS(on),max}$	0.90	$\Omega$
$Q_{g,typ}$	15	nC
$I_D$	6	A
$E_{oss} @ 500V$	1.4	$\mu J$
$V_{GS(th),typ}$	3	V
ESD class (HBM)	2	-

Type / Ordering Code	Package	Marking	Related Links
IPD80R900P7	PG-TO252-3	80R900P7	see Appendix A



RoHS

## Table of Contents

Description .....	1
Maximum ratings .....	3
Thermal characteristics .....	3
Electrical characteristics .....	4
Electrical characteristics diagrams .....	6
Test Circuits .....	10
Package Outlines .....	11
Appendix A .....	12
Revision History .....	13
Trademarks .....	13
Disclaimer .....	13

## 1 Maximum ratings

at  $T_j = 25^\circ\text{C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current <sup>1)</sup>	$I_D$	-	-	6 3.9	A	$T_C=25^\circ\text{C}$ $T_C=100^\circ\text{C}$
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$	-	-	14	A	$T_C=25^\circ\text{C}$
Avalanche energy, single pulse	$E_{AS}$	-	-	13	mJ	$I_D=0.9\text{A}$ ; $V_{DD}=50\text{V}$
Avalanche energy, repetitive	$E_{AR}$	-	-	0.11	mJ	$I_D=0.9\text{A}$ ; $V_{DD}=50\text{V}$
Avalanche current, repetitive	$I_{AR}$	-	-	0.9	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	100	V/ns	$V_{DS}=0$ to 400V
Gate source voltage	$V_{GS}$	-20 -30	-	20 30	V	static; AC ( $f>1$ Hz)
Power dissipation	$P_{tot}$	-	-	45	W	$T_C=25^\circ\text{C}$
Operating and storage temperature	$T_j, T_{stg}$	-55	-	150	$^\circ\text{C}$	-
Continuous diode forward current	$I_S$	-	-	4.4	A	$T_C=25^\circ\text{C}$
Diode pulse current <sup>2)</sup>	$I_{S,pulse}$	-	-	14	A	$T_C=25^\circ\text{C}$
Reverse diode dv/dt <sup>3)</sup>	dv/dt	-	-	1	V/ns	$V_{DS}=0$ to 400V, $I_{SD}<=1.1\text{A}$ , $T_j=25^\circ\text{C}$
Maximum diode commutation speed <sup>3)</sup>	di/dt	-	-	50	A/ $\mu\text{s}$	$V_{DS}=0$ to 400V, $I_{SD}<=1.1\text{A}$ , $T_j=25^\circ\text{C}$

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{thJC}$	-	-	2.8	$^\circ\text{C/W}$	-
Thermal resistance, junction - ambient	$R_{thJA}$	-	-	62	$^\circ\text{C/W}$	Device on PCB, minimal footprint
Thermal resistance, junction - ambient for SMD version	$R_{thJA}$	-	35	45	$^\circ\text{C/W}$	Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm <sup>2</sup> (one layer 70 $\mu\text{m}$ thickness) copper area for drain connection and cooling. PCB is vertical without air stream cooling.
Soldering temperature, wave- & reflow soldering allowed	$T_{sold}$	-	-	260	$^\circ\text{C}$	reflow MSL1

<sup>1)</sup> Limited by  $T_{j,max}$ . Maximum duty cycle  $D=0.5$

<sup>2)</sup> Pulse width  $t_p$  limited by  $T_{j,max}$

<sup>3)</sup>  $V_{DClink}=400\text{V}$ ;  $V_{DS,peak}<V_{(BR)DSS}$ ; identical low side and high side switch with identical  $R_G$ ;  $t_{cond}<2\mu\text{s}$

### 3 Electrical characteristics

at  $T_j = 25^\circ\text{C}$ , unless otherwise specified

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	800	-	-	V	$V_{GS}=0V, I_D=1mA$
Gate threshold voltage	$V_{GS(th)}$	2.5	3	3.5	V	$V_{DS}=V_{GS}, I_D=0.11mA$
Zero gate voltage drain current	$I_{DSS}$	-	-	1	$\mu A$	$V_{DS}=800V, V_{GS}=0V, T_j=25^\circ C$ $V_{DS}=800V, V_{GS}=0V, T_j=150^\circ C$
Gate-source leakage current incl. zener diode	$I_{GSS}$	-	-	1	$\mu A$	$V_{GS}=20V, V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.77	0.90	$\Omega$	$V_{GS}=10V, I_D=2.2A, T_j=25^\circ C$ $V_{GS}=10V, I_D=2.2A, T_j=150^\circ C$
Gate resistance	$R_G$	-	1.4	-	$\Omega$	$f=250kHz, \text{open drain}$

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	-	350	-	pF	$V_{GS}=0V, V_{DS}=500V, f=250kHz$
Output capacitance	$C_{oss}$	-	6	-	pF	$V_{GS}=0V, V_{DS}=500V, f=250kHz$
Effective output capacitance, energy related <sup>1)</sup>	$C_{o(er)}$	-	11	-	pF	$V_{GS}=0V, V_{DS}=0 \text{ to } 500V$
Effective output capacitance, time related <sup>2)</sup>	$C_{o(tr)}$	-	135	-	pF	$I_D=\text{constant}, V_{GS}=0V, V_{DS}=0 \text{ to } 500V$
Turn-on delay time	$t_{d(on)}$	-	12	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=2.2A, R_G=15\Omega$
Rise time	$t_r$	-	8	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=2.2A, R_G=15\Omega$
Turn-off delay time	$t_{d(off)}$	-	40	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=2.2A, R_G=15\Omega$
Fall time	$t_f$	-	20	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=2.2A, R_G=15\Omega$

**Table 6 Gate charge characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	2	-	nC	$V_{DD}=640V, I_D=2.2A, V_{GS}=0 \text{ to } 10V$
Gate to drain charge	$Q_{gd}$	-	6	-	nC	$V_{DD}=640V, I_D=2.2A, V_{GS}=0 \text{ to } 10V$
Gate charge total	$Q_g$	-	15	-	nC	$V_{DD}=640V, I_D=2.2A, V_{GS}=0 \text{ to } 10V$
Gate plateau voltage	$V_{plateau}$	-	4.5	-	V	$V_{DD}=640V, I_D=2.2A, V_{GS}=0 \text{ to } 10V$

<sup>1)</sup>  $C_{o(er)}$  is a fixed capacitance that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 500V

<sup>2)</sup>  $C_{o(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 500V

**Table 7 Reverse diode characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	$V_{SD}$	-	0.9	-	V	$V_{GS}=0V, I_F=2.2A, T_i=25^\circ C$
Reverse recovery time	$t_{rr}$	-	610	-	ns	$V_R=400V, I_F=1.1A, di_F/dt=50A/\mu s$
Reverse recovery charge	$Q_{rr}$	-	5	-	$\mu C$	$V_R=400V, I_F=1.1A, di_F/dt=50A/\mu s$
Peak reverse recovery current	$I_{rrm}$	-	11	-	A	$V_R=400V, I_F=1.1A, di_F/dt=50A/\mu s$

### 4 Electrical characteristics diagrams

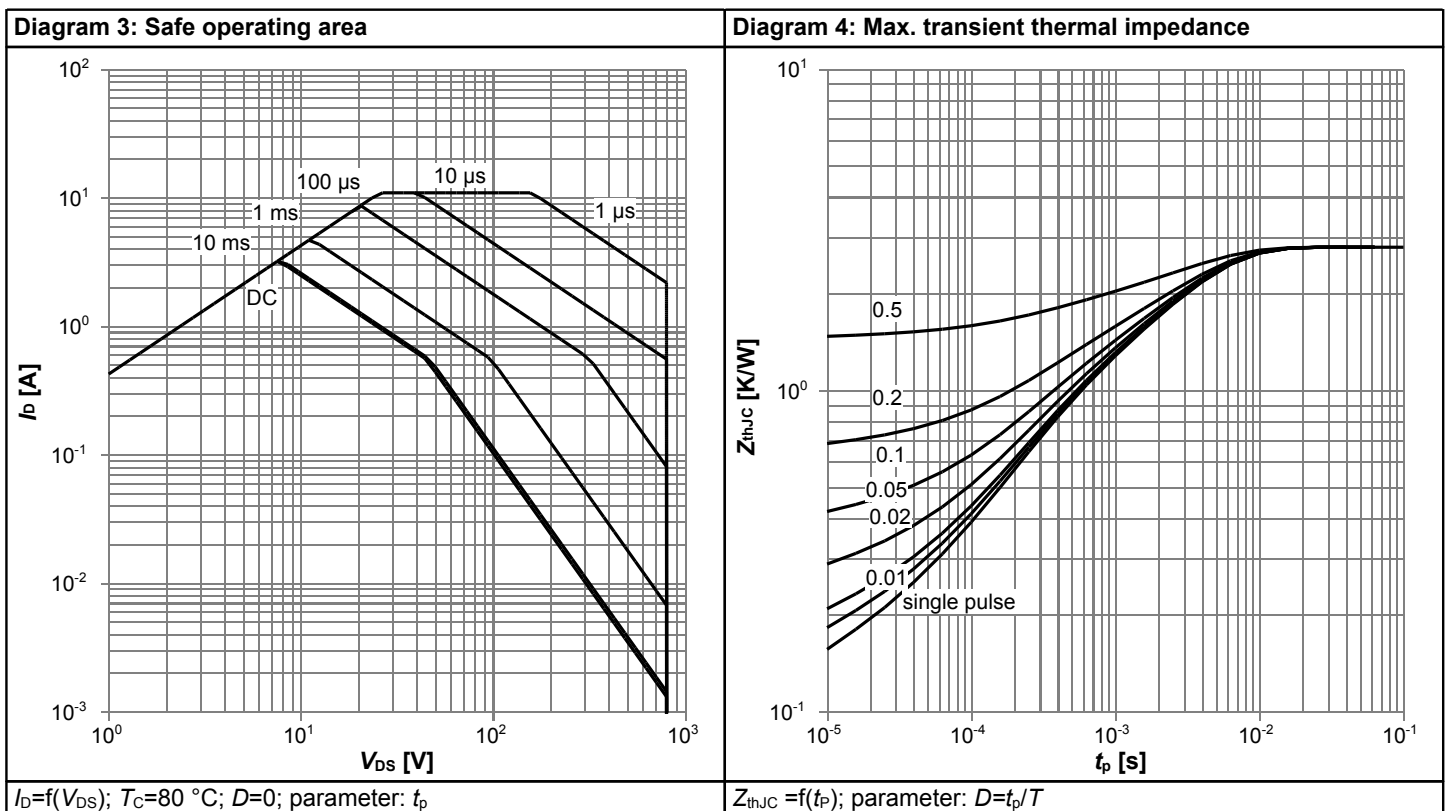
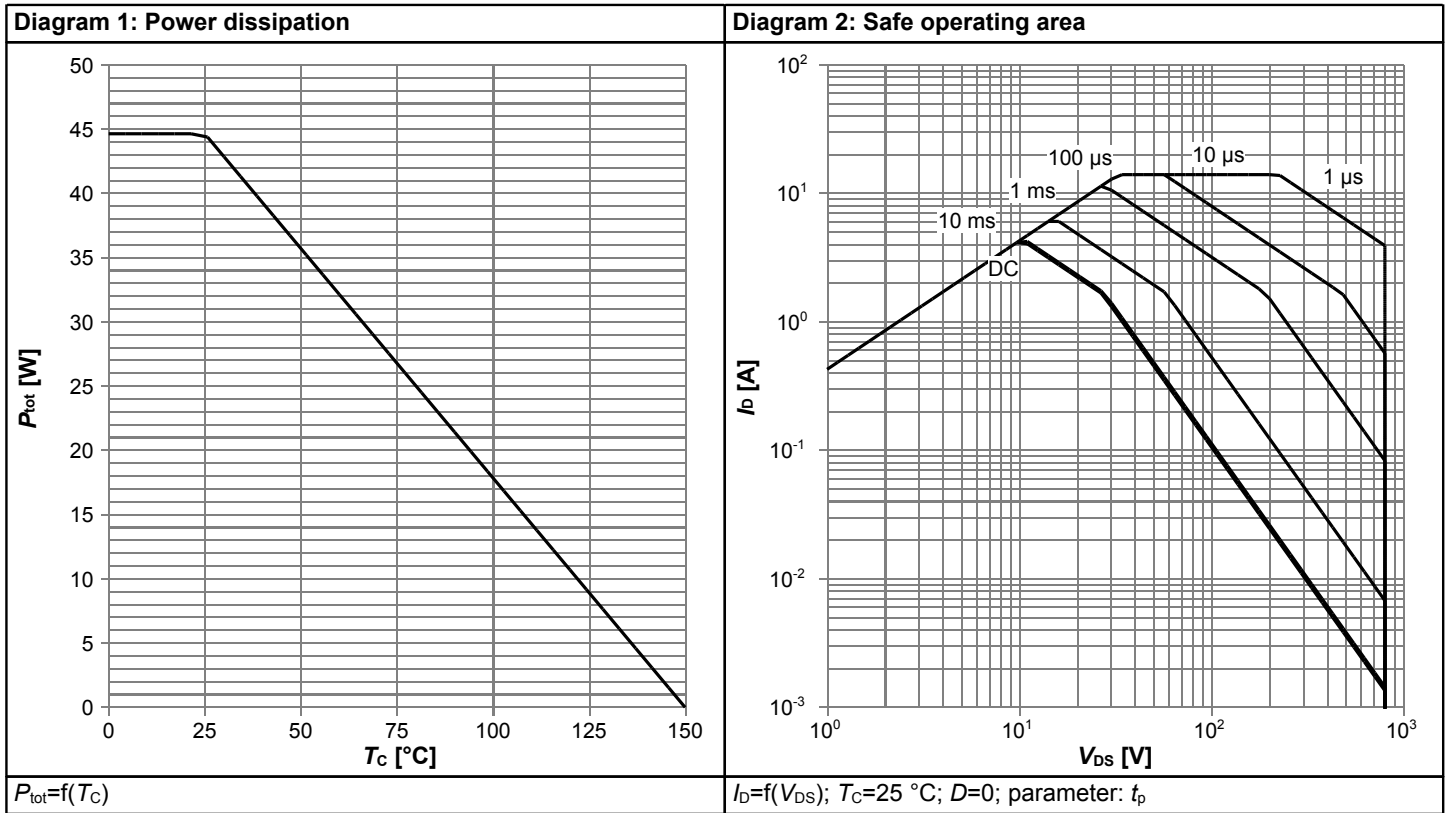
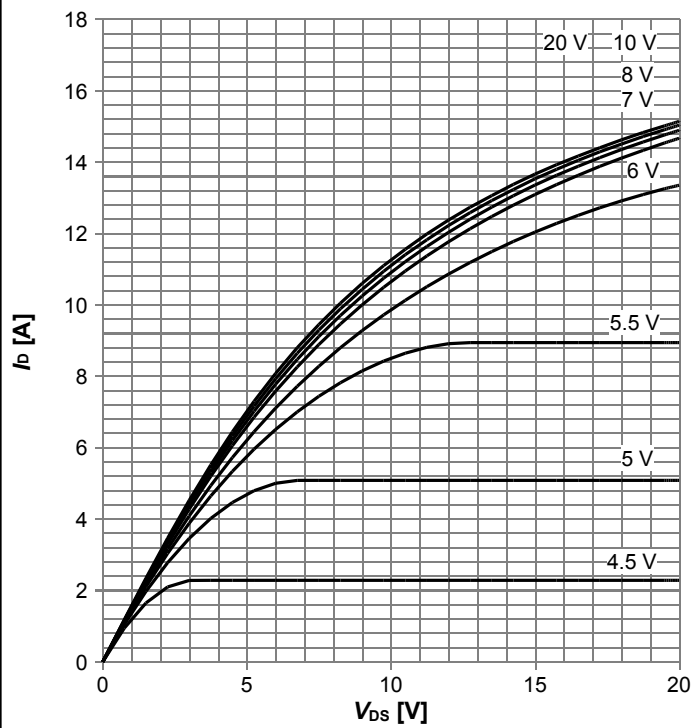
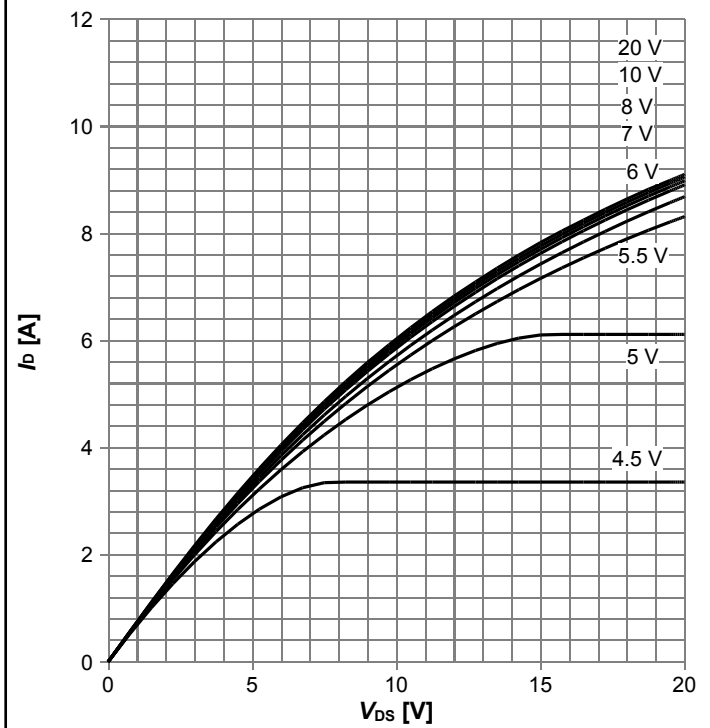


Diagram 5: Typ. output characteristics



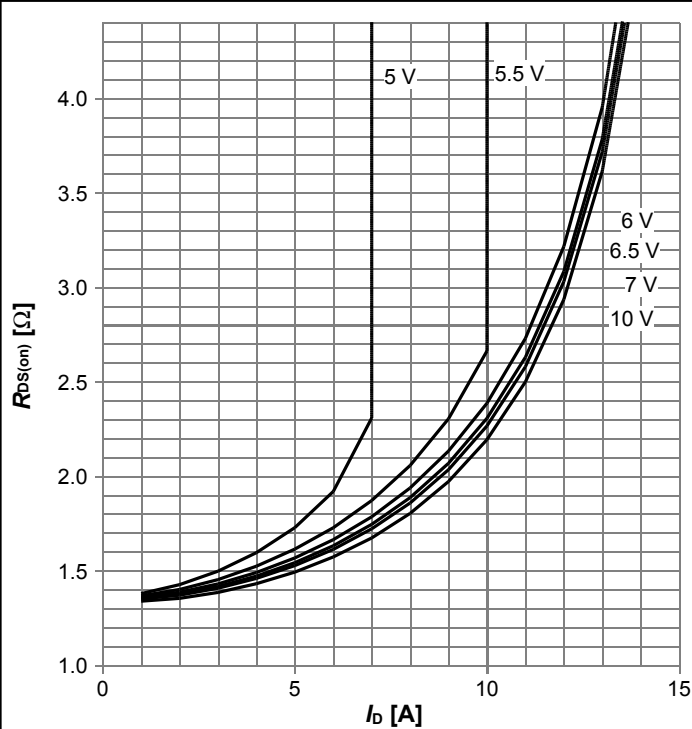
$I_D=f(V_{DS})$ ;  $T_j=25\text{ °C}$ ; parameter:  $V_{GS}$

Diagram 6: Typ. output characteristics



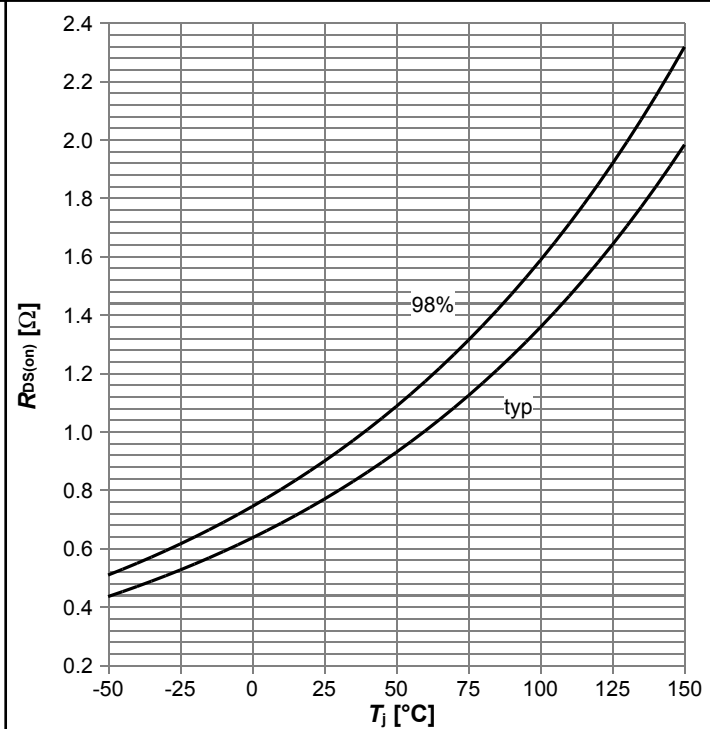
$I_D=f(V_{DS})$ ;  $T_j=125\text{ °C}$ ; parameter:  $V_{GS}$

Diagram 7: Typ. drain-source on-state resistance



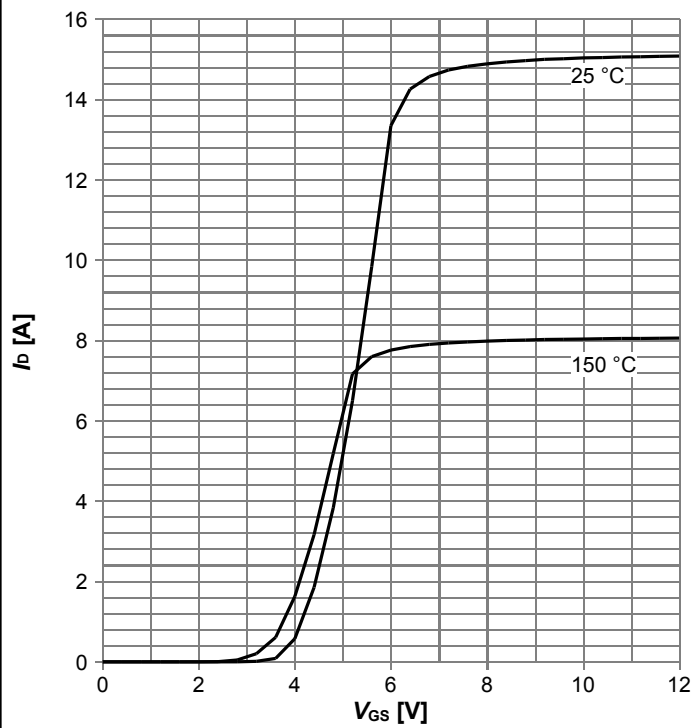
$R_{DS(on)}=f(I_D)$ ;  $T_j=125\text{ °C}$ ; parameter:  $V_{GS}$

Diagram 8: Drain-source on-state resistance



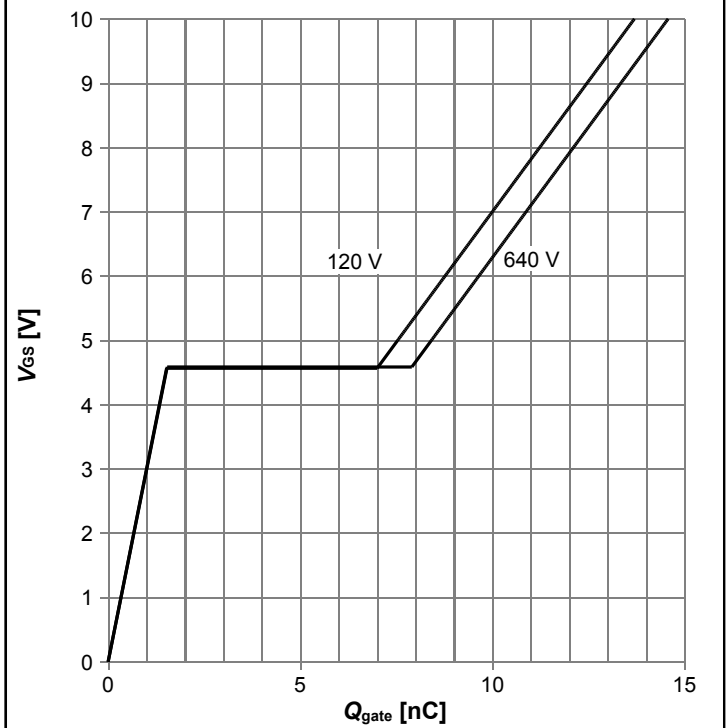
$R_{DS(on)}=f(T_j)$ ;  $I_D=2.2\text{ A}$ ;  $V_{GS}=10\text{ V}$

Diagram 9: Typ. transfer characteristics



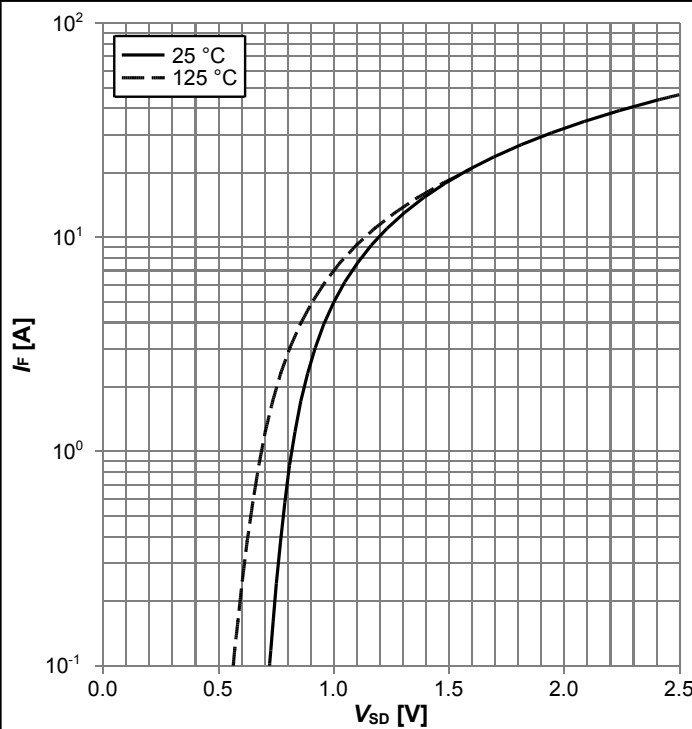
$I_D=f(V_{GS}); V_{DS}=20V$ ; parameter:  $T_j$

Diagram 10: Typ. gate charge



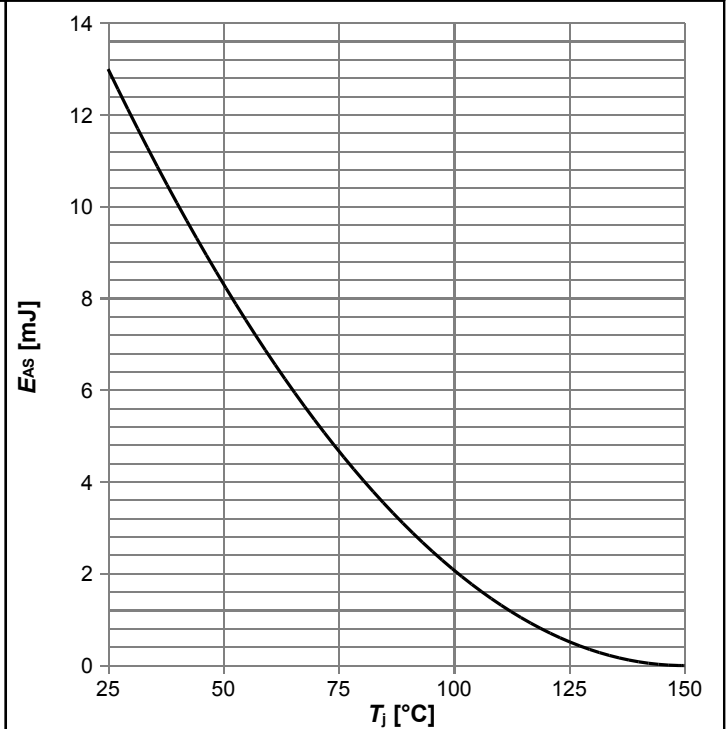
$V_{GS}=f(Q_{gate}); I_D=2.2 A$  pulsed; parameter:  $V_{DD}$

Diagram 11: Forward characteristics of reverse diode



$I_F=f(V_{SD})$ ; parameter:  $T_j$

Diagram 12: Avalanche energy



$E_{AS}=f(T_j); I_D=0.9 A; V_{DD}=50 V$

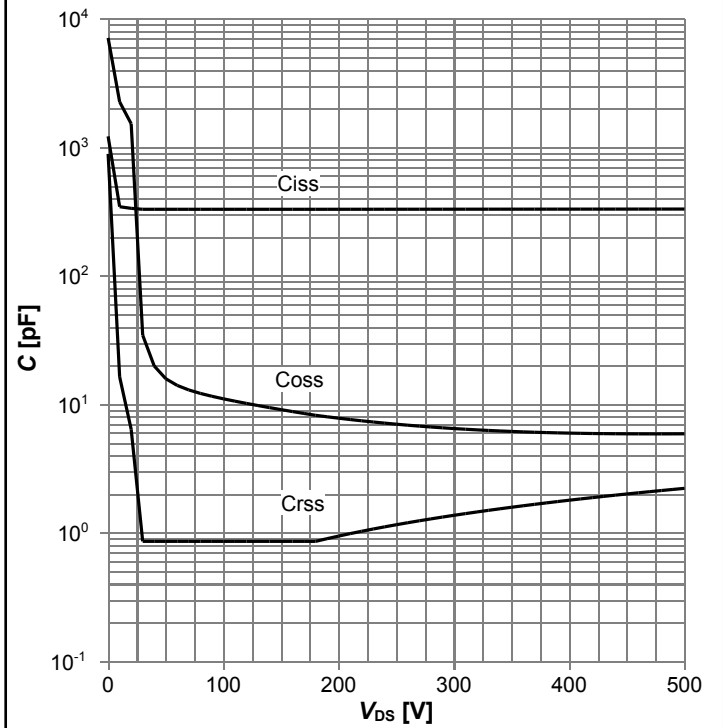


**Diagram 13: Drain-source breakdown voltage**



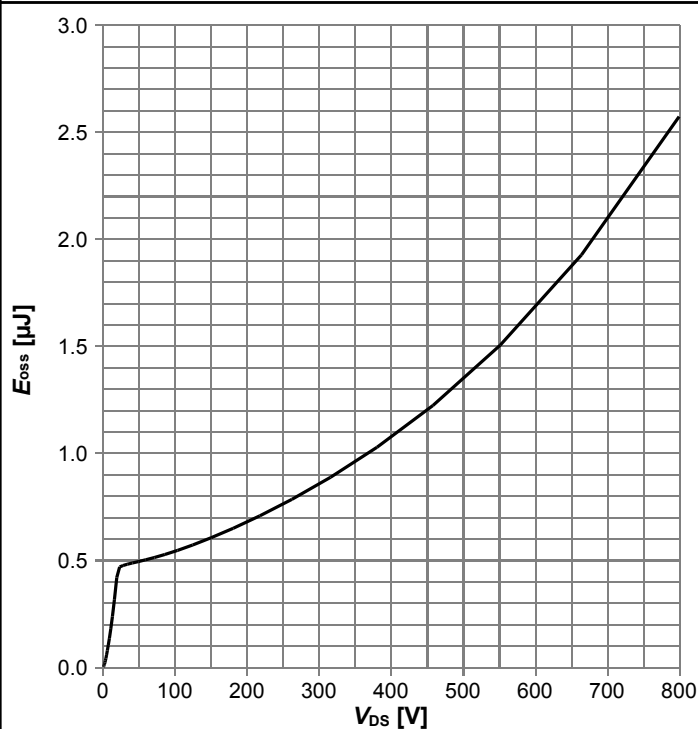
$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

**Diagram 14: Typ. capacitances**



$C=f(V_{DS}); V_{GS}=0 \text{ V}; f=250 \text{ kHz}$

**Diagram 15: Typ. Coss stored energy**



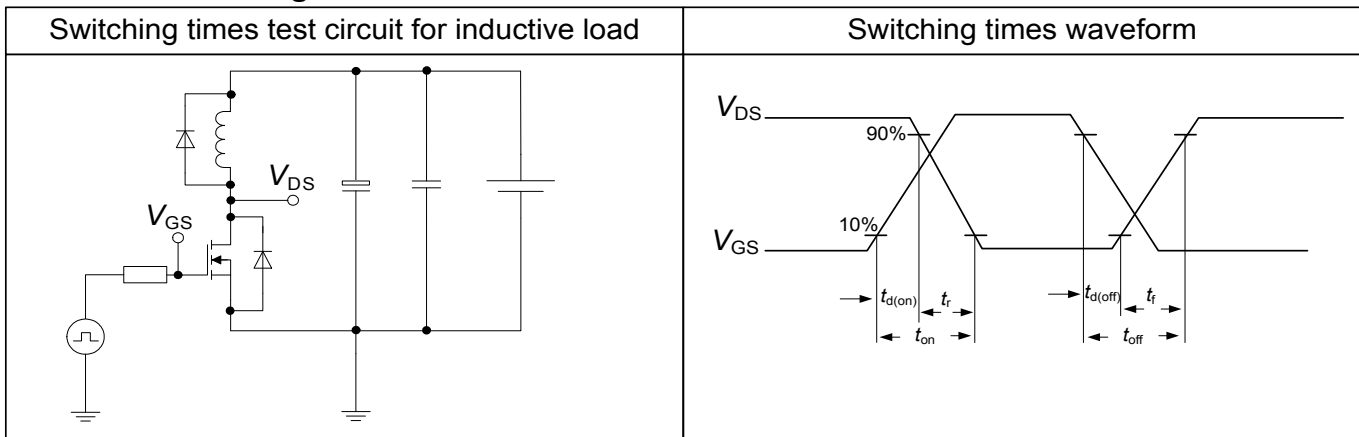
$E_{oss}=f(V_{DS})$

## 5 Test Circuits

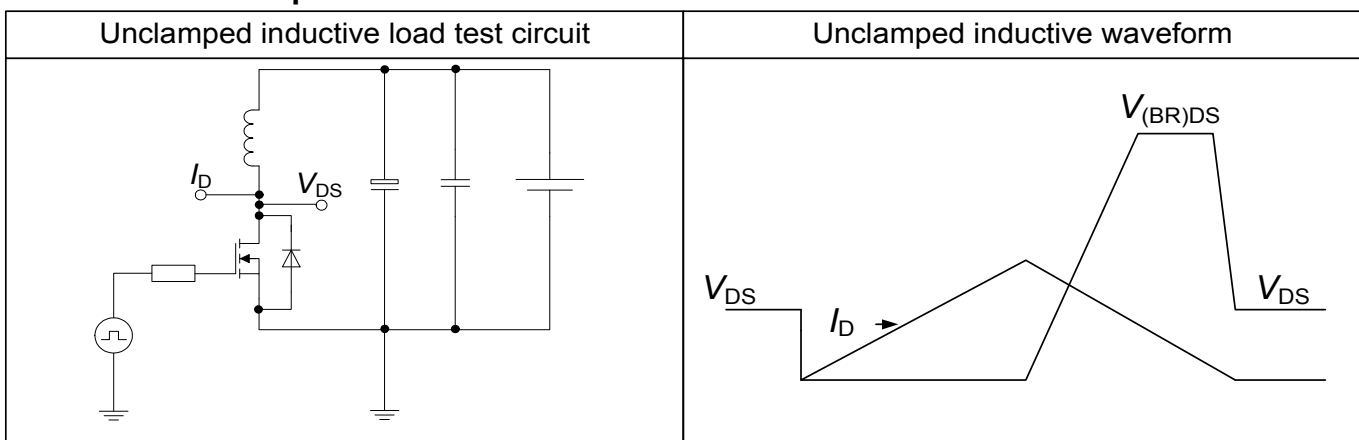
**Table 8 Diode characteristics**



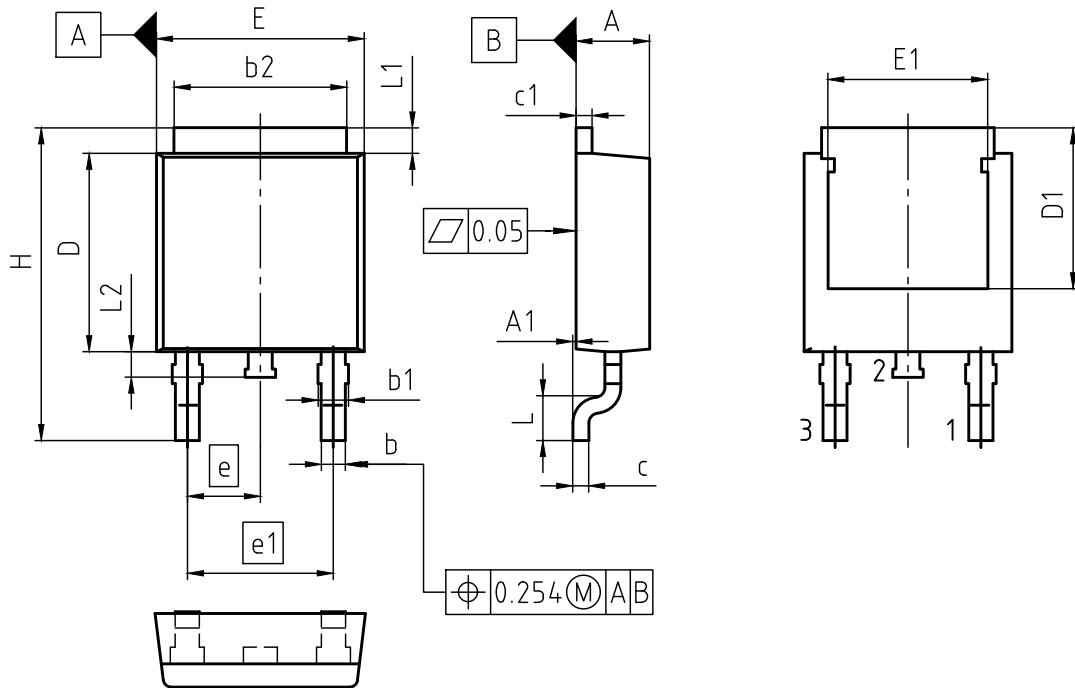
**Table 9 Switching times**



**Table 10 Unclamped inductive load**



## 6 Package Outlines



PACKAGE - GROUP NUMBER: <b>PG-TO252-3-U02</b>		
REVISION: 01		DATE: 23.11.2021
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	2.16	2.41
A1	0.00	0.15
b	0.64	0.89
b1	0.65	1.15
b2	4.95	5.50
c	0.46	0.61
c1	0.40	0.98
D	5.97	6.22
D1	5.02	5.84
E	6.35	6.73
E1	4.32	5.50
e	2.29	
e1	4.57	
N	3	
H	9.40	10.48
L	1.18	1.78
L1	0.89	1.27
L2	0.51	1.02

ALL DIMENSIONS REFER TO JEDEC STANDARD TO-252 AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

Figure 1 Outline PG-TO252-3, dimensions in mm

## **7 Appendix A**

### **Table 11 Related Links**

- **IFX CoolMOS Webpage:** [www.infineon.com](http://www.infineon.com)
- **IFX Design tools:** [www.infineon.com](http://www.infineon.com)

## Revision History

IPD80R900P7

**Revision: 2022-01-13, Rev. 2.3**

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2017-03-21	Release of final version
2.1	2018-02-09	Corrected front page text
2.2	2020-05-26	Updated package/symbol drawing, and product validation
2.3	2022-01-13	Updated Package Outlines

### Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

### We Listen to Your Comments

Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to:

[erratum@infineon.com](mailto:erratum@infineon.com)

### Published by

**Infineon Technologies AG**  
**81726 München, Germany**  
**© 2022 Infineon Technologies AG**  
**All Rights Reserved.**

### Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffungsgarantie").

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer's compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Infineon Technologies in customer's applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

### Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office ([www.infineon.com](http://www.infineon.com)).

### Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

The Infineon Technologies component described in this Data Sheet may be used in life-support devices or systems and/or automotive, aviation and aerospace applications or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support, automotive, aviation and aerospace device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.