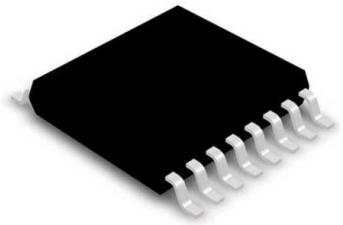
ADC120

Datasheet

8-channel, 50 ksps to 1 Msps, 12-bit A/D converter



TSSOP-16

Features

- 50 ksps to 1 Msps conversion rate
- 8-to-1-channel input MUX
- 3.3 V operating supply
- Pure CMOS
- Very low consumption
- SPI, serial digital output
- Power-down function

Applications

- Shunt resistor detector
- Analog multiplexing and conversion
- Telemetry

Description

The ADC120 is a low-power, eight-channel pure CMOS 12-bit analog-to-digital converter specified for conversion from 50 ksps to 1 Msps, tested at 1 Msps. The architecture is based on a successive-approximation register with an internal track-and-hold cell. The ADC120 features 8 single ended multiplexed inputs. The output serial data is straight binary and is SPI™ compatible.

The analog and digital power supplies operate from 2.7 V to 3.6 V. The power consumption at 3.3 V nominal supply is as low as 6.6 mW. The ADC120 comes plastic TSSOP-16, and can operates from -40 °C to +125 °C ambient temperature.

Maturity status link
ADC120

Device summary	
Order code	ADC120IPT
Temperature range	-40 °C to +125 °C
Package	TSSOP-16
Marking	ADC120I

1 Functional description

Figure 1. **Pin description (top view)**

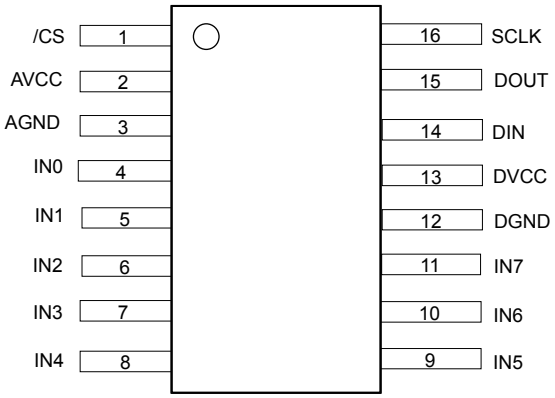


Figure 2. **Block diagram**

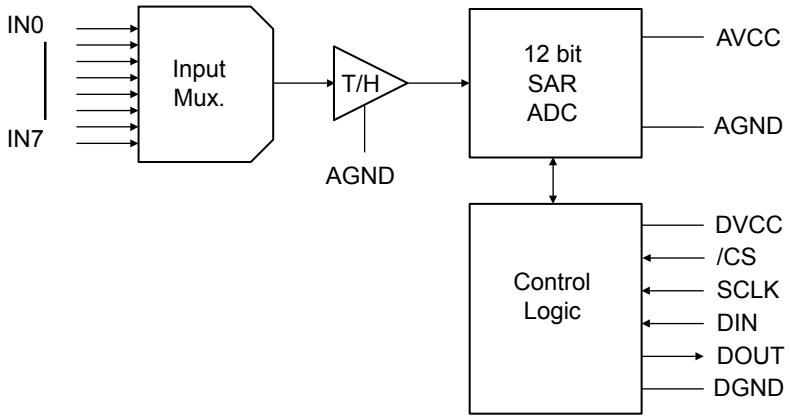


Table 1. **Control register bits**

Bit#	7 (MSB)	6	5	4	3	2	1	0
Symbol	Any code except 11		ADD2	ADD1	ADD0	Any code except 001		

Table 2. **Control register bit description**

Bit#	Symbol	Description
7, 6, 2, 1, 0	DONTC	Don't care (forbidden codes provided in Table 1. Control register bits)
5	ADD2	They determine which input channel converted, as per Table 3. Input channel description.
4	ADD1	
3	ADD0	

Table 3. **Input channel description**

ADD2	ADD1	ADD0	Input channel
0	0	0	IN0
0	0	1	IN1
0	1	0	IN2
0	1	1	IN3
1	0	0	IN4
1	0	1	IN5
1	1	0	IN6
1	1	1	IN7

2 Maximum ratings and operating conditions

Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 4. Absolute maximum ratings

Symbol	Parameters	Value	Units
AVCC (1)	Maximum analog power supply between AVCC and AGND	-0.3 V to 4.8 V	V
DVCC (1)	Maximum digital power supply between DVCC and DGND	-0.3 V to AVCC +0.3 V (max 4.8 V)	V
T_{stg}	Maximum temperature storage	-65 to +150	°C
T_j	Maximum junction temperature	+150	°C
R_{thja} (2)	Junction to ambient thermal resistance (TSSOP16 package)	95	°C/W
R_{thjc} (2)	Junction to case thermal resistance (TSSOP16 package)	35	°C/W
V_i (3)	Max voltage on any pin vs. GND	-0.3 V to AVCC +0.3 V	V
I_i	Max input current at any pin	± 10	mA
ESD	HBM on all pins (human body model)	± 4 k	V
	CDM on all pins (charged device model)	± 1 k	V

1. *All voltages, except differential I/O bus voltage, are with respect to the network ground terminal.*
2. *Short-circuits can cause excessive heating. Destructive dissipation can result from short-circuits on the amplifiers.*
3. *When the input voltage at any pin exceeds the power supplies (that is VIN < AGND or VIN > AVCC or DVCC), the current at that pin should be limited to 10 mA. The 20 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 10 mA to two.*

Table 5. Operating conditions

Symbol	Parameters	Min.	Max.	Units
AVCC	Analog supply voltage	2.7	3.6	V
DVCC	Digital supply voltage	AVCC - 0.15 V	AVCC + 0.15 V	V
VINA	Analog input voltage	0	AVCC	V
VIND	Digital input voltage	0	AVCC	V
SCLK	Clock frequency	0.8	16	MHz
Ta	Ambient temperature range	-40	+125	°C

3 Electrical characteristics

AVCC = DVCC = + 3.3 V, Single-ended input, AGND = DGND = 0 V, f_{SCLK} = 16 MHz, f_{SAMPLE} = 1 Msps, C_L = 25 pF, T_a = 25 °C, unless otherwise specified.

Table 6. Electrical characteristics

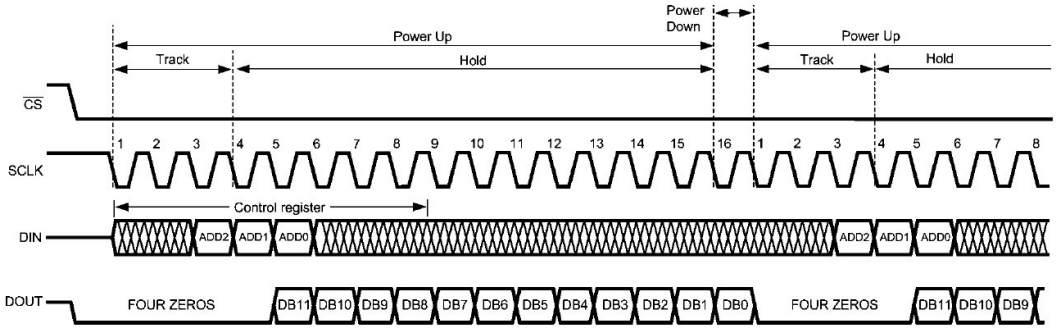
Symbol	Parameters	Test conditions	Min.	Typ.	Max	Unit
Static characteristics						
	Resolution with no missing codes				12	Bits
INL	Integral non-linearity (end point method)		-1.1	±0.4	1.1	LSB
DNL	Differential non-linearity		-0.8	±0.4	0.8	LSB
OE	Offset error		-2.3	0.8	2.3	LSB
OEM	Offset error match			0.8		
FSE	Full scale error		-2.3	0.8	2.3	LSB
FSEM	Full scale error match			0.8		LSB
Dynamic characteristics						
SINAD	Signal-to-noise plus distortion ratio (0 to Fs/2)	F_{IN} = 40.2 kHz, −0.02 dBFS	68.9	72		dB
SNR	Signal-to-noise ratio (0 to Fs/2)		71	73		dB
THD	Total harmonic distortion			−80	-73	dB
SFDR	Spurious-free dynamic range (0 to Fs/2)		74			dB
ENOB	Effective number of bits		11.1	11.7		Bits
ISO	Channel-to-channel isolation	F_{IN} = 20 kHz, −0.02 dBFS		84		dB
IM2	2nd order intermodulation	f_a = 19.5 kHz, f_b = 20.5 kHz VINA = VINB = -6.02 dBFS		−90		dB
IM3	3dr order intermodulation	f_a = 19.5 kHz, f_b = 20.5 kHz VINA = VINB = -6.02 dBFS		−90		dB
Analog input characteristics						
I_{DCL}	DC leakage current		-1		1	µA
C_{INA}	Input capacitance	Track mode		45		pF
		Hold mode		4.5		pF
Digital input characteristics						
V_{IH}	Input high voltage		2.1			V
V_{IL}	Input low voltage				0.8	V
I_{IN}	Digital input current	V_{IN} = 0 V or DVCC	-1		1	µA
C_{IND}	Digital input capacitance			4.5		pF
Digital output characteristics (output coding: straight (natural) binary)						
V_{OH} (1)	Output high voltage	I_{source} = 1 mA	2.8			V

Symbol	Parameters	Test conditions	Min.	Typ.	Max	Unit
V_{OL} (1)	Output low voltage	I_{sink} = 1 mA			0.4	V
I_{OZH}, I_{OZL}	Hi-impedance output leakage current		-1		1	µA
C_{OUT}	Hi-impedance output capacitance			4.5		pF
Power supply characteristic						
I_{AVCC} + I_{DVCC}	Total supply current, normal mode (CS low)	AVCC = DVCC = +2.7 V to +3.6 V, f_S = 1 MSPS, F_{IN} = 40 kHz			2	mA
	Total supply current, shutdown mode (CS high)	AVCC = DVCC = +2.7 V to +3.6 V, f_S = 0			5	µA
AC characteristics (AVCC = DVCC = +2.7 V to +3.6 V)						
$t_{CONVERT}$	Conversion (Hold) time				13	SCLK cycles
DC	SCLK duty cycle		40		60	%
t_{ACQ}	Acquisition (Track) Time cycles	See figure 3			3	SCLK cycles
	Throughput time Acquisition time + Conversion time				16	SCLK cycles
t_{AD}	Aperture delay			4		ns
Timing specifications (AVCC = DVCC = +2.7 V to +3.6 V) (2)						
t_{CSH}	CS/ hold time after SCLK rising edge	(3)	10	0		ns
t_{CSS}	CS/ setup time prior SCLK rising edge	(3)	10	4.5		ns
t_{EN}	CS/falling edge to DOUT enabled			5	30	ns
t_{DACC}	DOUT access time after SCLK falling edge	Load 25 pF		17	27	ns
t_{DHLD}	DOUT hold time after SCLK falling edge		7	4		ns
t_{DS}	DIN setup time prior to SCLK rising edge		10			ns
t_{DH}	DIN hold time after SCLK rising edge		10			ns
t_{DIS}	CS/ rising edge to DOUT high-impedance	DOUT falling		2.4	20	ns
		DOUT rising		0.9	20	
t_{CH}	Min. SCLK high time		0.4 x t_{SCLK}			ns
t_{CL}	Min. SCLK low time		0.4 x t_{SCLK}			ns

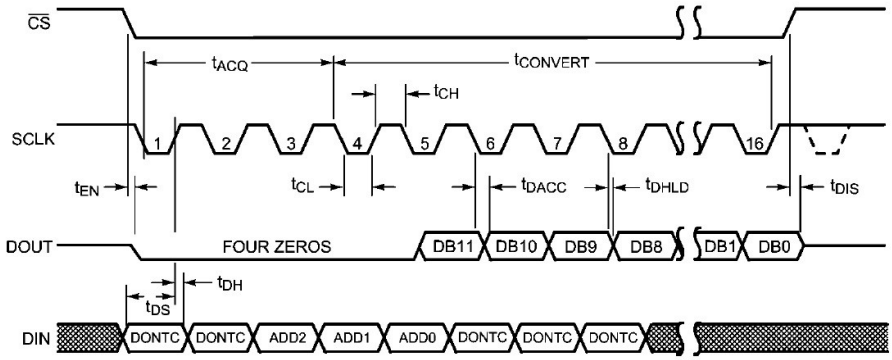
1. *Limits are guaranteed by functional test.*
2. *Limits are guaranteed by design or characterization.*
3. *Clock may be in any state (high or low) when CS/ goes high. Setup and hold time restrictions apply only to CS/ going low.*

4 Timing diagrams

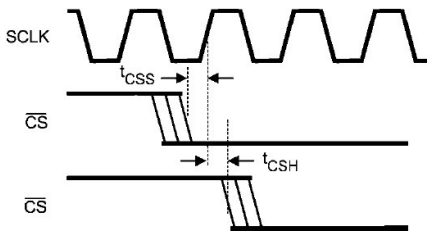
Figure 3. Timings



Operational Timing Diagram



Serial Timing Diagram



SCLK and $\overline{CS}$ Timing Parameters

5 Definitions

Acquisition Time is the time required to acquire the input voltage. During this time, the hold capacitor is charged by the input voltage.

Aperture Delay is the time between the fourth falling edge of SCLK and the time when the input signal is internally acquired or held for conversion.

Channel-to-channel isolation is the residual noise injected on the selected channel by other unselected channels.

Conversion Time is the time required, after the input voltage is acquired, to convert the input voltage to a digital word.

Differential Non-Linearity (DNL) is the maximum deviation from the ideal step size of 1 LSB.

Duty cycle is the ratio, for a periodic digital signal, of the high level duration divided by the total period.

Effective Number of Bits (ENOB) is a method of specifying Signal-to-Noise and Distortion or SINAD. ENOB is defined as (SINAD - 1.76) / 6.02 and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

Full Power Bandwidth is a measure of the frequency at which the reconstructed output fundamental drops 3dB below its low frequency value for a full scale input.

Full Scale Error (single-ended input) is the deviation of the last code transition (111...110) to (111...111) from the ideal (AVCC - 1.5 LSB or -1LSB), after adjusting for offset error.

Positive Full Scale Error (differential input) is the deviation of the last code transition (111...110) to (111...111) from the ideal (AVCC - 1.5 LSB or -1LSB), after adjusting for offset error.

Negative Full Scale Error (differential input) is the deviation of the last code transition (111...110) to (111...111) from the ideal (-AVCC + 1.5 LSB or +1LSB), after adjusting for offset error.

Integral Non-Linearity(INL) is the deviation of each individual code from a line drawn from negative full scale (½ LSB below the first code transition) through positive full scale (½ LSB above the last code transition). The deviation of any given code from this straight line is measured from the center of that code value.

Intermodulation distortion (IMD) is the results of the product of two pure sinewaves at frequency fa and fb applied to the ADC input. To avoid clipping when the sinewave are in phase, the level must be just below -6dBFS. Assuming that the level of the two tones is equal, IMD2 is the difference in dBc between level(fa or fb) and level(fa ± fb). IMD3 is is the difference in dBc between level(fa or fb) and level(2fa ± fb) or level(fa ± 2fb).

Missing Codes are those output codes that will never appear at the ADC outputs. The ADC120 is guaranteed not to have any missing codes.

Offset Error (Single-ended input) is the deviation of the first code transition (000...000) to (000...001) from the ideal (i.e. GND +1 LSB).

Offset Error (Differential input) is the deviation of the mid-code transition (01…111) to (10…000) from the ideal (i.e. AVCC/2 +1 LSB).

Signal to Noise Ratio (SNR) is the ratio, expressed in dB, of the rms value of the fundamental of input signal to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or DC-component.

Signal to Noise Plus Distortion (S/N+D or SINAD) is the ratio of the rms value of the fundamental of input signal to the rms value of all of the other spectral components below half the sampling frequency, including harmonics but excluding DC-component.

Spurious Free Dynamic Range (SFDR) is the difference, expressed in dB, between the desired signal amplitude of fundamental to the amplitude of the peak spurious spectral component, where a spurious spectral component is any signal present in the output spectrum that is not present at the input and may or may not be a harmonic.

Total Harmonic Distortion (THD) is the ratio, expressed in dBc, of the rms total of the first nine harmonic components at the output to the rms level of fundamental of the input signal frequency as seen at the output. THD is calculated as THD = 20log10 [sqrt((Af2²+…+Af10²)/Af1²)]

where Af1 is the RMS power of the fundamental at the output and Af2 to Af10 are the RMS power in the first nine harmonic frequencies.

Throughput Time is the minimum time required between the start of two successive conversions. It is the acquisition time plus the conversion time.

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

6.1 TSSOP-16 package information

Figure 4. TSSOP-16 package outline

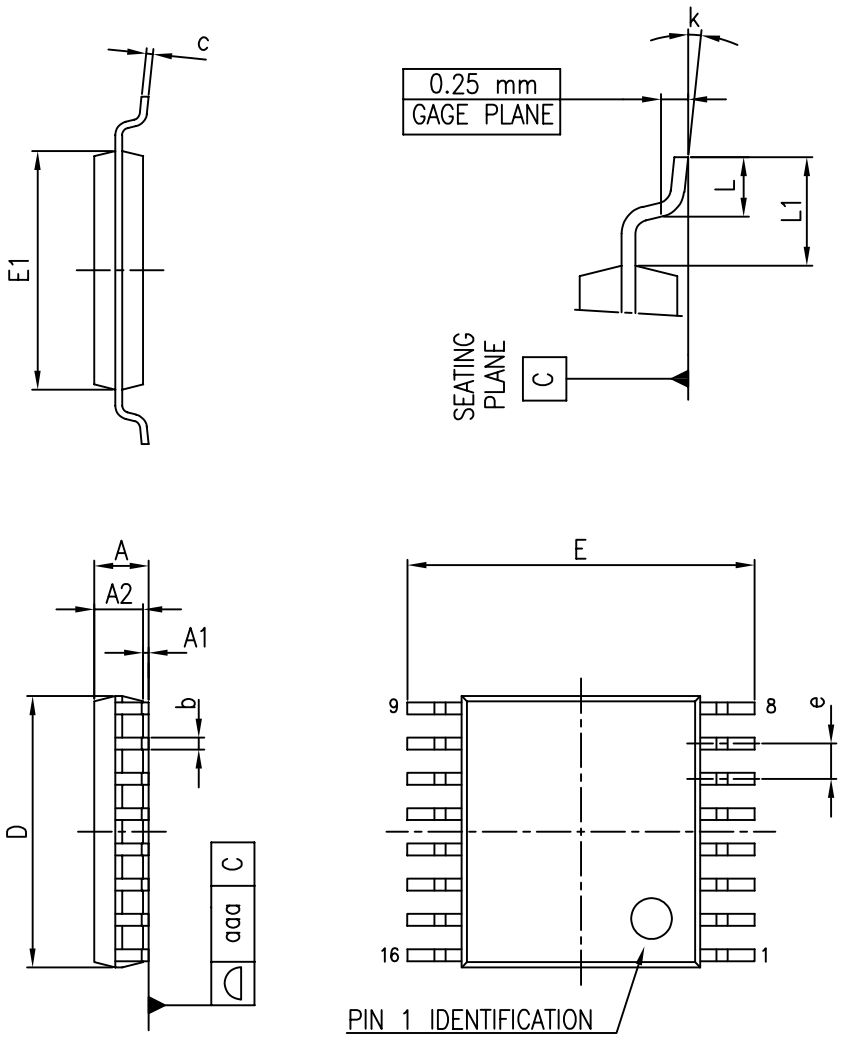


Table 7. **TSSOP-16 package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A			1.20
A1	0.05		0.15
A2	0.80	1.00	1.05
b	0.19		0.30
c	0.09		0.20
D	4.90	5.00	5.10
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e		0.65	
k	0°		8°
L	0.45	0.60	0.75
L1		1.00	
aaa			0.10

Revision history

Table 8. **Document revision history**

Date	Version	Changes
11-Apr-2019	1	Initial release.

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