

# 74AC175, 74ACT175 Quad D-Type Flip-Flop

## Features

- $I_{CC}$  reduced by 50%
- Edge-triggered D-type inputs
- Buffered positive edge-triggered clock
- Asynchronous common reset
- True and complement output
- Outputs source/sink 24mA
- ACT175 has TTL-compatible inputs

## General Description

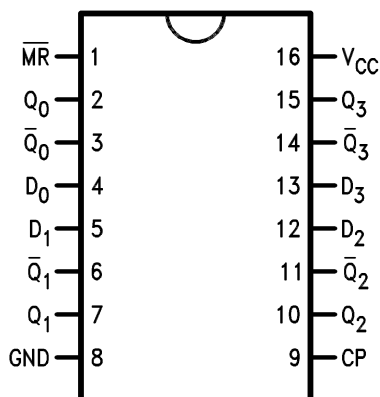
The AC/ACT175 is a high-speed quad D-type flip-flop. The device is useful for general flip-flop requirements where clock and clear inputs are common. The information on the D-type inputs is stored during the LOW-to-HIGH clock transition. Both true and complemented outputs of each flip-flop are provided. A Master Reset input resets all flip-flops, independent of the Clock or D-type inputs, when LOW.

## Ordering Information

Order Number	Package Number	Package Description
74AC175SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body
74AC175SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC175MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC175PC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74ACT175SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body
74ACT175SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ACT175MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

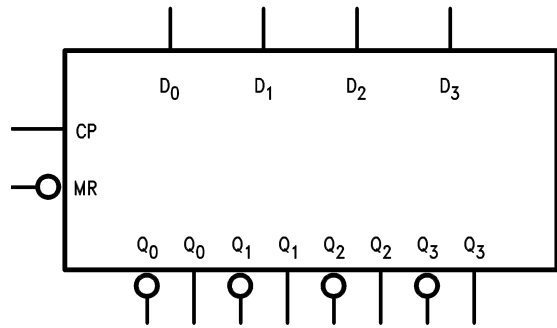
## Connection Diagram



## Pin Descriptions

Pin Names	Description
$D_0-D_3$	Data Inputs
CP	Clock Pulse Input
$\overline{MR}$	Master Reset Input
$Q_0-Q_3$	True Outputs
$\overline{Q_0}-\overline{Q_3}$	Complement Outputs

### Logic Symbol



### Functional Description

The AC/ACT175 consists of four edge-triggered D-type flip-flops with individual D inputs and Q and  $\bar{Q}$  outputs. The Clock and Master Reset are common. The four flip-flops will store the state of their individual D inputs on the LOW-to-HIGH clock (CP) transition, causing individual Q and  $\bar{Q}$  outputs to follow. A LOW input on the Master Reset ( $\overline{MR}$ ) will force all Q outputs LOW and  $\bar{Q}$  outputs HIGH independent of Clock or Data inputs. The AC/ACT175 is useful for general logic applications where a common Master Reset and Clock are acceptable.

### Truth Table

Inputs @ $t_n$ , $\overline{MR} = H$	Outputs @ $t_{n+1}$	
$D_n$	$Q_n$	$\bar{Q}_n$
L	L	H
H	H	L

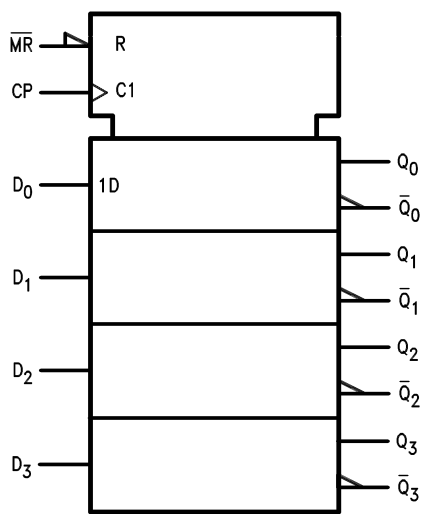
H = HIGH Voltage Level

L = LOW Voltage Level

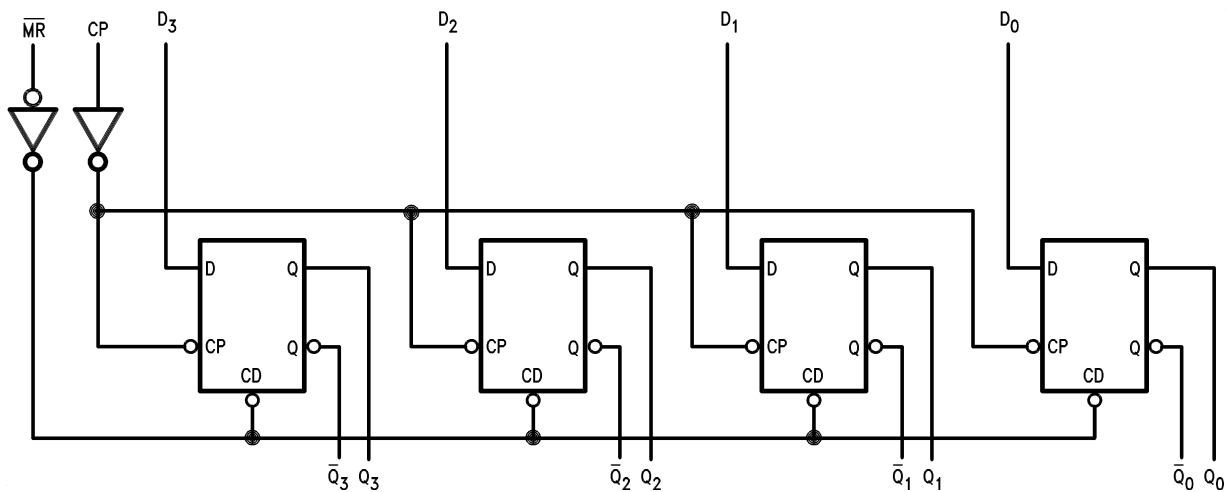
$t_n$  = Bit Time before Clock Pulse

$t_{n+1}$  = Bit Time after Clock Pulse

### IEEE/IEC



### Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure 1.

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
$V_{CC}$	Supply Voltage	-0.5V to +7.0V
$I_{IK}$	DC Input Diode Current $V_I = -0.5V$ $V_I = V_{CC} + 0.5V$	-20mA +20mA
$V_I$	DC Input Voltage	-0.5V to $V_{CC} + 0.5V$
$I_{OK}$	DC Output Diode Current $V_O = -0.5V$ $V_O = V_{CC} + 0.5V$	-20mA +20mA
$V_O$	DC Output Voltage	-0.5V to $V_{CC} + 0.5V$
$I_O$	DC Output Source or Sink Current	$\pm 50mA$
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ or Ground Current per Output Pin	$\pm 50mA$
$T_{STG}$	Storage Temperature	-65°C to +150°C
$T_J$	Junction Temperature	140°C

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
$V_{CC}$	Supply Voltage AC ACT	2.0V to 6.0V 4.5V to 5.5V
$V_I$	Input Voltage	0V to $V_{CC}$
$V_O$	Output Voltage	0V to $V_{CC}$
$T_A$	Operating Temperature	-40°C to +85°C
$\Delta V / \Delta t$	Minimum Input Edge Rate, AC Devices: $V_{IN}$ from 30% to 70% of $V_{CC}$ , $V_{CC}$ @ 3.3V, 4.5V, 5.5V	125mV/ns
$\Delta V / \Delta t$	Minimum Input Edge Rate, ACT Devices: $V_{IN}$ from 0.8V to 2.0V, $V_{CC}$ @ 4.5V, 5.5V	125mV/ns

## DC Electrical Characteristics for AC

Symbol	Parameter	V <sub>CC</sub> (V)	Conditions	T <sub>A</sub> = +25°C		T <sub>A</sub> = -40°C to +85°C		Units	
				Typ.	Guaranteed Limits				
V <sub>IH</sub>	Minimum HIGH Level Input Voltage	3.0	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V	1.5	2.1	2.1		V	
		4.5		2.25	3.15	3.15			
		5.5		2.75	3.85	3.85			
V <sub>IL</sub>	Maximum LOW Level Input Voltage	3.0	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V	1.5	0.9	0.9		V	
		4.5		2.25	1.35	1.35			
		5.5		2.75	1.65	1.65			
V <sub>OH</sub>	Minimum HIGH Level Output Voltage	3.0	I <sub>OUT</sub> = -50μA	2.99	2.9	2.9		V	
		4.5		4.49	4.4	4.4			
		5.5		5.49	5.4	5.4			
		3.0	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> : I <sub>OH</sub> = -12mA			2.56	2.46		
		4.5	I <sub>OH</sub> = -24mA			3.86	3.76		
		5.5	I <sub>OH</sub> = -24mA <sup>(1)</sup>			4.86	4.76		
V <sub>OL</sub>	Maximum LOW Level Output Voltage	3.0	I <sub>OUT</sub> = 50μA	0.002	0.1	0.1		V	
		4.5		0.001	0.1	0.1			
		5.5		0.001	0.1	0.1			
		3.0	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> : I <sub>OL</sub> = 12mA			0.36	0.44		
		4.5	I <sub>OL</sub> = 24mA			0.36	0.44		
		5.5	I <sub>OL</sub> = 24mA <sup>(1)</sup>			0.36	0.44		
I <sub>IN</sub> <sup>(3)</sup>	Maximum Input Leakage Current	5.5	V <sub>I</sub> = V <sub>CC</sub> , GND		±0.1	±1.0		μA	
I <sub>OLD</sub>	Minimum Dynamic Output Current <sup>(2)</sup>	5.5	V <sub>OLD</sub> = 1.65V Max.			75		mA	
I <sub>OHD</sub>		5.5	V <sub>OHD</sub> = 3.85V Min.			-75		mA	
I <sub>CC</sub> <sup>(3)</sup>	Maximum Quiescent Supply Current	5.5	V <sub>IN</sub> = V <sub>CC</sub> or GND		4.0	40.0		μA	

**Notes:**

1. All outputs loaded; thresholds on input associated with output under test.
2. Maximum test duration 2.0ms, one output loaded at a time.
3. I<sub>IN</sub> and I<sub>CC</sub> @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V<sub>CC</sub>.

## DC Electrical Characteristics for ACT

Symbol	Parameter	V <sub>CC</sub> (V)	Conditions	T <sub>A</sub> = +25°C		T <sub>A</sub> = -40°C to +85°C		Units
				Typ.	Guaranteed Limits			
V <sub>IH</sub>	Minimum HIGH Level Input Voltage	4.5	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V	1.5	2.0	2.0		V
		5.5		1.5	2.0	2.0		
V <sub>IL</sub>	Maximum LOW Level Input Voltage	4.5	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V	1.5	0.8	0.8		V
		5.5		1.5	0.8	0.8		
V <sub>OH</sub>	Minimum HIGH Level Output Voltage	4.5	I <sub>OUT</sub> = -50μA	4.49	4.4	4.4		V
		5.5		5.49	5.4	5.4		
		4.5	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> : I <sub>OH</sub> = -24mA		3.86	3.76		
		5.5		I <sub>OH</sub> = -24mA <sup>(4)</sup>		4.86	4.76	
V <sub>OL</sub>	Maximum LOW Level Output Voltage	4.5	I <sub>OUT</sub> = 50μA	0.001	0.1	0.1		V
		5.5		0.001	0.1	0.1		
		4.5	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> : I <sub>OL</sub> = 24mA		0.36	0.44		
		5.5		I <sub>OL</sub> = 24mA <sup>(4)</sup>		0.36	0.44	
I <sub>IN</sub>	Maximum Input Leakage Current	5.5	V <sub>I</sub> = V <sub>CC</sub> , GND		±0.1	±1.0		μA
I <sub>CCT</sub>	Maximum I <sub>CC</sub> /Input	5.5	V <sub>I</sub> = V <sub>CC</sub> - 2.1V	0.6		1.5		mA
I <sub>OLD</sub>	Minimum Dynamic Output Current <sup>(5)</sup>	5.5	V <sub>OLD</sub> = 1.65V Max.			75		mA
I <sub>OHD</sub>		5.5	V <sub>OHD</sub> = 3.85V Min.			-75		mA
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5	V <sub>IN</sub> = V <sub>CC</sub> or GND		4.0	40.0		μA

**Notes:**

- All outputs loaded; thresholds on input associated with output under test.
- Maximum test duration 2.0ms, one output loaded at a time.

## AC Electrical Characteristics for AC

Symbol	Parameter	$V_{CC}$ (V) <sup>(6)</sup>	$T_A = +25^\circ\text{C}$ , $C_L = 50\text{pF}$			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ , $C_L = 50\text{pF}$		Units
			Min.	Typ.	Max.	Min.	Max.	
$f_{\text{MAX}}$	Maximum Clock Frequency	3.3	149	214		139		MHz
		5.0	187	244		187		
$t_{\text{PLH}}$	Propagation Delay, CP to $Q_n$ or $\overline{Q}_n$	3.3	2.0	9.5	12.0	2.0	13.5	ns
		5.0	1.5	7.0	9.0	1.0	9.5	
$t_{\text{PHL}}$	Propagation Delay, CP to $Q_n$ or $\overline{Q}_n$	3.3	2.5	8.5	13.0	2.0	14.5	ns
		5.0	1.5	6.0	9.5	1.5	10.5	
$t_{\text{PLH}}$	Propagation Delay, $\overline{\text{MR}}$ to $Q_n$	3.3	3.0	7.5	12.5	2.5	13.5	ns
		5.0	2.0	5.5	9.0	1.5	10.0	
$t_{\text{PHL}}$	Propagation Delay, $\overline{\text{MR}}$ to $Q_n$	3.3	3.0	8.5	11.0	2.5	12.5	ns
		5.0	2.0	6.0	8.5	1.5	9.0	

## Note:

6. Voltage range 3.3 is  $3.3\text{V} \pm 0.3\text{V}$ . Voltage range 5.0 is  $5.0\text{V} \pm 0.5\text{V}$ .

## AC Operating Requirements for AC

Symbol	Parameter	$V_{CC}$ (V) <sup>(7)</sup>	$T_A = +25^\circ\text{C}$ , $C_L = 50\text{pF}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ , $C_L = 50\text{pF}$		Units
			Typ.	Guaranteed Minimum			
$t_S$	Setup Time, HIGH or LOW, $D_n$ to CP	3.3	2.0	4.5	4.5		ns
		5.0	1.0	3.0	3.0		
$t_H$	Hold Time, HIGH or LOW, $D_n$ to CP	3.3	1.0	1.0	1.0		ns
		5.0	1.0	1.0	1.0		
$t_W$	CP Pulse Width, HIGH or LOW	3.3	2.5	4.5	4.5		ns
		5.0	2.0	3.5	3.5		
$t_W$	$\overline{\text{MR}}$ Pulse Width, LOW	3.3	2.5	4.5	5.0		ns
		5.0	2.0	3.5	3.5		
$t_{\text{REC}}$	Recovery Time, $\overline{\text{MR}}$ to CP	3.3	-2.0	0	0		ns
		5.0	-1.0	0	0		

## Note:

7. Voltage range 3.3 is  $3.3\text{V} \pm 0.3\text{V}$ . Voltage range 5.0 is  $5.0\text{V} \pm 0.5\text{V}$ .

## AC Electrical Characteristics for ACT

Symbol	Parameter	$V_{CC}$ (V) <sup>(8)</sup>	$T_A = +25^\circ\text{C}$ , $C_L = 50\text{pF}$			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ , $C_L = 50\text{pF}$		Units
			Min.	Typ.	Max.	Min.	Max.	
$f_{MAX}$	Maximum Clock Frequency	5.0	175	236		145		MHz
$t_{PLH}$	Propagation Delay, CP to $Q_n$ or $\overline{Q}_n$	5.0	2.0	6.0	10.0	1.5	11.0	ns
$t_{PHL}$	Propagation Delay, CP to $Q_n$ or $\overline{Q}_n$	5.0	2.0	7.0	11.0	1.5	12.0	ns
$t_{PLH}$	Propagation Delay, $\overline{MR}$ to $\overline{Q}_n$	5.0	2.0	6.0	9.5	1.5	10.5	ns
$t_{PHL}$	Propagation Delay, $\overline{MR}$ to $Q_n$	5.0	2.0	5.5	9.5	1.5	10.5	ns

**Note:**8. Voltage Range 5.0 is  $5.0\text{V} \pm 0.5\text{V}$ .

## AC Operating Requirements for ACT

Symbol	Parameter	$V_{CC}$ (V) <sup>(9)</sup>	$T_A = +25^\circ\text{C}$ , $C_L = 50\text{pF}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ , $C_L = 50\text{pF}$		Units
			Typ.	Guaranteed Minimum			
$t_S$ (H)	Setup Time, $D_n$ to CP	5.0	3.0	2.0	2.0		ns
$t_S$ (L)			3.0	2.5	2.5		
$t_H$	Hold Time, HIGH or LOW, $D_n$ to CP	5.0	0	1.0	1.0		ns
$t_W$	CP Pulse Width, HIGH or LOW	5.0	4.0	3.0	3.5		ns
$t_W$	$\overline{MR}$ Pulse Width, LOW	5.0	4.0	3.0	4.0		ns
$t_{rec}$	Recovery Time, $\overline{MR}$ to CP	5.0	0	0	0		ns

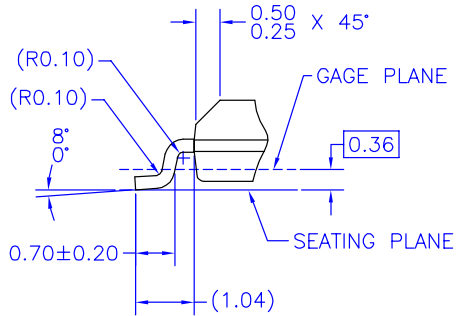
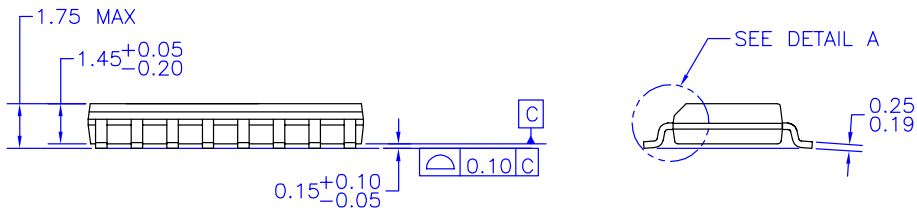
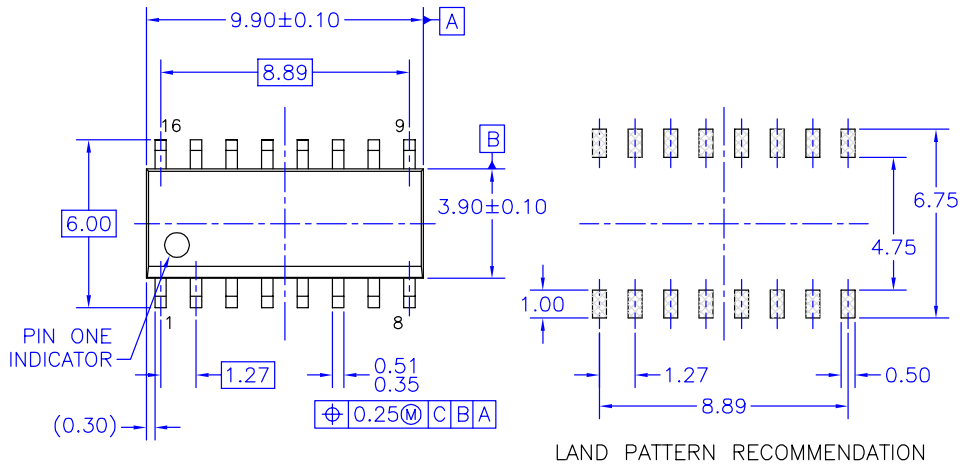
**Note:**9. Voltage Range 5.0 is  $5.0\text{V} \pm 0.5\text{V}$ .

## Capacitance

Symbol	Parameter	Conditions	Typ.	Units
$C_{IN}$	Input Capacitance	$V_{CC} = \text{OPEN}$	4.5	pF
$C_{PD}$	Power Dissipation Capacitance	$V_{CC} = 5.0\text{V}$	45.0	pF

### Physical Dimensions

Dimensions are in millimeters unless otherwise noted.



DETAIL A  
SCALE: 2:1

NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AC, ISSUE C, DATED MAY 1990.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) STANDARD LEAD FINISH:  
200 MICRONS / 5.08 MICRONS MIN.  
LEAD/TIN (SOLDER) ON COPPER.

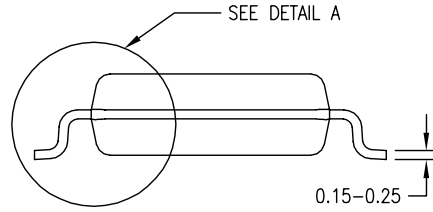
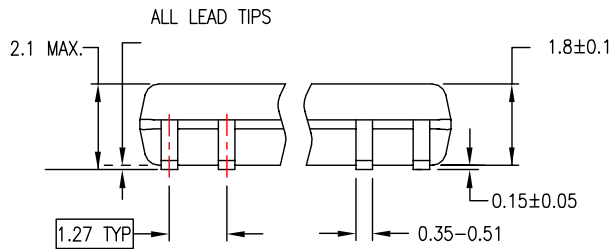
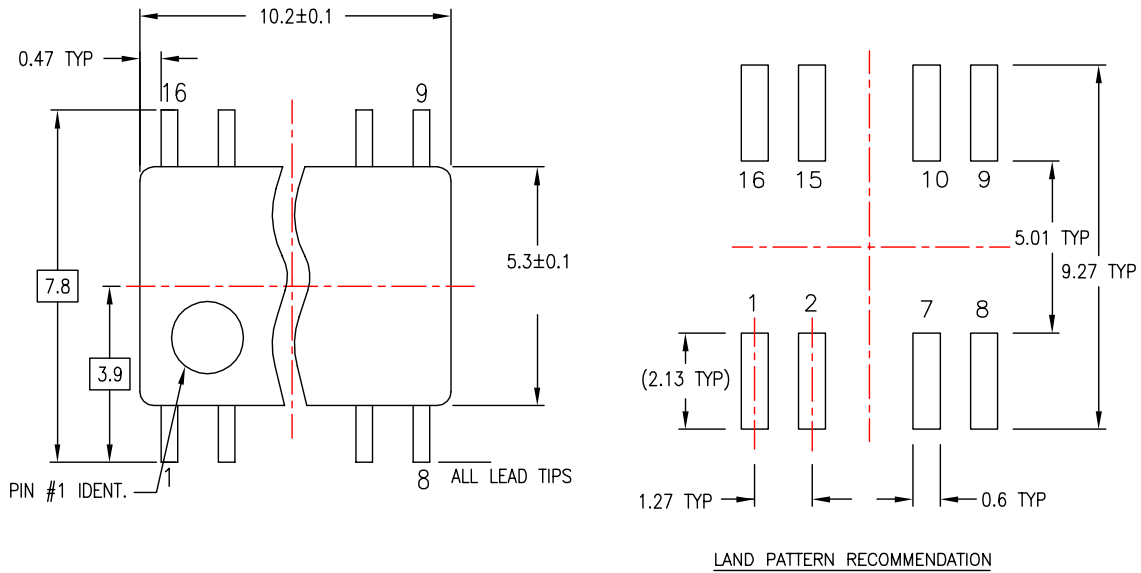
M16AREVK

**Figure 2. 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M16A**



**Physical Dimensions** (Continued)

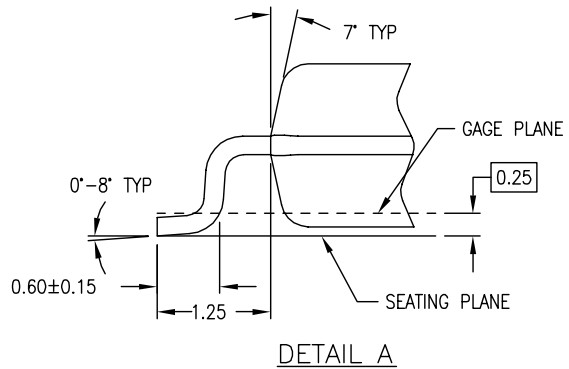
Dimensions are in millimeters unless otherwise noted.



DIMENSIONS ARE IN MILLIMETERS

NOTES:

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

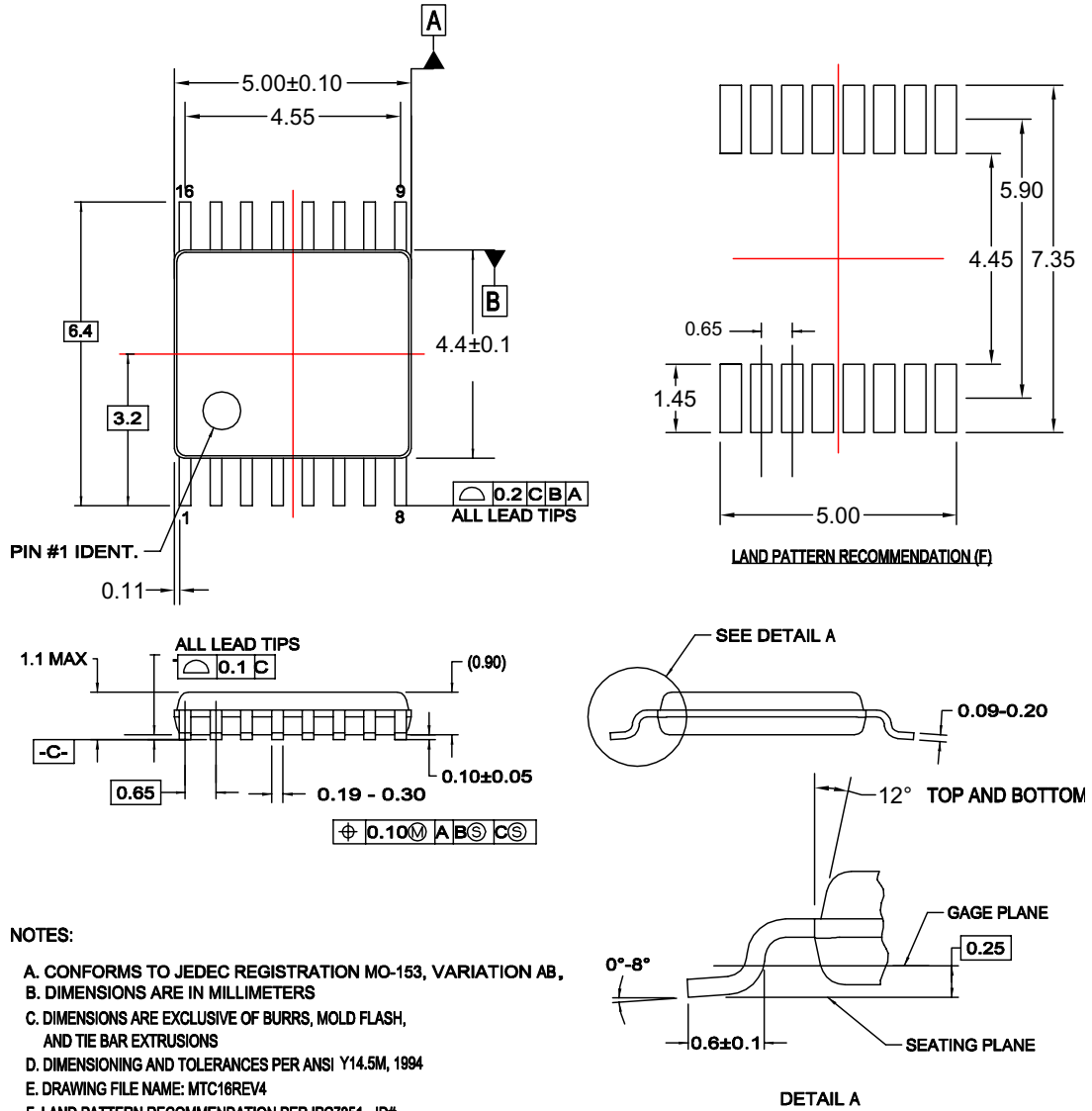


M16DREVC

**Figure 3. 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M16D**

**Physical Dimensions** (Continued)

Dimensions are in millimeters unless otherwise noted.



MTC16rev4

**Figure 4. 16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC16**

**Physical Dimensions** (Continued)

Dimensions are in inches (millimeters) unless otherwise noted.

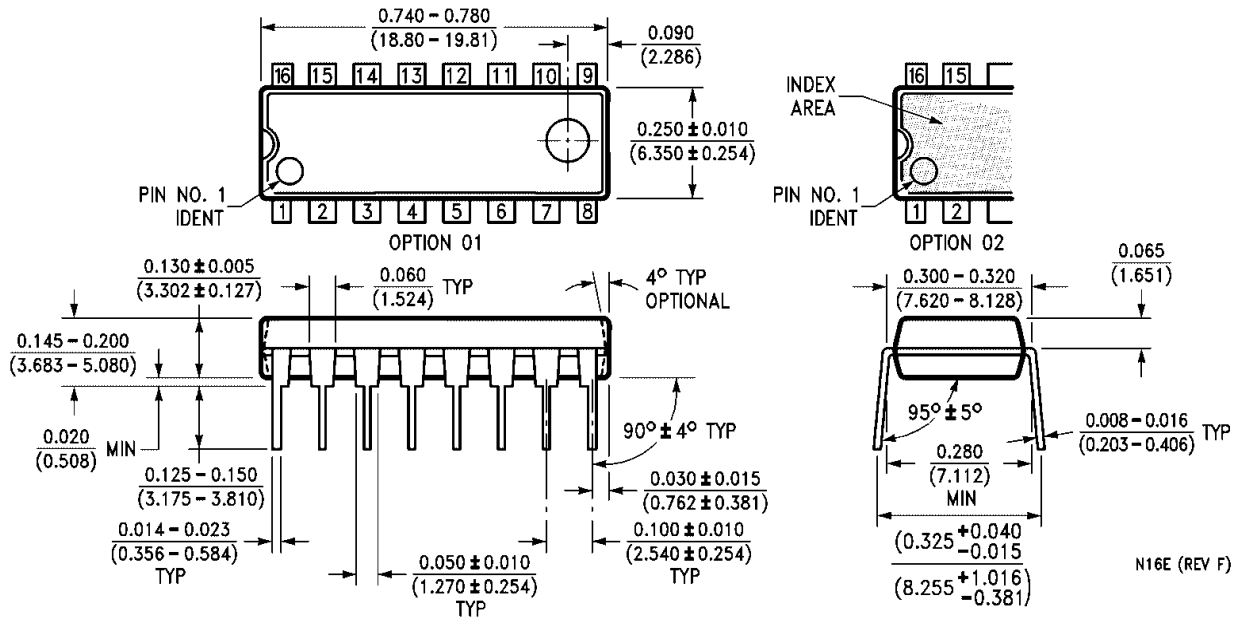



Figure 5. 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N16E

N16E (REV F)

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ActiveArray <sup>™</sup>	ImpliedDisconnect <sup>™</sup>	QS <sup>™</sup>	TinyPower <sup>™</sup>
Bottomless <sup>™</sup>	IntelliMAX <sup>™</sup>	QT Optoelectronics <sup>™</sup>	TinyWire <sup>™</sup>
Build it Now <sup>™</sup>	ISOPLANAR <sup>™</sup>	Quiet Series <sup>™</sup>	TruTranslation <sup>™</sup>
CoolFET <sup>™</sup>	MICROCOUPLER <sup>™</sup>	RapidConfigure <sup>™</sup>	μSerDes <sup>™</sup>
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Current Transfer Logic <sup>™</sup>	MSX <sup>™</sup>	SMART START <sup>™</sup>	VCX <sup>™</sup>
DOME <sup>™</sup>	MSXPro <sup>™</sup>	SPM <sup>®</sup>	Wire <sup>™</sup>
E <sup>2</sup> CMOS <sup>™</sup>	OCX <sup>™</sup>	STEALTH <sup>™</sup>	
EcoSPARK <sup>®</sup>	OCXPro <sup>™</sup>	SuperFET <sup>™</sup>	
EnSigna <sup>™</sup>	OPTOLOGIC <sup>®</sup>	SuperSOT <sup>™</sup> -3	
FACT Quiet Series <sup>™</sup>	OPTOPLANAR <sup>®</sup>	SuperSOT <sup>™</sup> -6	
FACT <sup>®</sup>	PACMAN <sup>™</sup>	SuperSOT <sup>™</sup> -8	
FAST <sup>®</sup>	POP <sup>™</sup>	SyncFET <sup>™</sup>	
FASTr <sup>™</sup>	Power220 <sup>®</sup>	TCM <sup>™</sup>	
FPS <sup>™</sup>	Power247 <sup>®</sup>	The Power Franchise <sup>®</sup>	
FRFET <sup>®</sup>	PowerEdge <sup>™</sup>	 ™	
GlobalOptoisolator <sup>™</sup>	PowerSaver <sup>™</sup>	TinyBoost <sup>™</sup>	
GTO <sup>™</sup>	PowerTrench <sup>®</sup>	TinyBuck <sup>™</sup>	

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As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

## PRODUCT STATUS DEFINITIONS

### Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild Semiconductor. The datasheet is printed for reference information only.

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