FINAL

Am29F010

1 Megabit (128 K x 8-bit)
CMOS 5.0 Volt-only, Uniform Sector Flash Memory

DISTINCTIVE CHARACTERISTICS

- **Single power supply operation**
  - — 5.0 V ± 10% for read, erase, and program operations
  - — Simplifies system-level power requirements
- **High performance**
  - — 45 ns maximum access time
- **Low power consumption**
  - — 30 mA max active read current
  - — 50 mA max program/erase current
  - — <25 µA typical standby current
- **Flexible sector architecture**
  - — Eight uniform sectors
  - — Any combination of sectors can be erased
  - — Supports full chip erase
- **Sector protection**
  - — Hardware-based feature that disables/re-enables program and erase operations in any combination of sectors
  - — Sector protection/unprotection can be implemented using standard PROM programming equipment
- **Embedded Algorithms**
  - — Embedded Erase algorithm automatically pre-programs and erases the chip or any combination of designated sector
  - — Embedded Program algorithm automatically programs and verifies data at specified address
- **Minimum 100,000 program/erase cycles guaranteed**
- **Package options**
  - — 32-pin PLCC
  - — 32-pin TSOP
  - — 32-pin PDIP
- **Compatible with JEDEC standards**
  - — Pinout and software compatible with single-power-supply flash
  - — Superior inadvertent write protection
- **Data# Polling and Toggle Bits**
  - — Provides a software method of detecting program or erase cycle completion

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GENERAL DESCRIPTION

The Am29F010 is a 1 Mbit, 5.0 Volt-only Flash memory organized as 131,072 bytes. The Am29F010 is offered in 32-pin PLCC, TSOP, and PDIP packages. The byte-wide data appears on DQ0-DQ7. The device is designed to be programmed in-system with the standard system 5.0 Volt V_{CC} supply. A 12.0 volt V_{PP} is not required for program or erase operations. The device can also be programmed or erased in standard EPROM programmers.

The standard device offers access times of 45, 55, 70, 90, and 120 ns, allowing high-speed microprocessors to operate without wait states. To eliminate bus contention the device has separate chip enable (CE#), write enable (WE#) and output enable (OE) controls.

The device requires only a **single 5.0 volt power supply** for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

The device is entirely command set compatible with the **JEDEC single-power-supply Flash standard**. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device programming occurs by executing the program command sequence. This invokes the **Embedded Program** algorithm—an internal algorithm that automatically times the program pulse widths and verifies proper cell margin.

Device erasure occurs by executing the erase command sequence. This invokes the **Embedded Erase** algorithm—an internal algorithm that automatically preprograms the array (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The host system can detect whether a program or erase operation is complete by reading the DQ7 (Data# Polling) and DQ6 (toggle) **status bits**. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is erased when shipped from the factory.

The **hardware data protection** measures include a low V_{CC} detector automatically inhibits write operations during power transitions. The **hardware sector protection** feature disables both program and erase operations in any combination of the sectors of memory, and is implemented using standard EPROM programmers.

The system can place the device into the **standby mode**. Power consumption is greatly reduced in this mode.

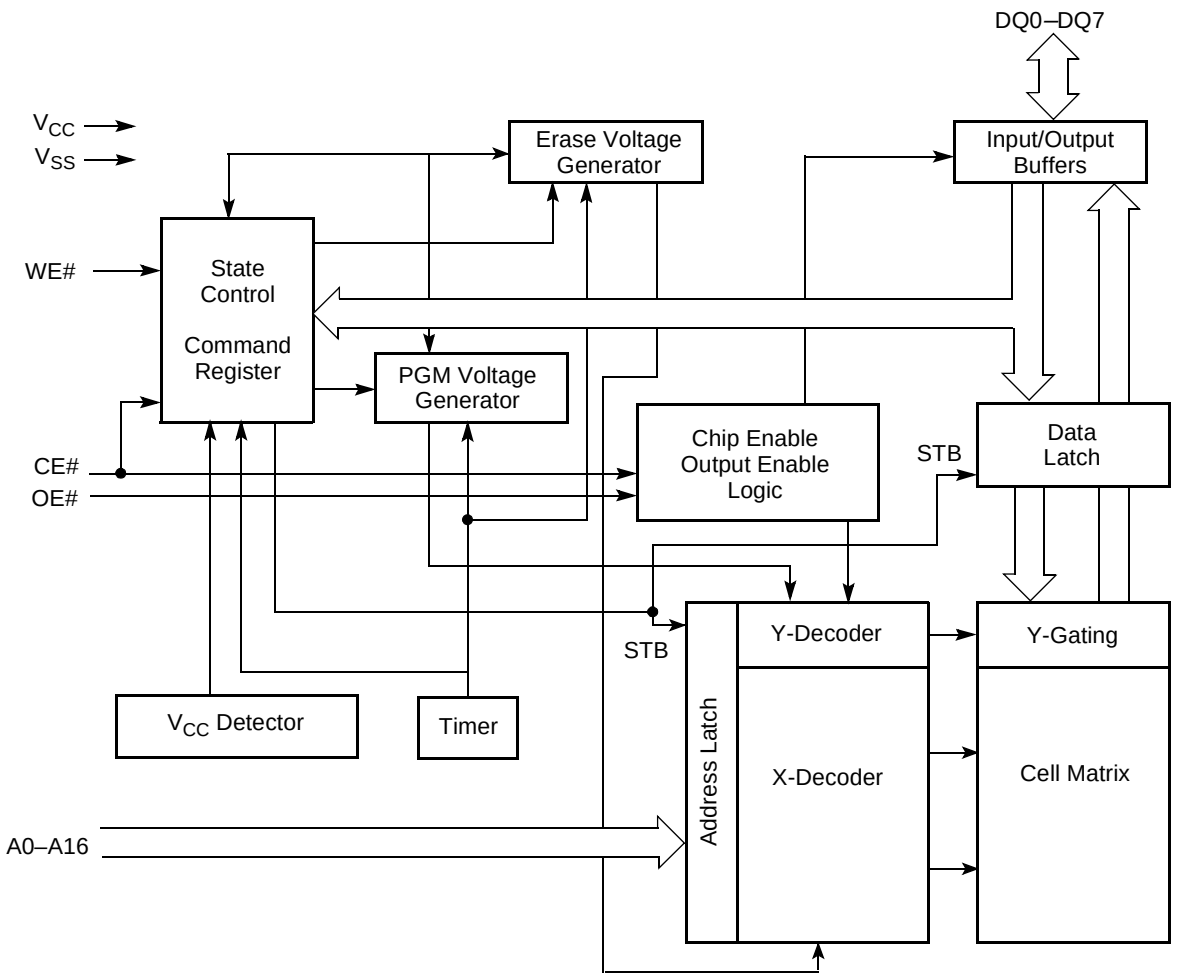
AMD's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability, and cost effectiveness. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The bytes are programmed one byte at a time using the EPROM programming mechanism of hot electron injection.

PRODUCT SELECTOR GUIDE

Family Part Number		Am29F010				
Speed Option	V_{CC} = 5.0 V ± 5%	**-45**	**-55 (P)**			
	V_{CC} = 5.0 V ± 10%		**-55 (J, E, F)**	**-70**	**-90**	**-120**
Max Access Time (ns)		45	55	70	90	120
CE# Access (ns)		45	55	70	90	120
OE# Access (ns)		25	30	30	35	50

Note: *See the AC Characteristics section for full specifications.*

BLOCK DIAGRAM



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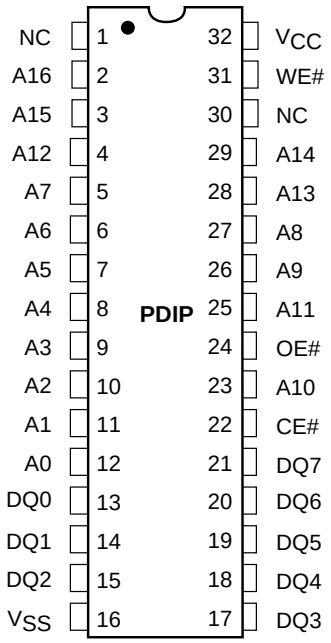
CONNECTION DIAGRAMS



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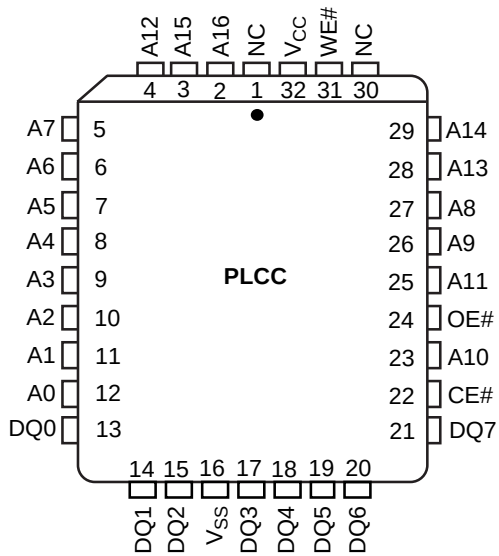

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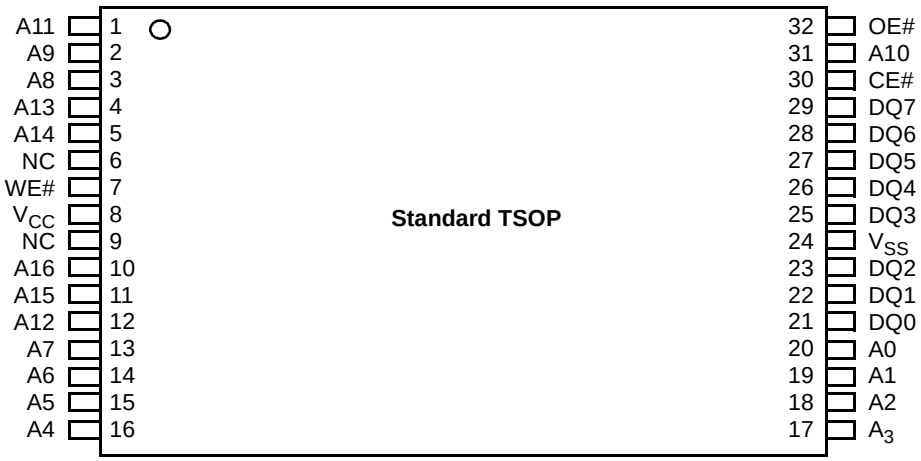

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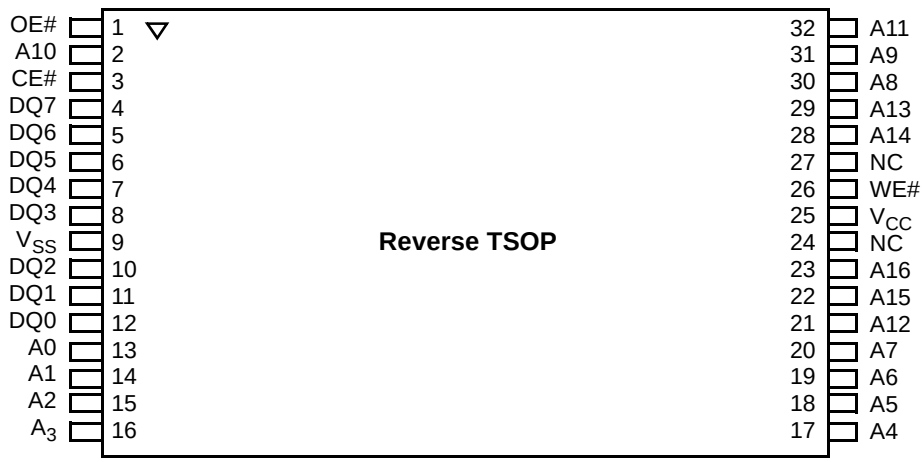
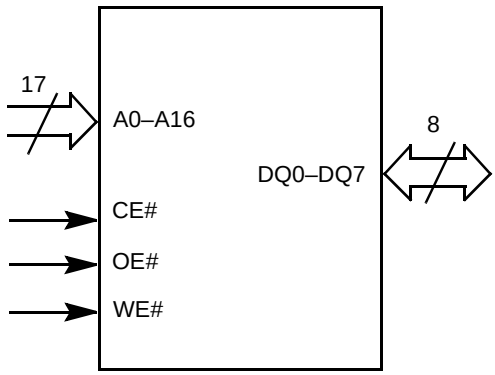


16736G-5

PIN CONFIGURATION

A0–A16	=	17 Addresses
DQ0–DQ7	=	8 Data Inputs/Outputs
CE#	=	Chip Enable
OE#	=	Output Enable
WE#	=	Write Enable
V_{CC}	=	+5.0 Volt Single Power Supply (See Product Selector Guide for speed options and voltage supply tolerances)
V_{SS}	=	Device Ground
NC	=	Pin Not Connected Internally

LOGIC SYMBOL

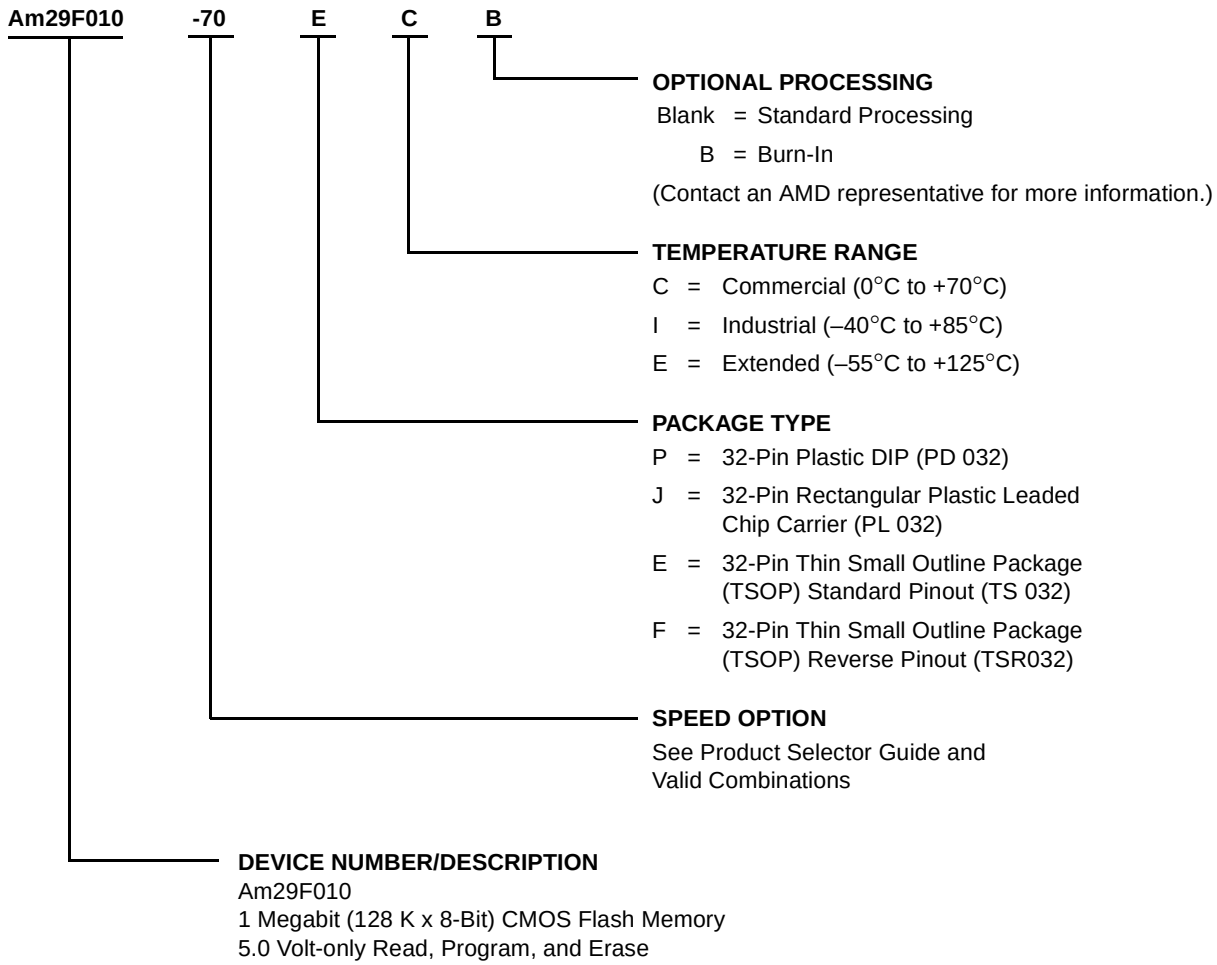


16736G-6

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations	
AM29F010-45	PC, PI, PE, JC, JI, JE, EC, EI, EE, FC, FI, FE
AM29F010-55 V_{CC} = 5.0 V ± 5%	PC5, PI5, PE5
AM29F010-55 V_{CC} = 5.0 V ± 10%	JC, JI, JE, EC, EI, EE, FC, FI, FE
AM29F010-70 AM29F010-90 AM29F010-120	PC, PI, PE, JC, JI, JE, EC, EI, EE, FC, FI, FE

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

DEVICE BUS OPERATIONS

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is composed of latches that store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. The appropriate device bus operations table lists the inputs and control levels required, and the resulting output. The following subsections describe each of these operations in further detail.

Table 1. Am29F010 Device Bus Operations

Operation	CE#	OE#	WE#	Addresses (Note 1)	DQ0–DQ7
Read	L	L	H	A_{IN}	D_{OUT}
Write	L	H	L	A_{IN}	D_{IN}
Standby	V_{CC} ± 0.5 V	X	X	X	High-Z
Output Disable	L	H	H	X	High-Z
Hardware Reset	X	X	X	X	High-Z
Temporary Sector Unprotect	X	X	X	A_{IN}	D_{IN}

Legend:

L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{ID} = 12.0± 0.5 V, X = Don't Care, A_{IN} = Addresses In, D_{IN} = Data In, D_{OUT} = Data Out

Notes:

1. *Addresses are A16:A0.*
2. *The sector protect and sector unprotect functions must be implemented via programming equipment. See the "Sector Protection/Unprotection" section.*

Requirements for Reading Array Data

To read array data from the outputs, the system must drive the CE# and OE# pins to V_{IL}. CE# is the power control and selects the device. OE# is the output control and gates array data to the output pins. WE# should remain at V_{IH}.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. The device remains enabled for read access until the command register contents are altered.

See "Reading Array Data" for more information. Refer to the AC Read Operations table for timing specifications and to the Read Operations Timings diagram for the timing waveforms. I_{CC1} in the DC Characteristics table represents the active current specification for reading array data.

Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive WE# and CE# to V_{IL}, and OE# to V_{IH}.

An erase operation can erase one sector, multiple sectors, or the entire device. The Sector Address Tables indicate the address space that each sector occupies. A "sector address" consists of the address bits required to uniquely select a sector. See the "Command Definitions" section for details on erasing a sector or the entire chip.

After the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ7–DQ0. Standard read cycle timings apply in this mode. Refer to the "Autoselect Mode" and "Autoselect Command Sequence" sections for more information.

I_{CC2} in the DC Characteristics table represents the active current specification for the write mode. The "AC Characteristics" section contains timing specification tables and timing diagrams for write operations.

Program and Erase Operation Status

During an erase or program operation, the system may check the status of the operation by reading the status bits on DQ7–DQ0. Standard read cycle timings and I_{CC} read specifications apply. Refer to "Write Operation Status" for more information, and to each AC Characteristics section in the appropriate data sheet for timing diagrams.

Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE# pin is held at $V_{CC} \pm 0.5$ V. (Note that this is a more restricted voltage range than V_{IH}.) The device enters the TTL standby mode when CE# is held at V_{IH}. The device requires the standard access time (t_{CE}) before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

I_{CC3} in the DC Characteristics tables represents the standby current specification.

Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled. The output pins are placed in the high impedance state.

Table 2. Am29F010 Sector Addresses Table

Sector	A16	A15	A14	Address Range
SA0	0	0	0	00000h-03FFFh
SA1	0	0	1	04000h-07FFFh
SA2	0	1	0	08000h-0BFFFh
SA3	0	1	1	0C000h-0FFFFh
SA4	1	0	0	10000h-13FFFh
SA5	1	0	1	14000h-17FFFh
SA6	1	1	0	18000h-1BFFFh
SA7	1	1	1	1C000h-1FFFFh

Autoselect Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output on DQ7–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires V_{ID} (11.5 V to 12.5 V) on address pin A9. Address pins A6, A1, and A0 must be as shown in Autoselect Codes (High Voltage Method) table. In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits. Refer to the corresponding Sector Address Tables. The Command Definitions table shows the remaining address bits that are don't care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on DQ7–DQ0.

To access the autoselect codes in-system, the host system can issue the autoselect command via the command register, as shown in the Command Definitions table. This method does not require V_{ID}. See "Command Definitions" for details on using the autoselect mode.

Table 3. Am29F010 Autoselect Codes (High Voltage Method)

Description	CE#	OE#	WE#	A16 to A14	A13 to A10	A9	A8 to A7	A6	A5 to A2	A1	A0	DQ7 to DQ0
Manufacturer ID: AMD	L	L	H	X	X	V_{ID}	X	L	X	L	L	01h
Device ID: Am29F010	L	L	H	X	X	V_{ID}	X	L	X	L	H	20h
Sector Protection Verification	L	L	H	SA	X	V_{ID}	X	L	X	H	L	01h (protected)
												00h (unprotected)

L = Logic Low = V_{IL}, H = Logic High = V_{IH}, SA = Sector Address, X = Don't care.

Sector Protection/Unprotection

The hardware sector protection feature disables both program and erase operations in any sector. The hardware sector unprotection feature re-enables both program and erase operations in previously protected sectors.

Sector protection/unprotection must be implemented using programming equipment. The procedure requires a high voltage (V_{ID}) on address pin A9 and the control pins. Details on this method are provided in a supplement, publication number 20495. Contact an AMD representative to obtain a copy of the appropriate document.

The device is shipped with all sectors unprotected. AMD offers the option of programming and protecting sectors at its factory prior to shipping the device through AMD's ExpressFlash™ Service. Contact an AMD representative for details.

It is possible to determine whether a sector is protected or unprotected. See "Autoselect Mode" for details.

Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes (refer to the Command Definitions table). In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control pins to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

Write Pulse "Glitch" Protection

Noise pulses of less than 5 ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

Logical Inhibit

Write cycles are inhibited by holding any one of OE# = V_{IL}, CE# = V_{IH} or WE# = V_{IH}. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one.

Power-Up Write Inhibit

If WE# = CE# = V_{IL} and OE# = V_{IH} during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to reading array data on power-up.

COMMAND DEFINITIONS

Writing specific address and data commands or sequences into the command register initiates device operations. The Command Definitions table defines the valid register command sequences. Writing **incorrect address and data values** or writing them in the **improper sequence** resets the device to reading array data.

All addresses are latched on the falling edge of WE# or CE#, whichever happens later. All data is latched on the rising edge of WE# or CE#, whichever happens first. Refer to the appropriate timing diagrams in the "AC Characteristics" section.

Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is also ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

The system *must* issue the reset command to re-enable the device for reading array data if DQ5 goes high, or while in the autoselect mode. See the "Reset Command" section, next.

See also "Requirements for Reading Array Data" in the "Device Bus Operations" section for more information. The Read Operations table provides the read parameters, and Read Operation Timings diagram shows the timing diagram.

Reset Command

Writing the reset command to the device resets the device to reading array data. Address bits are don't care for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to reading array data. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the device to reading array data. Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command *must* be written to return to reading array data.

If DQ5 goes high during a program or erase operation, writing the reset command returns the device to reading array data.

Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and devices codes, and determine whether or not a sector is protected. The Command Definitions table shows the address and data requirements. This method is an alternative to that shown in the Autoselect Codes (High Voltage Method) table, which is intended for PROM programmers and requires V_{ID} on address bit A9.

The autoselect command sequence is initiated by writing two unlock cycles, followed by the autoselect command. The device then enters the autoselect mode, and the system may read at any address any number of times, without initiating another command sequence.

A read cycle at address XX00h or retrieves the manufacturer code. A read cycle at address XX01h returns the device code. A read cycle containing a sector address (SA) and the address 02h in returns 01h if that sector is protected, or 00h if it is unprotected. Refer to the Sector Address tables for valid sector addresses.

The system must write the reset command to exit the autoselect mode and return to reading array data.

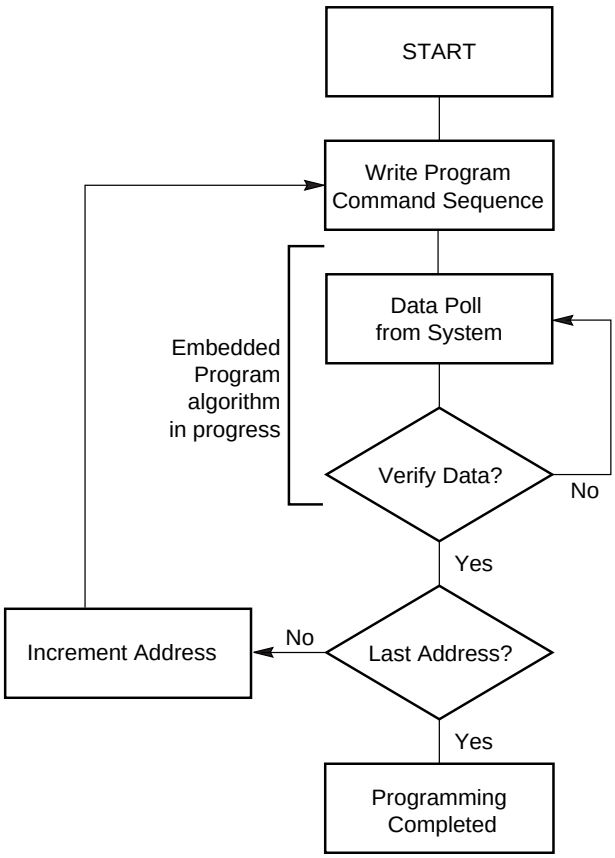
Byte Program Command Sequence

Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is *not* required to provide further controls or timings. The device automatically provides internally generated program pulses and verify the programmed cell margin. The Command Definitions take shows the address and data requirements for the byte program command sequence.

When the Embedded Program algorithm is complete, the device then returns to reading array data and addresses are no longer latched. The system can determine the status of the program operation by using DQ7or DQ6. See "Write Operation Status" for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored.

Programming is allowed in any sequence and across sector boundaries. **A bit cannot be programmed from a "0" back to a "1".** Attempting to do so may halt the operation and set DQ5 to "1", or cause the Data# Polling algorithm to indicate the operation was successful. However, a succeeding read will show that the data is still "0". Only erase operations can convert a "0" to a "1".



Note: *See the appropriate Command Definitions table for program command sequence.*

Figure 1. Program Operation

Chip Erase Command Sequence

Chip erase is a six-bus-cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. The Command Definitions table shows the address and data requirements for the chip erase command sequence.

Any commands written to the chip during the Embedded Erase algorithm are ignored.

The system can determine the status of the erase operation by using DQ7 or DQ6. See “Write Operation Status” for information on these status bits. When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched.

Figure 2 illustrates the algorithm for the erase operation. See the Erase/Program Operations tables in “AC Characteristics” for parameters, and to the Chip/Sector Erase Operation Timings for timing waveforms.

Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the address of the sector to be erased, and the sector erase command. The Command Definitions table shows the address and data requirements for the sector erase command sequence.

The device does *not* require the system to preprogram the memory prior to erase. The Embedded Erase algorithm automatically programs and verifies the sector for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase time-out of 50 µs begins. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50 µs, otherwise the last address and command might not be accepted, and erasure may begin. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is

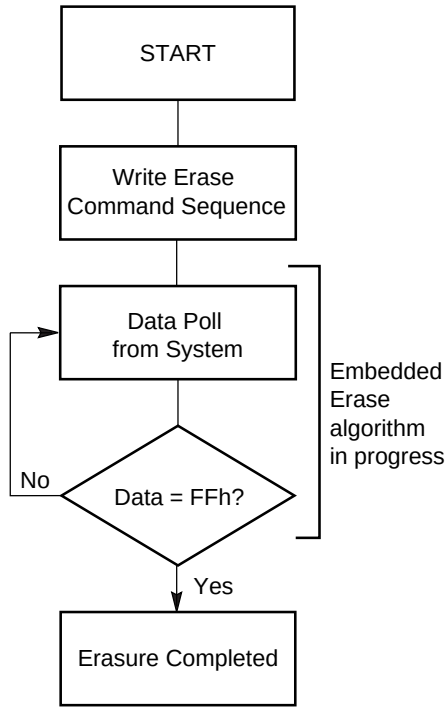
written. If the time between additional sector erase commands can be assumed to be less than 50 µs, the system need not monitor DQ3. **Any command during the time-out period resets the device to reading array data.** The system must rewrite the command sequence and any additional sector addresses and commands.

The system can monitor DQ3 to determine if the sector erase timer has timed out. (See the "DQ3: Sector Erase Timer" section.) The time-out begins from the rising edge of the final WE# pulse in the command sequence.

Once the sector erase operation has begun, all other commands are ignored.

When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7 or DQ6. Refer to "Write Operation Status" for information on these status bits.

Figure 2 illustrates the algorithm for the erase operation. Refer to the Erase/Program Operations tables in the "AC Characteristics" section for parameters, and to the Sector Erase Operations Timing diagram for timing waveforms.



Notes:

1. *See the appropriate Command Definitions table for erase command sequence.*
2. *See "DQ3: Sector Erase Timer" for more information.*

Figure 2. Erase Operation

Table 4. Am2F010 Command Definitions

Command Sequence (Note 1)		Cycles	Bus Cycles (Notes 2-3)											
			First		Second		Third		Fourth		Fifth		Sixth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (Note 4)		1	RA	RD										
Reset (Note 5)		1	XXXX	F0										
Autoselect (Note 6)	Manufacturer ID	4	5555	AA	2AAA	55	5555	90	XX00	01				
	Device ID	4	5555	AA	2AAA	55	5555	90	XX01	20				
	Sector Protect Verify (Note 7)	4	5555	AA	2AAA	55	5555	90	(SA) X02	00				
										01				
Program		4	5555	AA	2AAA	55	5555	A0	PA	PD				
Chip Erase		6	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	5555	10
Sector Erase		6	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	SA	30

Legend:

X = Don't care

RA = Address of the memory location to be read.

RD = Data read from location RA during read operation.

PA = Address of the memory location to be programmed. Addresses latch on the falling edge of the WE# or CE# pulse, whichever happens later.

PD = Data to be programmed at location PA. Data latches on the rising edge of WE# or CE# pulse, whichever happens first.

SA = Address of the sector to be verified (in autoselect mode) or erased. Address bits A16–A14 uniquely select any sector.

Notes:

1. *See Table 1 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Except when reading array or autoselect data, all command bus cycles are write operations.*
4. *No unlock or command cycles required when reading array data.*
5. *The Reset command is required to return to reading array data when device is in the autoselect mode, or if DQ5 goes high (while the device is providing status data).*
6. *The fourth cycle of the autoselect command sequence is a read operation.*
7. *The data is 00h for an unprotected sector and 01h for a protected sector. See "Autoselect Command Sequence" for more information.*

WRITE OPERATION STATUS

The device provides several bits to determine the status of a write operation: DQ3, DQ5, DQ6, and DQ7. Table 5 and the following subsections describe the functions of these bits. DQ7 and DQ6 each offer a method for determining whether a program or erase operation is complete or in progress. These three bits are discussed first.

DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Algorithm is in progress or completed. Data# Polling is valid after the rising edge of the final WE# pulse in the program or erase command sequence.

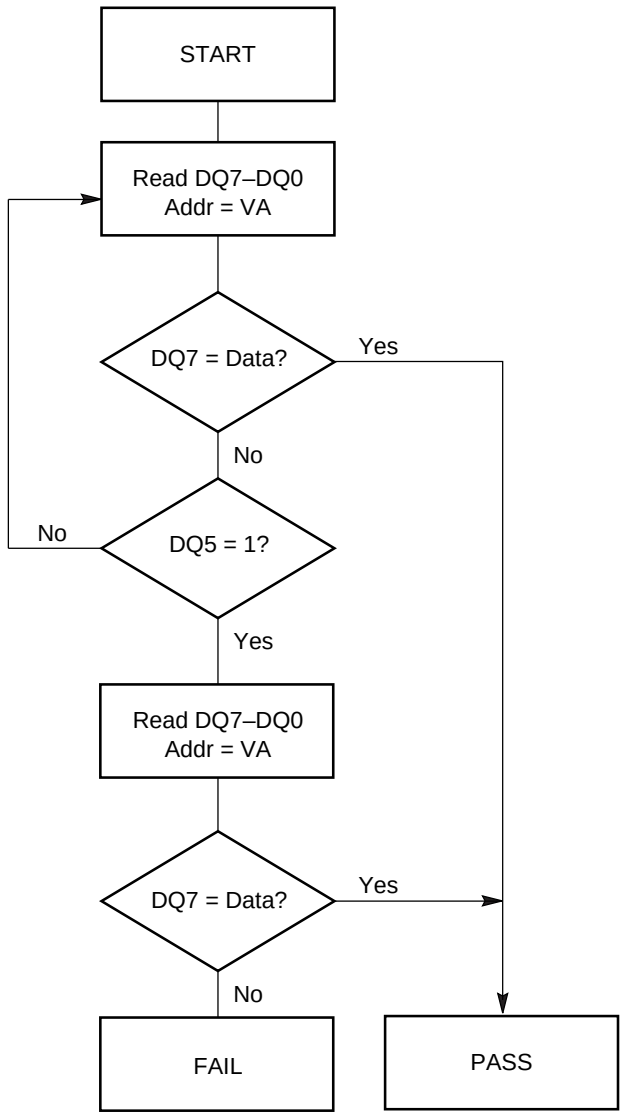
During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately 2 µs, then the device returns to reading array data.

During the Embedded Erase algorithm, Data# Polling produces a “0” on DQ7. When the Embedded Erase algorithm is complete, Data# Polling produces a “1” on DQ7. This is analogous to the complement/true datum output described for the Embedded Program algorithm: the erase function changes all the bits in a sector to “1”; prior to this, the device outputs the “complement,” or “0.” The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately 100 µs, then the device returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

When the system detects DQ7 has changed from the complement to true data, it can read valid data at DQ7–DQ0 on the *following* read cycles. This is because DQ7 may change asynchronously with DQ0–DQ6 while Output Enable (OE#) is asserted low. The Data# Polling Timings (During Embedded Algorithms) figure in the “AC Characteristics” section illustrates this.

Table 5 shows the outputs for Data# Polling on DQ7. Figure 3 shows the Data# Polling algorithm.



Notes:

1. *VA = Valid address for programming. During a sector erase operation, a valid address is an address within any sector selected for erasure. During chip erase, a valid address is any non-protected sector address.*
2. *DQ7 should be rechecked even if DQ5 = “1” because DQ7 may change simultaneously with DQ5.*

16736G-9

Figure 3. Data# Polling Algorithm

DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. (The system may use either OE# or CE# to control the read cycles.) When the operation is complete, DQ6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately 100 µs, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

If a program address falls within a protected sector, DQ6 toggles for approximately 2 µs after the program command sequence is written, then returns to reading array data.

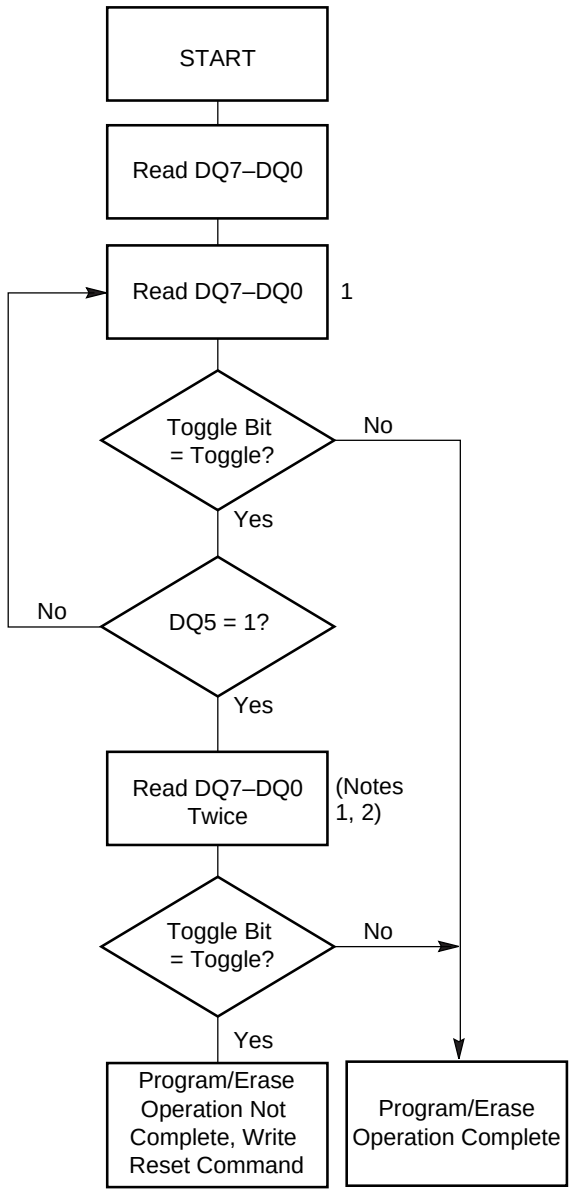
The Write Operation Status table shows the outputs for Toggle Bit I on DQ6. Refer to Figure 4 for the toggle bit algorithm, and to the Toggle Bit Timings figure in the "AC Characteristics" section for the timing diagram.

Reading Toggle Bit DQ6

Refer to Figure 4 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, a system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of Figure 4).



Notes:

1. *Read toggle bit twice to determine whether or not it is toggling. See text.*
2. *Recheck toggle bit because it may stop toggling as DQ5 changes to "1". See text.*

16736G-10

Figure 4. Toggle Bit Algorithm

DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a “1.” This is a failure condition that indicates the program or erase cycle was not successfully completed.

The DQ5 failure condition may appear if the system tries to program a “1” to a location that is previously programmed to “0.” **Only an erase operation can change a “0” back to a “1.”** Under this condition, the device halts the operation, and when the operation has exceeded the timing limits, DQ5 produces a “1.”

Under both these conditions, the system must issue the reset command to return the device to reading array data.

DQ3: Sector Erase Timer

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not an erase operation has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out is complete, DQ3 switches from “0” to “1.” The system may ignore DQ3 if the system can guarantee that the time between additional sector erase commands will always be less than 50 µs. See also the “Sector Erase Command Sequence” section.

After the sector erase command sequence is written, the system should read the status on DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure the device has accepted the command sequence, and then read DQ3. If DQ3 is “1”, the internally controlled erase cycle has begun; all further commands are ignored until the erase operation is complete. If DQ3 is “0”, the device will accept additional sector erase commands. To ensure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted. Table 5 shows the outputs for DQ3.

Table 5. Write Operation Status

Operation	DQ7 (Note 1)	DQ6	DQ5 (Note 2)	DQ3
Embedded Program Algorithm	DQ7#	Toggle	0	N/A
Embedded Erase Algorithm	0	Toggle	0	1

Notes:

1. *DQ7 requires a valid address when reading status information. Refer to the appropriate subsection for further details.*
2. *DQ5 switches to ‘1’ when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. See “DQ5: Exceeded Timing Limits” for more information.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Plastic Packages . . . . . –65°C to +125°C

Ambient Temperature
with Power Applied . . . . . –55°C to +125°C

Voltage with Respect to Ground
V_{CC} (Note 1). . . . . –2.0 V to +7.0 V

A9 (Note 2). . . . . –2.0 V to +12.5 V

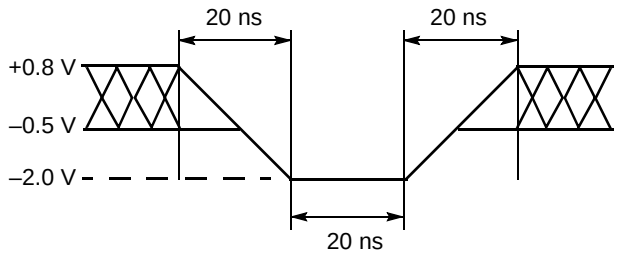
All other pins (Note 1) . . . . . –2.0 V to +7.0 V

Output Short Circuit Current (Note 3) . . . . . 200 mA

Notes:

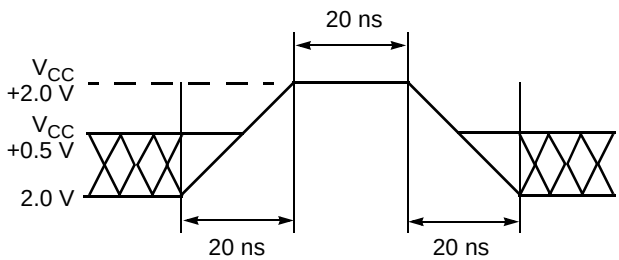
1. *Minimum DC voltage on input or I/O pin is –0.5 V. During voltage transitions, inputs may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 5. Maximum DC voltage on input and I/O pins is V_{CC} + 0.5 V. During voltage transitions, input and I/O pins may overshoot to V_{CC} + 2.0 V for periods up to 20 ns. See Figure 6.*
2. *Minimum DC input voltage on A9 pin is –0.5 V. During voltage transitions, A9 pins may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 5. Maximum DC input voltage on A9 is +12.5 V which may overshoot to 13.5 V for periods up to 20 ns.*
3. *No more than one output shorted at a time. Duration of the short circuit should not be greater than one second.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.



16736G-11

Figure 5. Maximum Negative Overshoot Waveform



16736G-12

Figure 6. Maximum Positive Overshoot Waveform

OPERATING RANGES

Commercial (C) Devices

Case Temperature (T_A) . . . . . 0°C to +70°C

Industrial (I) Devices

Case Temperature (T_A) . . . . . –40°C to +85°C

Extended (E) Devices

Case Temperature (T_A) . . . . . –55°C to +125°C

V_{CC} Supply Voltages

V_{CC} for ±5% devices . . . . . +4.75 V to +5.25 V

V_{CC} for ±10% devices . . . . . +4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS

TTL/NMOS Compatible

Parameter Symbol	Parameter Description	Test Description	Min	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max		±1.0	µA
I_{LIT}	A9 Input Load Current	$V_{CC} = V_{CC}$ Max, A9 = 12.5 V		50	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max		±1.0	µA
I_{CC1}	V_{CC} Active Current (Note 1)	CE# = V_{IL}, OE# = V_{IH}, $V_{CC} = V_{CC}$ Max		30	mA
I_{CC2}	V_{CC} Active Current (Notes 2, 3)	CE# = V_{IL}, OE# = V_{IH}, $V_{CC} = V_{CC}$ Max		50	mA
I_{CC3}	V_{CC} Standby Current	$V_{CC} = V_{CC}$ Max, CE# and OE# = V_{IH}		1.0	mA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V
V_{ID}	Voltage for Autoselect and Temporary Sector Unprotect	V_{CC} = 5.0 V	11.5	12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 12 mA, $V_{CC} = V_{CC}$ Min		0.45	V
V_{OH}	Output High Voltage	I_{OH} = –2.5 mA, $V_{CC} = V_{CC}$ Min	2.4		V
V_{LKO}	Low V_{CC} Lock-out Voltage		3.2	4.2	V

Notes:

1. *The I_{CC} current listed is typically less than 2 mA/MHz, with OE# at V_{IH}.*
2. *I_{CC} active while Embedded Program or Embedded Erase Algorithm is in progress.*
3. *Not 100% tested.*

DC CHARACTERISTICS (continued)

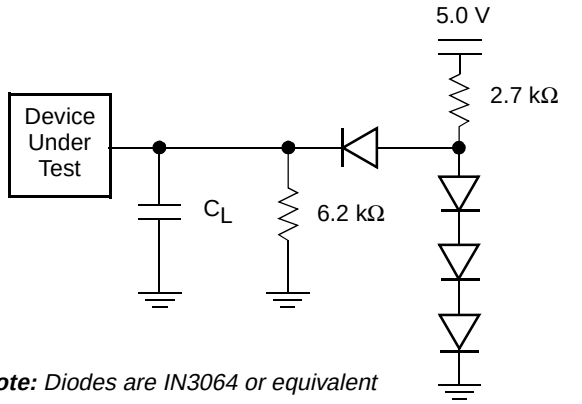
CMOS Compatible

Parameter Symbol	Parameter Description	Test Description	Min	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max		±1.0	µA
I_{LIT}	A9 Input Load Current	$V_{CC} = V_{CC}$ Max, A9 = 12.5 V		50	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max		±1.0	µA
I_{CC1}	V_{CC} Active Current (Note 1)	CE# = V_{IL}, OE# = V_{IH}, $V_{CC} = V_{CC}$ Max		30	mA
I_{CC2}	V_{CC} Active Current (Notes 2, 3)	CE# = V_{IL}, OE# = V_{IH}, $V_{CC} = V_{CC}$ Max		50	mA
I_{CC3}	V_{CC} Standby Current	$V_{CC} = V_{CC}$ Max, CE# = V_{CC} ± 0.5 V, OE# = V_{IH}		100	µA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		0.7 x V_{CC}	V_{CC} + 0.5	V
V_{ID}	Voltage for Autoselect and Temporary Sector Unprotect	V_{CC} = 5.0 V	11.5	12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 12 mA, $V_{CC} = V_{CC}$ Min		0.45	V
V_{OH1}	Output High Voltage	I_{OH} = –2.5 mA, $V_{CC} = V_{CC}$ Min	0.85 V_{CC}		V
V_{OH2}		I_{OH} = –100 µA, $V_{CC} = V_{CC}$ Min	V_{CC} –0.4		V
V_{LKO}	Low V_{CC} Lock-out Voltage		3.2	4.2	V

Notes:

1. *The I_{CC} current listed is typically less than 2 mA/MHz, with OE# at V_{IH}.*
2. *I_{CC} active while Embedded Program or Embedded Erase Algorithm is in progress.*
3. *Not 100% tested.*

TEST CONDITIONS



Note: *Diodes are IN3064 or equivalent*

16736G-13

Figure 7. Test Setup

Table 6. Test Specifications

Test Condition	-45	All others	Unit
Output Load	1 TTL gate		
Output Load Capacitance, C_L (including jig capacitance)	30	100	pF
Input Rise and Fall Times	5	20	ns
Input Pulse Levels	0.0–3.0	0.45–2.4	V
Input timing measurement reference levels	1.5	0.8	V
Output timing measurement reference levels	1.5	2.0	V

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High Z)

KS000010-PAL

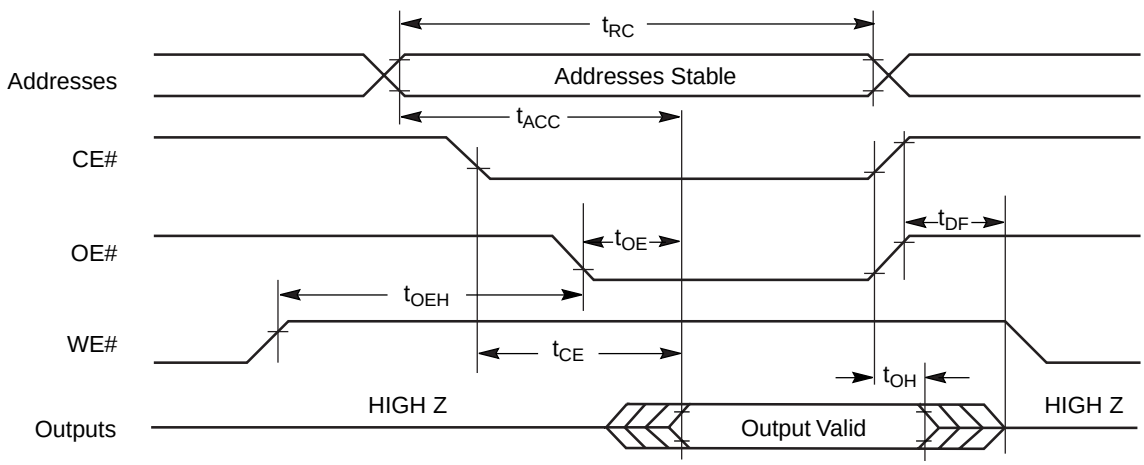
AC CHARACTERISTICS

Read-only Operations Characteristics

Parameter Symbol		Parameter Description	Test Setup		-45	-55	-70	-90	-120	Unit
JEDEC	Std.									
t_{AVAV}	t_{RC}	Read Cycle Time (Note 1)		Min	45	55	70	90	120	ns
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE}$ = V_{IL} $\overline{OE}$ = V_{IL}	Max	45	55	70	90	120	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE}$ = V_{IL}	Max	45	55	70	90	120	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay		Max	25	30	30	35	50	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (Notes 1, 2)		Max	10	15	20	20	30	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Notes 1, 2)		Max	10	15	20	20	30	ns
	t_{OEH}	Output Enable Hold Time (Note 1)	Read	Min	0					ns
			Toggle and Data Polling	Min	10					ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses $\overline{CE}$ or $\overline{OE}$, Whichever Occurs First		Min	0					ns

Notes:

1. *Not 100% tested.*
2. *Output Driver Disable Time.*
3. *See Figure 7 and Table 6 for test specifications.*



16736G-14

Figure 8. Read Operations Timings

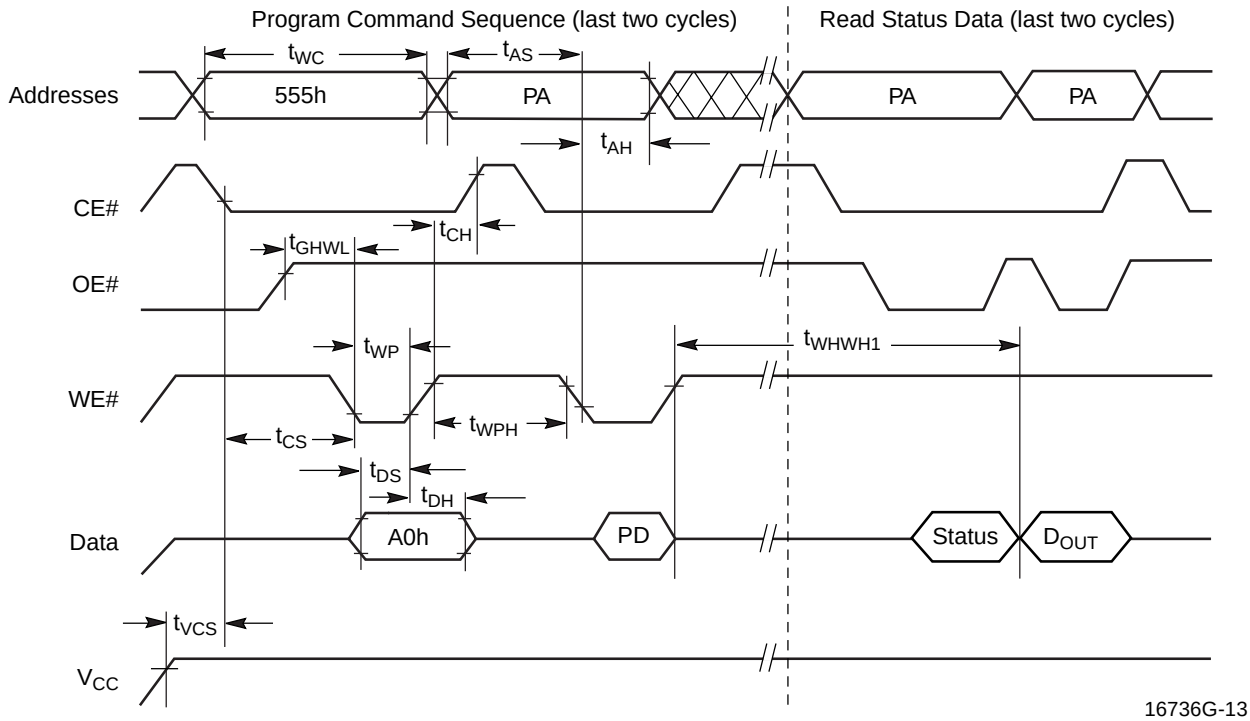
AC CHARACTERISTICS
Erase and Program Operations

Parameter Symbol		Parameter Description		-45	-55	-70	-90	-120	Unit
JEDEC	Standard								
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min	45	55	70	90	120	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	0					ns
t_{WLAX}	t_{AH}	Address Hold Time	Min	35	45	45	45	50	ns
t_{DVWH}	t_{DS}	Data Setup Time	Min	20	20	30	45	50	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min	0					ns
t_{GHWL}	t_{GHWL}	Read Recover Time Before Write (OE# High to WE# Low)	Min	0					ns
t_{ELWL}	t_{CS}	CE# Setup Time	Min	0					ns
t_{WHEH}	t_{CH}	CE# Hold Time	Min	0					ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min	25	30	35	45	50	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High	Min	20					ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation (Note 2)	Typ	14					µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)	Typ	1.0					sec
	t_{VCS}	V_{CC} Set Up Time (Note 1)	Min	50					µs

Notes:

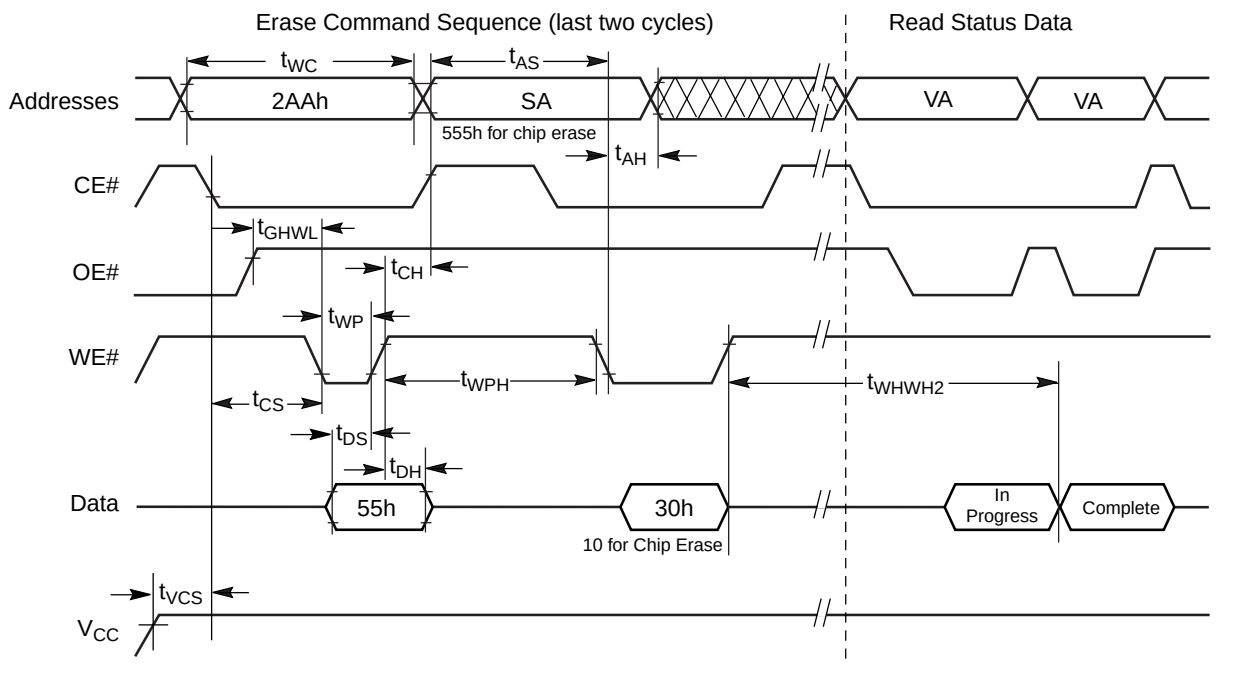
1. *Not 100% tested.*
2. *See the "Erase and Programming Performance" section for more informaiton.*

AC CHARACTERISTICS



Note: *PA = program address, PD = program data, D_{OUT} is the true data at the program address.*

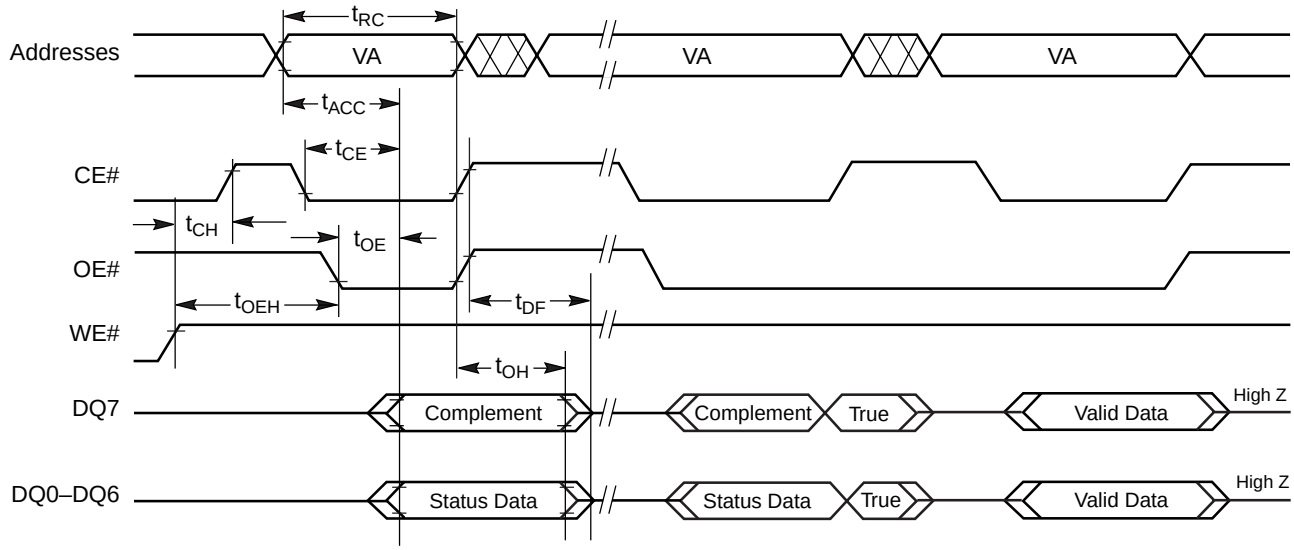
Figure 9. Program Operation Timings



Note: *SA = sector address (for Sector Erase), VA = Valid Address for reading status data (see "Write Operation Status").*

Figure 10. Chip/Sector Erase Operation Timings

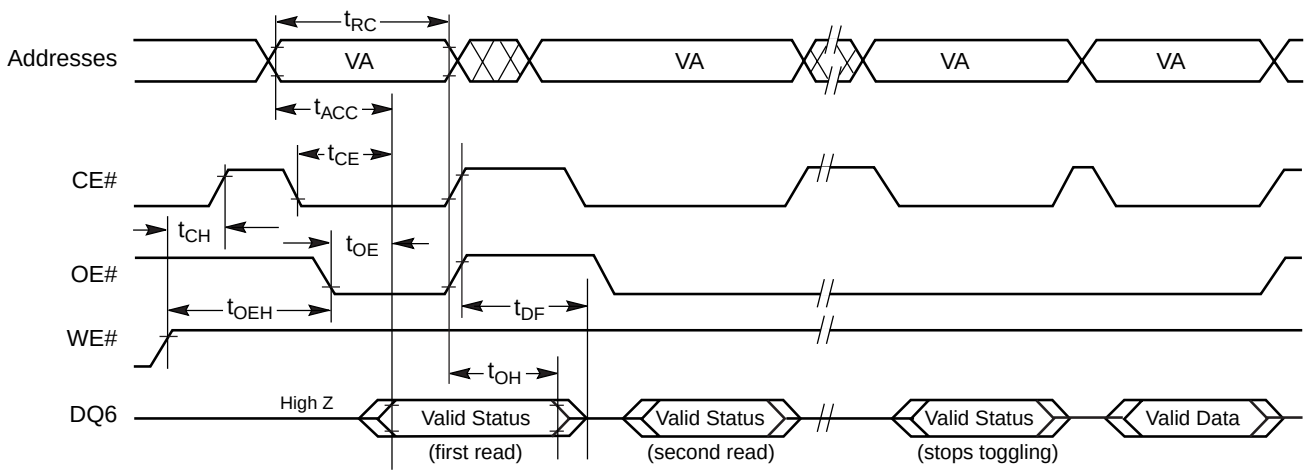
AC CHARACTERISTICS



Note: *VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.*

16736G-15

Figure 11. Data# Polling Timings (During Embedded Algorithms)



Note: *VA = Valid address; not required for DQ6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle.*

16736G-16

Figure 12. Toggle Bit Timings (During Embedded Algorithms)

AC CHARACTERISTICS

Erase and Program Operations

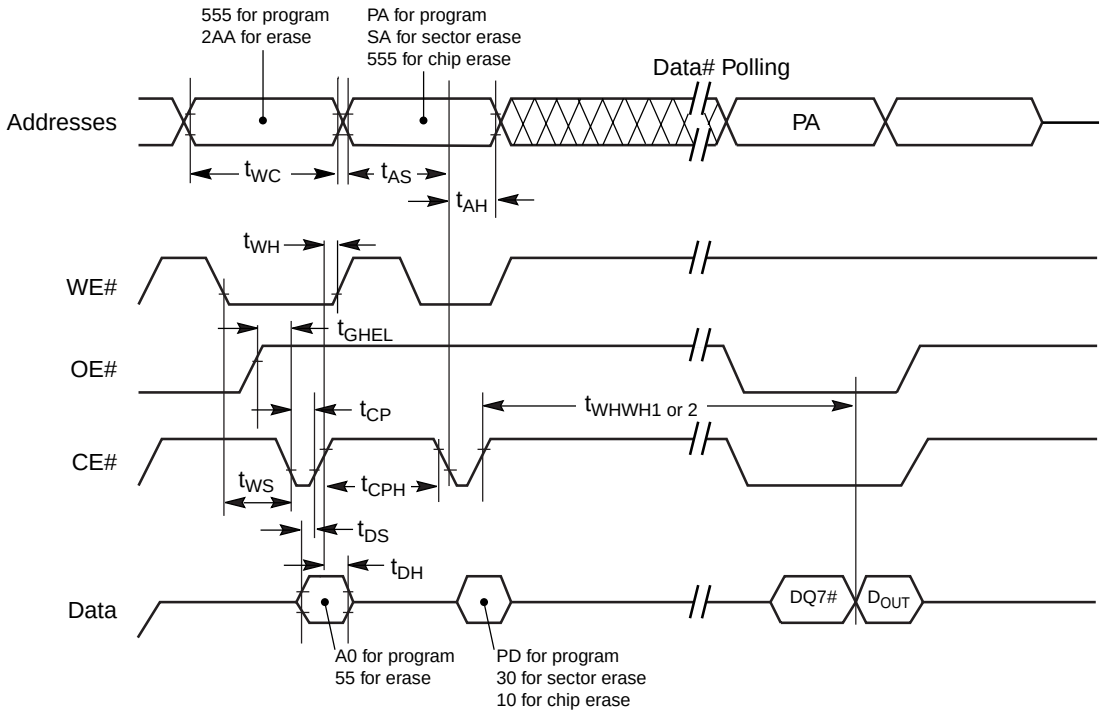
Alternate CE# Controlled Writes

Parameter Symbol		Parameter Description		-45	-55	-70	-90	-120	Unit
JEDEC	Standard								
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min	45	55	70	90	120	ns
t_{AVEL}	t_{AS}	Address Setup Time	Min	0					ns
t_{ELAX}	t_{AH}	Address Hold Time	Min	35	45	45	45	50	ns
t_{DVEH}	t_{DS}	Data Setup Time	Min	20	20	30	45	50	ns
t_{EHDX}	t_{DH}	Data Hold Time	Min	0					ns
	t_{OES}	Output Enable Setup Time (Note 1)	Min	0					ns
t_{GHEL}	t_{GHEL}	Read Recover Time Before Write	Min	0					ns
t_{WLEL}	t_{WS}	WE# Setup Time	Min	0					ns
t_{EHWH}	t_{WH}	WE# Hold Time	Min	0					ns
t_{ELEH}	t_{CP}	CE# Pulse Width	Min	25	30	35	45	50	ns
t_{EHEL}	t_{CPH}	CE# Pulse Width High	Min	20					ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation (Note 2)	Typ	14					µs
t_{WHWH2}	t_{WHWH2}	Chip/Sector Erase Operation (Note 2)	Typ	1.0					sec

Notes:

1. *Not 100% tested.*
2. *See the "Erase and Programming Performance" section for more information.*

AC CHARACTERISTICS



Notes:

1. *PA = Program Address, PD = Program Data, SA = Sector Address, DQ7# = Complement of Data Input, D_{OUT} = Array Data.*
2. *Figure indicates the last two bus cycles of the command sequence.*

16736G-17

Figure 13. Alternate CE# Controlled Write Operation Timings

ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits			Comments
	Typ (Note 1)	Max (Note 2)	Unit	
Chip/Sector Erase Time	1.0	15	sec	Excludes 00h programming prior to erasure (Note 4)
Byte Programming Time	14	1000	µs	Excludes system-level overhead (Note 5)
Chip Programming Time (Note 3)	1.8	12.5	sec	

Notes:

1. *Typical program and erase times assume the following conditions: 25°C, 5.0 V V_{CC}, 100,000 cycles. Additionally, programming typicals assume checkerboard pattern.*
2. *Under worst case conditions of 90°C, V_{CC} = 4.5 V (4.75 V for -45, -55 PDIP), 100,000 cycles.*
3. *The typical chip programming time is considerably less than the maximum chip programming time listed, since most bytes program faster than the maximum byte program time listed. If the maximum byte program time given is exceeded, only then does the device set DQ5 = 1. See the section on DQ5 for further information.*
4. *In the pre-programming step of the Embedded Erase algorithm, all bytes are programmed to 00h before erasure.*
5. *System-level overhead is the time required to execute the four-bus-cycle command sequence for programming. See Table 1 for further information on command definitions.*
6. *The device has a typical erase and program cycle endurance of 1,000,000 cycles. 100,000 cycles are guaranteed.*

LATCHUP CHARACTERISTIC

Parameter Description	Min	Max
Input Voltage with respect to V_{SS} on I/O pins	–1.0 V	V_{CC} + 1.0 V
V_{CC} Current	–100 mA	+100 mA

Note: *Includes all pins except V_{CC}. Test conditions: V_{CC} = 5.0 Volt, one pin at a time.*

TSOP PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	6	7.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8.5	12	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	8	10	pF

Notes:

1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25°C, f = 1.0 MHz.*

PLCC AND PDIP PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8	12	pF
C_{IN2}	Control Pin Capacitance	V_{PP} = 0	8	12	pF

Notes:

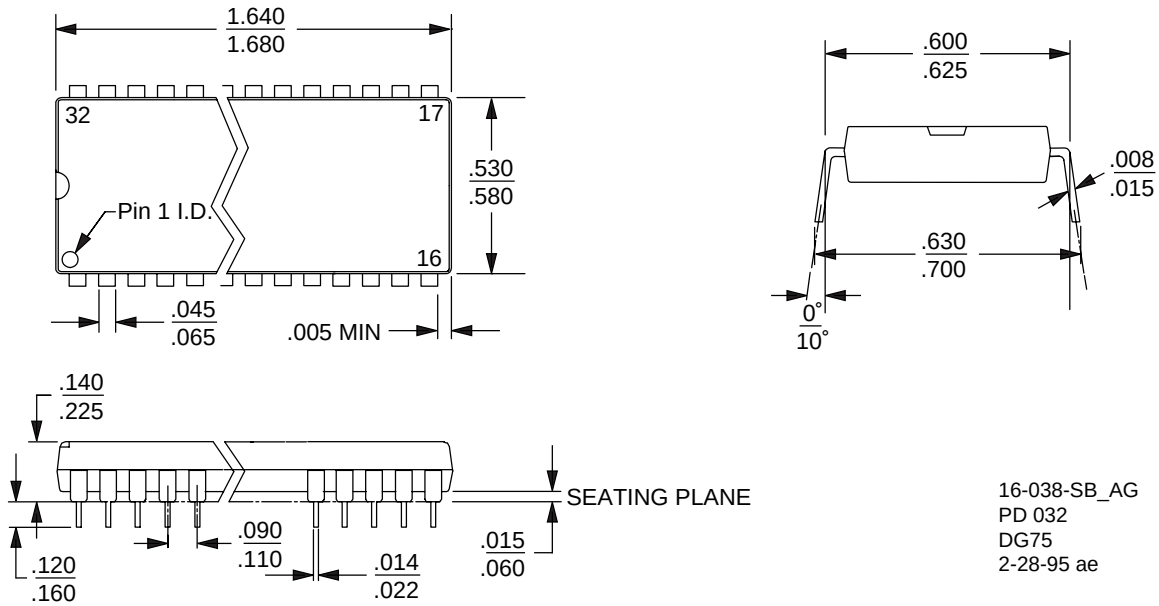
1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25°C, f = 1.0 MHz.*

DATA RETENTION

Parameter Description	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

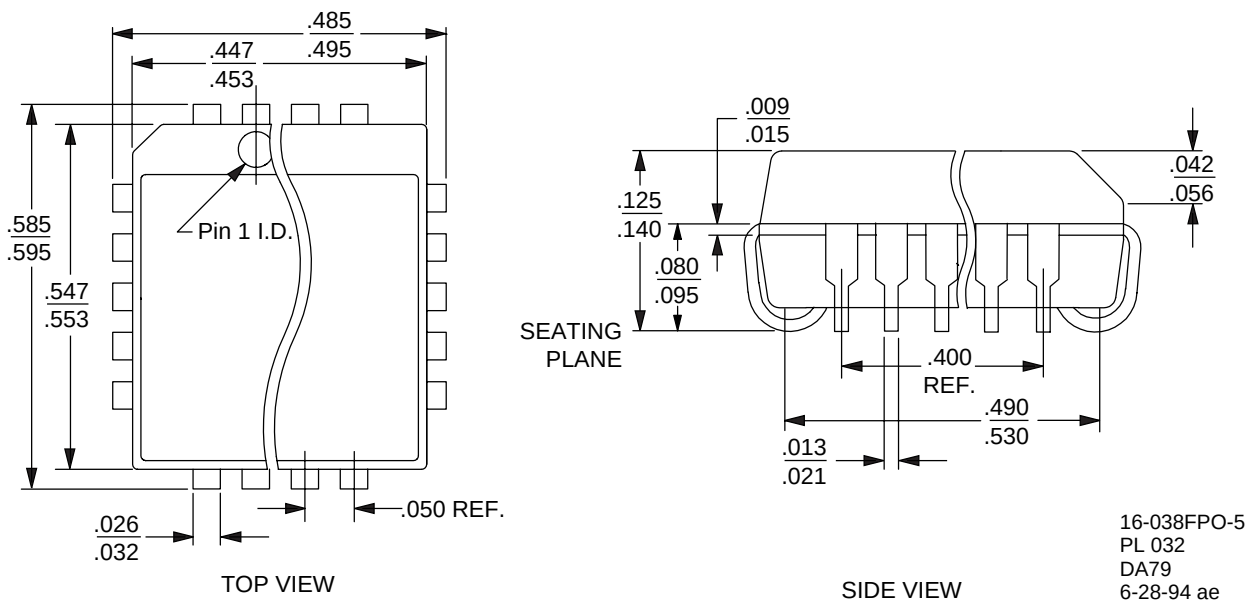
PHYSICAL DIMENSIONS

PD 032
32-Pin Plastic DIP (measured in inches)



16-038-SB_AG
PD 032
DG75
2-28-95 ae

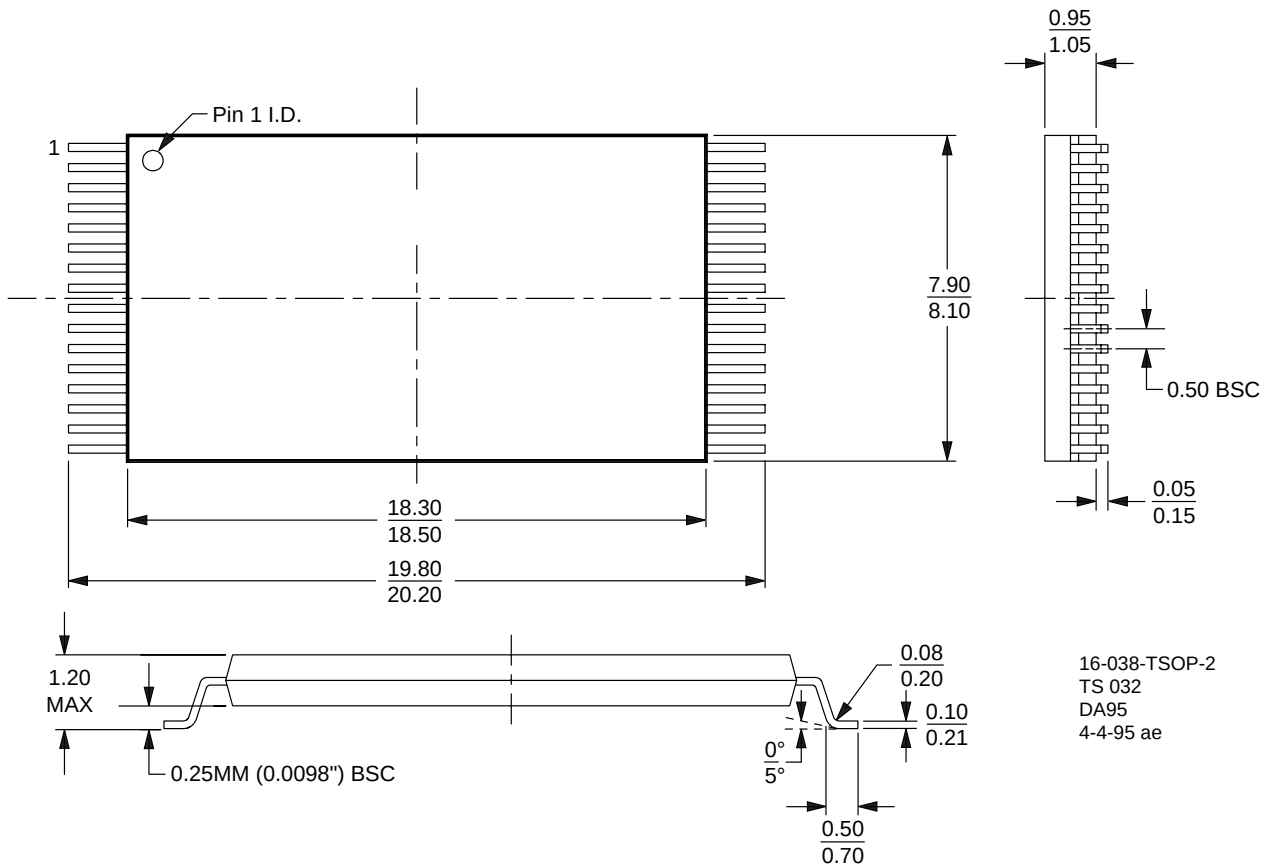
PL 032
32-Pin Plastic Leaded Chip Carrier (measured in inches)



16-038FPO-5
PL 032
DA79
6-28-94 ae

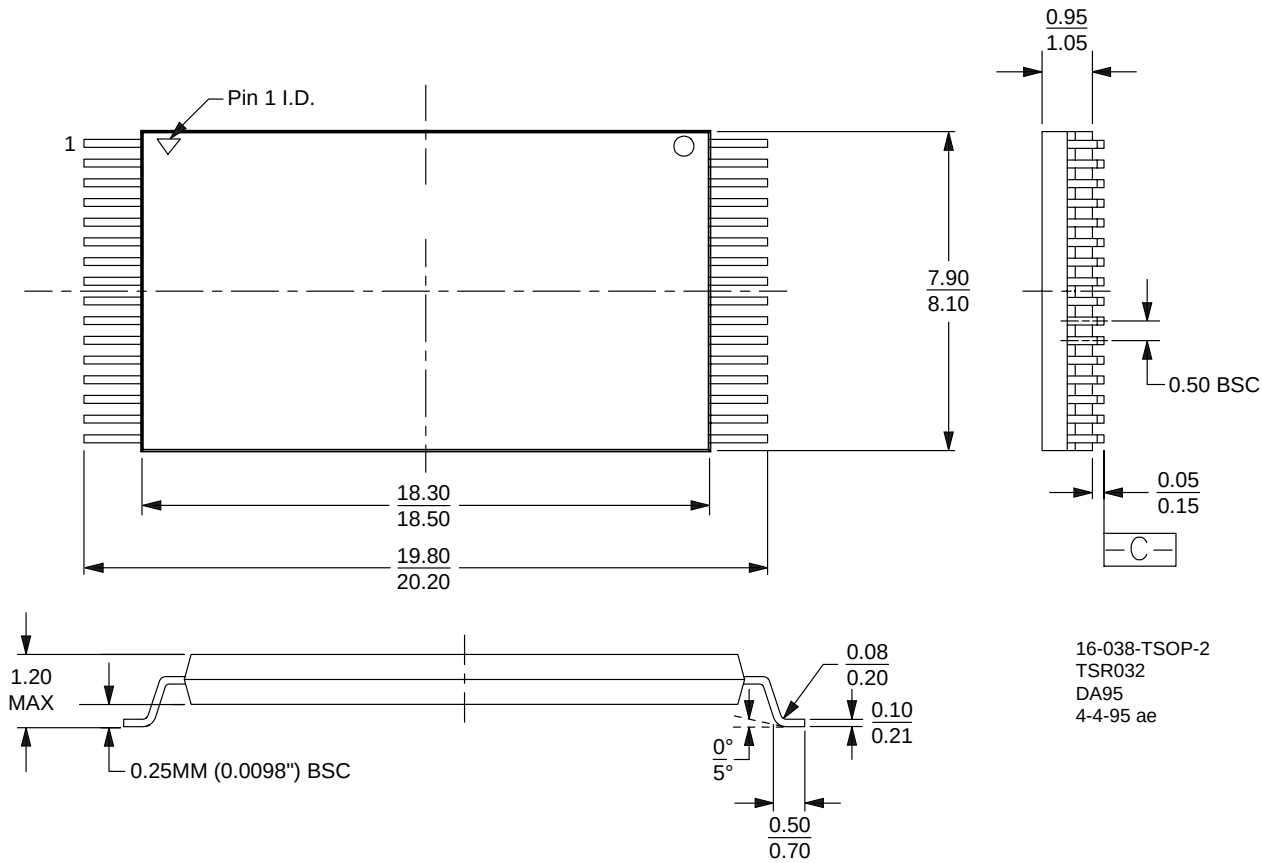
PHYSICAL DIMENSIONS (continued)

TS 032
32-Pin Standard Thin Small Outline Package (measured in millimeters)



PHYSICAL DIMENSIONS (continued)

TSR 032
32-Pin Standard Thin Small Outline Package (measured in millimeters)



REVISION SUMMARY FOR AM29F010

Revision F+1

Product Selector Guide

There are now two V_{CC} supply operating ranges available for the 55 ns speed option. The PDIP package is only available in the ±5% V_{CC} operating range. The other packages are available in the ±10% operating range.

Ordering Information

The 45 ns speed grade is now also available in PC configuration (PDIP package, commercial temperature.)

Operating Ranges

V_{CC} Supply Voltages: Changed to reflect the available speed options.

AC Characteristics

Write/Erase/Program Operations: Corrected to indicate t_{VLHT}, t_{OESP}, t_{WHWH1}, and t_{WHWH2} are typical values, not minimum values. Changed value for t_{WHWH2}.

AC Characteristics

Write/Erase/Program Operations, Alternate CE# *Controlled Writes:* Corrected to indicate t_{WHWH1} and t_{WHWH2} are typical values, not minimum values. Changed value for t_{WHWH2}.

Erase and Programming Performance

Combined chip and sector erase specifications; changed typical and maximum values. Added Note 6.

Revision G

Global

Made formatting and layout consistent with other data sheets. Used updated common tables and diagrams.

Revision G+1

Table 4, Command Definitions

Address bits A0–A14 are required for unlock cycles. Therefore, addresses for second and fifth write cycles are 2AAAh. Addresses for first, third, fourth, and sixth cycles are 5555h. Read cycles are not affected. Deleted Note 4 to reflect the correction.

Revision G+2

AC Characteristics

Erase/Program Operations; Erase and Program Operations Alternate CE# Controlled Writes: Corrected the notes reference for t_{WHWH1} and t_{WHWH2}. These parameters are 100% tested. Corrected the note reference for t_{VCS}. This parameter is not 100% tested.