■ BCM5208

10/100BASE-TX/FX Quad-Φ™ Transceiver

GENERAL DESCRIPTION

The BCM5208 is a single-chip Quad 10/100BASE-TX/FX transceiver targeted at Fast Ethernet switches and segmentable repeaters. The device contains four full-duplex 10BASE-T/100BASE-TX/100BASE-FX Fast Ethernet transceivers, each of which performs all of the physical layer interface functions for 10BASE-T Ethernet on CAT 3, 4 or 5 unshielded twisted pair (UTP) cable and 100BASE-TX Fast Ethernet on CAT 5 UTP cable. 100BASE-FX is supported at each port through the use of external fiber-optic transmit and receive devices.

The BCM5208 is a highly integrated solution combining digital adaptive equalizers, ADCs, phase locked loops, line drivers, encoders, decoders and all the required support circuitry into a single monolithic CMOS chip. It complies fully with the IEEE 802.3u specification, including the Media Independent Interface (MII) and Auto-Negotiation subsections, providing compatibility with all industry standard Fast Ethernet Media Access Controller (MAC) and repeater devices.

The effective use of digital technology in the BCM5208 design results in robust performance over a broad range of operating scenarios. Problems inherent to mixed-signal implementations, such as analog offset and on-chip noise, are eliminated by employing field proven digital adaptive equalization and digital clock recovery techniques.

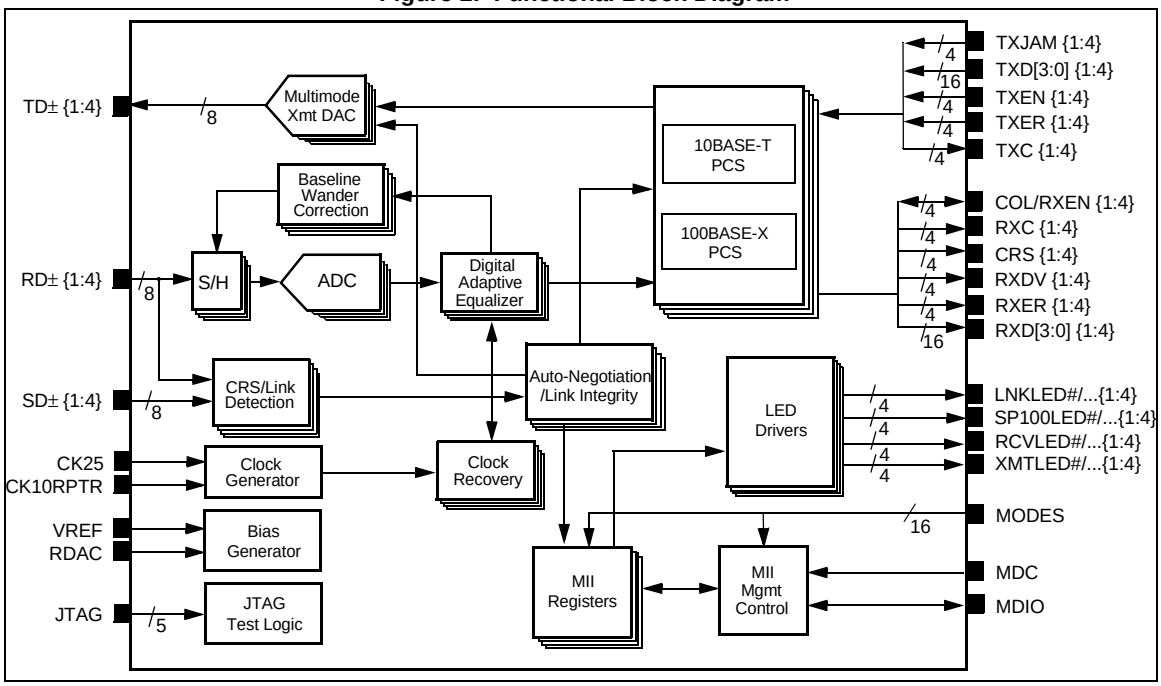
FEATURES

- 10BASE-T/100BASE-TX/FX IEEE 802.3u Compliant
- Single-chip Quad Physical Interface - MII to Magnetics
- Media Independent Interface (MII) for each Port
- Fully Integrated Digital Adaptive Equalizers
- 125 MHz Clock Generator and Timing Recovery
- On-chip Multimode Transmit Waveshaping
- Edge-Rate Control eliminates External Filters
- Integrated Baseline Wander Correction
- MII Repeater Mode support in all Modes
- 10 Mbps Serial Repeater Mode
- Port Switching for Multi-Segment Repeaters
- Full-duplex Support
- IEEE 802.3u-Compliant Auto-Negotiation
- Carrier Integrity Monitor on each Port
- Shared MII Management Interface up to 12.5 Mbps
- Multiple Programmable Serial or Parallel LED Modes
- Interrupt Output Capability
- Loopback Mode for Diagnostics
- IEEE 1149.1 (JTAG) and NAND-Chain ICT support
- Low-Power Single-Supply 3.3 Volt CMOS Technology
- Compatible with 3.3 Volt and 5.0 Volt I/O
- 208-Pin PQFP

APPLICATIONS

- Switches
- Segmentable Single/Dual-Speed Repeaters
- Multi-Port Adapter Cards

Figure 1: Functional Block Diagram



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REVISION HISTORY

REVISION #	*DATE*	*CHANGE DESCRIPTION*
SP1.8	July 13, 1998	Preliminary Release
SP2.0	March 5, 1999	Final Release: 1. Page 9, Table 4, VREF default condition changed. 2. Pages 10 and 12, pin 44 description changed from DVDD to DLLTEST. 3. Page 16, Table 6 and page 24, Table 14 updated bit 8, register 10h definition. Changed from “Preliminary” to “Final” (the qualifier “Preliminary” is removed).
5208-DS03-R	November 3, 1999	1. Page 15, added “Note that at least one or more clocked idle states...” and “A final 65th clock pulse...” to the Idle frame format for the MII Management Interface. 2. Pages 16 and 17, changed PHYID Low Init from “6135h” to “6136h” and Auxiliary Control/Status bit 8 from “TXDAC” to “Rsvd.” for Table 6. 3. Page 23, added “This bit is cleared when...” to Page Received bit description. 4. Page 47, deleted “RD +/- {1:4}, and changed MIN from “700” to “100” for V_{IDIFF} in Table 42.

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SECTION 1: FUNCTIONAL DESCRIPTION

OVERVIEW

The BCM5208 is a single-chip device containing four independent Fast Ethernet transceivers. Each performs all the physical layer interface functions for 100BASE-TX full-duplex or half-duplex Ethernet on CAT 5 twisted pair cable and 10BASE-T full- or half-duplex Ethernet on CAT 3, 4 or 5 cable. Each port may also be configured for 100BASE-FX full or half-duplex transmission over fiber-optic cabling when paired with an external fiber-optic transmitter and receiver.

The chip performs 4B5B, MLT3, NRZI, and Manchester encoding and decoding, clock and data recovery, stream cipher scrambling/descrambling, digital adaptive equalization, line transmission, carrier sense and link integrity monitor, Auto-Negotiation, and MII management functions. The BCM5208 may be connected to a MAC or repeater controller through the MII on one side, and connects directly to the network media on the other side through isolation transformers for UTP modes or fiber-optic transmitter/receiver components for FX modes. In repeater mode, the MII ports may be bussed with other BCM5208 devices. Port multiplexing logic also allows the BCM5208 to be optimized for multi-segment and dual-speed repeater configurations. The BCM5208 is fully compliant with the IEEE 802.3 and 802.3u standards.

ENCODER / DECODER

In 100BASE-TX and 100BASE-FX modes, the BCM5208 transmits and receives a continuous data stream on twisted pair or fiber-optic cable. When the MII transmit enable is asserted, nibble-wide (4-bit) data from the transmit data pins is encoded into 5-bit code-groups and inserted into the transmit data stream. The 4B5B encoding is shown in Table 1 on page 3. The transmit packet is encapsulated by replacing the first two nibbles of preamble with a start of stream delimiter (J/K codes) and appending an end of stream delimiter (T/R codes) to the end of the packet. When the MII transmit error input is asserted during a packet, the transmit error code group (H) is sent in place of the corresponding data code group. The transmitter will repeatedly send the idle code group between packets.

In TX mode, the encoded data stream is scrambled by a stream cipher block and then serialized and encoded into MLT3 signal levels. A multimode transmit DAC is used to drive the MLT3 data onto the twisted pair cable. In FX mode, the scrambling function is bypassed and the data is NRZI encoded. The multimode transmit DAC drives differential positive ECL (PECL) levels to an external fiber-optic transmitter.

Following baseline wander correction, adaptive equalization, and clock recovery in TX mode, the receive data stream is converted from MLT3 to serial NRZ data. The NRZ data is descrambled by the stream cipher block and then deserialized and aligned into 5-bit code groups.

In FX mode, the receive data stream differential PECL levels are sampled from the fiber-optic receiver. Baseline wander correction, adaptive equalization, and stream cipher descrambling functions are bypassed and NRZI decoding is used instead of MLT3.

The 5-bit code groups are decoded into 4-bit data nibbles, as shown in Table 1. The start of stream delimiter is replaced with preamble nibbles and the end of stream delimiter and idle codes are replaced with all zeros. The decoded data is driven onto the MII receive data pins. When an invalid code group is detected in the data stream, the BCM5208 will assert the MII RXER signal. The chip will also assert RXER for several other error conditions which improperly terminate the data stream. While RXER is asserted, the receive data pins will be driven with a 4-bit code indicating the type of error detected. The error codes are listed in Table 2 on page 4.

In 10BASE-T mode, Manchester encoding and decoding is performed on the data stream. The multimode transmit DAC performs pre-equalization for 100 meters of CAT 3 cable.

LINK MONITOR

In 100BASE-TX mode, receive signal energy is detected by monitoring the receive pair for transitions in the signal level. Signal levels are qualified using squelch detect circuits. When no signal or certain invalid signals are detected on the receive pair, the link monitor will enter and remain in the “Link Fail” state where only idle codes will be transmitted. When a valid signal is detected on the receive pair for a minimum period of time, the link monitor will enter the “Link Pass” state and the transmit and receive functions will be enabled.

In 100BASE-FX mode, the external fiber-optic receiver performs the signal energy detection function and communicates this information directly to the BCM5208 through the differential SD +/- pins.

In 10BASE-T mode, a link-pulse detection circuit constantly monitors the RD+/- pins for the presence of valid link pulses.

CARRIER SENSE

In 100BASE-X modes, carrier sense is asserted asynchronously on the CRS pin as soon as activity is detected in the receive data stream. RXDV is asserted as soon as a valid start-of-stream delimiter (SSD) is detected. Carrier sense and RXDV are deasserted synchronously upon detection of a valid end of stream delimiter or two consecutive idle code groups in the receive data stream. If carrier sense is asserted and a valid SSD is not detected immediately, then RXER will be asserted in place of RXDV. A value of Eh (E hex) will be driven on the receive data pins to indicate false carrier sense.

In 10BASE-T mode, carrier sense is asserted asynchronously on the CRS pin when valid preamble activity is detected on the RD+/- input pins.

In half-duplex DTE mode, the BCM5208 will additionally assert carrier sense while transmit enable is asserted and the link monitor is in the “Pass” state. In repeater or full-duplex mode, CRS is only asserted for receive activity.

COLLISION DETECTION

In half-duplex mode, collision detect is asserted on the COL pin whenever carrier sense is asserted while transmission is in progress. Collision detect is never asserted in full-duplex mode.

CARRIER INTEGRITY MONITOR

In 100BASE-X repeater applications, it is necessary to protect the repeater core from spurious carrier events generated by the transceiver. The BCM5208 implements the carrier integrity monitor (CIM) on each port as specified in the IEEE 802.3 standard. When the transceiver detects excessive false carrier events, it will enter the “Disconnect” state, and transmission and reception will be disabled. The CIM function may be enabled or disabled at reset by a mode select pin, and may be enabled or disabled following reset through the MII management interface. The CIM function is not enabled in 100BASE-X DTE or any 10BASE-T mode.

AUTO-NEGOTIATION

The BCM5208 contains the ability to negotiate its mode of operation over the twisted pair link using the Auto-Negotiation mechanism defined in the IEEE 802.3u specification. Auto-Negotiation may be enabled or disabled by hardware or software control. When the Auto-Negotiation function is enabled, the BCM5208 will automatically choose its mode of operation by advertising its abilities and comparing them with those received from its link partner. The BCM5208 can be configured to advertise 100BASE-TX full-duplex and/or half-duplex and 10BASE-T full and/or half-duplex. Each transceiver will negotiate independently with its link partner, and choose the highest level of operation available for its own link. Auto-Negotiation must be disabled during 100BASE-FX operation and will not advertise full-duplex abilities when the device is configured in repeater mode.

DIGITAL ADAPTIVE EQUALIZER

The digital adaptive equalizer removes interzonal interference created by the transmission channel media. The equalizer accepts sampled unequalized data from the ADC on each channel and produces equalized data. The BCM5208 achieves an optimum signal to noise ratio by using a combination of feed forward equalization and decision feedback equalization. This powerful technique achieves a 100BASE-TX BER of less than 1×10^{-12} for transmission up to 100 meters on CAT 5 twisted pair cable, even in harsh noise environments. The digital adaptive equalizers in the BCM5208 achieve performance close to theoretical limits. The all-digital nature of the design makes the performance very tolerant to on-chip noise. The filter coefficients are self adapting to any quality of cable or cable length. Due to transmit pre-equalization in 10BASE-T mode and complete lack of ISI in 100BASE-FX mode, the adaptive equalizer is bypassed in these two modes of operation.

ADC

Each receive channel has its own 6-bit 125 MHz analog to digital converter (ADC). The ADC samples the incoming data on the receive channel and produces a 6-bit output. The output of the ADC is fed to the digital adaptive equalizer. Advanced analog circuit techniques achieve low offset, high power supply noise rejection, fast settling time, and low bit error rate.

DIGITAL CLOCK RECOVERY/GENERATOR

The all-digital clock recovery and generator block creates all internal transmit and receive clocks. The transmit clocks are locked to the 25 MHz clock input while the receive clocks are locked to the incoming data streams. Clock recovery circuits optimized to MLT3, NRZI, and Manchester encoding schemes are included for use with each of the three different operating modes. The input data streams are sampled by the recovered clock from each port and fed synchronously to the respective digital adaptive equalizer.

BASELINE WANDER CORRECTION

A 100BASE-TX data stream is not always DC balanced. Because the receive signal must pass through a transformer, the DC offset of the differential receive input can wander. This effect, known as baseline wander, can greatly reduce the noise immunity of the receiver. The BCM5208 automatically compensates for baseline wander by removing the DC offset from the input signal, and thereby significantly reduces the chance of a receive symbol error. The baseline wander correction circuit is not required, and therefore bypassed, in 10BASE-T and 100BASE-FX operating modes.

Table 1: 4B5B Encoding

NAME	*4B CODE*	*5B CODE*	*MEANING*
0	0000	11110	Data 0
1	0001	01001	Data 1
2	0010	10100	Data 2
3	0011	10101	Data 3
4	0100	01010	Data 4
5	0101	01011	Data 5
6	0110	01110	Data 6
7	0111	01111	Data 7
8	1000	10010	Data 8
9	1001	10011	Data 9
A	1010	10110	Data A
B	1011	10111	Data B
C	1100	11010	Data C
D	1101	11011	Data D
E	1110	11100	Data E
F	1111	11101	Data F
I	0000*	11111	Idle
J	0101*	11000	Start-of-Stream Delimiter, Part 1
K	0101*	10001	Start-of-Stream Delimiter, Part 2
T	0000*	01101	End-of-Stream Delimiter, Part 1
R	0000*	00111	End-of-Stream Delimiter, Part 2
H	1000	00100	Transmit Error (used to force signalling errors)

Table 1: 4B5B Encoding(Continued)

V	0111	00000	Invalid Code
V	0111	00001	Invalid Code
V	0111	00010	Invalid Code
V	0111	00011	Invalid Code
V	0111	00101	Invalid Code
V	0111	00110	Invalid Code
V	0111	01000	Invalid Code
V	0111	01100	Invalid Code
V	0111	10000	Invalid Code
V	0111	11001	Invalid Code
* Treated as invalid code (mapped to 0111) when received in data field.			

Table 2: Receive Error Encoding

ERROR TYPE	***RXD[3:0]***
Stream cipher error - descrambler lost lock	0010
Link failure	0011
Premature end of stream	0110
Invalid code	0111
Transmit error	1000
False carrier sense	1110

MULTIMODE TRANSMIT DAC

The multimode transmit digital to analog converter (DAC) transmits MLT3-coded symbols in 100BASE-TX mode, NRZI-coded symbols in 100BASE-FX mode, and Manchester-coded symbols in 10BASE-T mode. It performs programmable edge-rate control in TX mode, which decreases unwanted high frequency signal components thus reducing EMI. High-frequency pre-emphasis is performed in 10BASE-T mode; no filtering is performed in 100BASE-FX mode. The transmit DAC utilizes a current drive output which is well balanced and produces very low noise transmit signals. PECL voltage levels are produced with resistive terminations in 100BASE-FX mode.

STREAM CIPHER

In 100BASE-TX mode, the transmit data stream is scrambled in order to reduce radiated emissions on the twisted pair cable. The data is scrambled by *exclusive ORing* the NRZ signal with the output of an 11-bit wide linear feedback shift register (LFSR), which produces a 2047-bit non-repeating sequence. The scrambler reduces peak emissions by randomly spreading the signal energy over the transmit frequency range, and eliminating peaks at certain frequencies. For repeater applications, where all ports transmit the same data simultaneously, signal energy is spread further by using unique seeds to generate a different non-repeating sequence for each of the four ports.

The receiver descrambles the incoming data stream by *exclusive ORing* it with the same sequence generated at the transmitter. The descrambler detects the state of the transmit LFSR by looking for a sequence representing consecutive idle codes. The descrambler will “lock” to the scrambler state after detecting a sufficient number of consecutive idle code-groups. The receiver will not attempt to decode the data stream unless the descrambler is locked. Once locked, the descrambler will continuously monitor the data stream to make sure that it has not lost synchronization. The receive data stream is expected to contain inter-packet idle periods. If the descrambler does not detect enough idle codes within 724µs, it will become “unlocked”, and the receive decoder will be disabled. The descrambler will always be forced into the “unlocked” state when a link failure condition is detected.

Stream cipher scrambling/descrambling is not used in 100BASE-FX and 10BASE-T modes.

FAR-END FAULT

Auto-Negotiation provides a Remote Fault capability for detection of asymmetric link failures. Since Auto-Negotiation is not available for 100BASE-FX, the BCM5208 implements the IEEE 802.3 standard Far-End Fault mechanism for the indication and detection of remote error conditions. If the Far-End Fault mechanism is enabled, a transceiver will transmit the Far-End Fault Indication whenever a receive channel failure is detected (signal detect is deasserted). Each transceiver will also continuously monitor the receive channel when a valid signal is present (signal detect asserted). When its link partner is indicating a remote error, the transceiver will force its link monitor into the link fail state and set the Remote Fault bit in the MII status register. The Far-End Fault mechanism is on by default in 100BASE-FX mode and off by default in 100BASE-TX and 10BASE-T modes, and may be controlled by software after reset.

MII MANAGEMENT

Each transceiver within the BCM5208 contains an independent set of MII management registers. They share a single MDC/MDIO serial interface, Each transceiver has a unique address and must be accessed individually. The common base address for the group of four individual transceivers is defined by configuring the three external PHYAD address input pins.

10 MBIT SERIAL REPEATER MODE

When the 10 Mbit Serial Repeater Mode is enabled by setting SER10 high, the signal CK10RPTR is used to clock in TXD and TXEN. Data is delivered on pin RXD(0) and taken from TXD(0). Pins RXD(3:1) and TXD(3:1) are not used.

SEGMENTATION MODE

Segmentation allows the connection of any port to any MII bus. Each transceiver has a segmentation control (Register 1Dh, bits 14 and 15) which may be used to map it to any of the four MII busses. Segmentation, which is available only in repeater mode, is enabled by setting bit 12 of Register 1Dh.

After segmentation is enabled, the PHY Enable bit, Register 1Dh, bit 13, must also be enabled to actually establish the connection between the transceiver and the MII bus.

If LINK is lost and re-established at a speed different from the last speed, the PHY enable bit will automatically de-assert in order to isolate the transceiver from the previously selected segment. The repeater controller must subsequently determine which MII bus to attach the transceiver to before re-asserting the PHY enable bit.

INTERRUPT MODE

The BCM5208 can be programmed to provide an interrupt output from each of the four transceivers. The interrupt feature is disabled by default. When the interrupt capability is enabled by setting MII register 1Ah, bit 14, the XMTLED# pin becomes the INTR# pin and the RCVLED# pin becomes an “activity” pin named ACTLED#. The INTR# pins are open-drain and may be wire-ORed together. The status of each interrupt source is also reflected in Register 1Ah, bits 1, 2 and 3. The sources of interrupt are change in link, speed or full-duplex status. If any type of interrupt occurs, the Interrupt Status bit, Register 1Ah, bit “0”, will be set.

In addition, each transceiver has its own register controlling the interrupt function.

If the interrupt enable bit is set to “0”, no status bits will be set and no interrupts will be generated. If the interrupt enable bit is set to “1”, the following conditions apply:

1. If mask status bits are to “0” and the interrupt mask is set to “1”, status bits will be set but no interrupts generated.
2. If mask status bits are set to “0” and the interrupt mask is set to “0”, status bits and interrupts will be available.
3. If mask status bits are set to “1” and the interrupt mask is set to “0”, no status bits and no interrupts will be available.

Changes from “active” to “inactive” or vice versa will cause an interrupt. Setting Register 1Ah, bit 8 high will mask all interrupts, regardless of the settings of the individual mask bits.

SERIAL LED MODES

The BCM5208 supports several modes for providing LED and interrupt information as a serial bit stream. The LED data is presented on a single pin with a second pin providing a shift clock and a third providing framing. When the Serial LED mode is enabled, pin 182 becomes the bit clock output, pin 183 becomes the data output and pin 184 provides the framing pulse.

After the Serial LED mode is enabled, several options for bit format become available. If no action is taken, bits will be shifted out as shown in the top line of the table below. If the INTR bit (bit 14 of MII Register 1Ah) is set, data will be shifted out as shown in the Interrupt row of the table. If the FDXLED bit (bit 15 of MII Register 1Ah) is set, data will be shifted out as shown in the Full-Duplex row of the table.

In each mode, 24 bits comprise a frame. Bits are shifted in the order shown in the table below, with those bits in the column marked BIT 0 leaving the chip first and those in the column marked BIT 5 leaving the chip later in time. The sequence will repeat 4 times between frame pulses to provide data for each PHY in the quad device. Bits are numbered from 0 to 5; frames are numbered from 1 to 4. Therefore, bit 0 of PHY 1 is the first bit out of the frame, and bit 5 of PHY 4 is the 24th. bit out of the frame.

Table 3: Serial LED Mode Bit Framing

OPTION	*MII REG 1AH*	*BIT 5*	*BIT 4*	*BIT 3*	*BIT 2*	*BIT 1*	*BIT 0*
Normal	Bit 14 =0 Bit 15 =0	FDX	1	Speed	Link	Transmit	Receive
Interrupt	Bit 14 =1 Bit 15 =0	FDX	Global Interrupt	Speed	Link	Slice Interrupt	Activity
Full-Duplex	Bit 14 =0 Bit 15 =1	FDX	1	Speed	Link	FDX	Activity
A Global Interrupt indicates an interrupt from any of the 4 slices ORed together; a Slice Interrupt is from one of the 4 PHYs.							

Data is shifted out on the falling edge of the shift clock which is approximately 1 MHz. Data will be valid on the rising edge of the shift clock. The framing pulse is high during the bit 0 time of frame1. For timing information, see Table 37 and Figure 11.

SECTION 2: HARDWARE SIGNAL DEFINITION TABLE

Table 4 provides the pin descriptions for the BCM5208.

Table 4: Pin Descriptions

PIN	PIN LABEL	TYPE	DESCRIPTION
MEDIA CONNECTIONS			
60, 75, 82, 97	RD+ {1:4}	I_A	**Receive Pair.** Differential data from the media is received on the RD± signal pair.
61, 74, 83, 96	RD– {1:4}		
65, 70, 87, 92	TD+ {1:4}	O_A	**Transmit Pair.** Differential data is transmitted to the media on the TD± signal pair.
66, 69, 88, 91	TD– {1:4}		
48,46,108, 110	SD+ {1:4}	I	**100BASE-FX Signal Detect.** Indicates signal quality status on the fiber-optic link in 100BASE-FX mode. When the signal quality is good, the SD+ pin should be driven high relative to the SD– pin. 100BASE-FX mode is disabled when both pins are simultaneously pulled low.
49, 47, 109, 111	SD– {1:4}		
CLOCK			
6	CK25	I	**25 MHz Reference Clock Input.** This pin must be driven with a continuous 25 MHz clock in all operating modes. In 100BASE-X repeater modes, this signal may be used as the transmit clock input when the BCM5208 is receiving instead of sourcing the transmit clock.
114	CK10RPTR	I_{PD}	**10BASE-T Repeater Clock Input.** This pin must be driven with a continuous clock only if one or more transceivers are to operate in 10BASE-T repeater mode. It must be sourced with a 2.5 MHz clock for 10BASE-T MII repeater mode and with a 10 MHz clock for 10BASE-T serial repeater mode.
MII INTERFACE			
27 12 145 130	TXC {1}/CLK2.5 TXC {2}/CLK10 TXC {3}/CLK20 TXC {4}/CLK40	O_{3S}	**Transmit Clock.** When in DTE mode, delivers a 25 MHz output in 100BASE-X mode and 2.5 MHz in 10BASE-T mode. When in Repeater Mode (RPTR pin 41 High), the TXC pins output fixed frequency clocks during and after Reset. These clocks are continuously driven, free-running outputs, generated from CK25 at frequencies of 2.5, 10, 20 and 40 MHz.
33, 34, 35, 36	TXD[3:0] {1}	I_{PD}	**Transmit Data Input.** Nibble-wide transmit data is input on these pins synchronously to TXC. TXD[3] is the most significant bit.
208, 1, 9, 10	TXD[3:0] {2}		
150, 149, 148, 147	TXD[3:0] {3}		
124, 123, 122, 121	TXD[3:0] {4}		
37,11,146, 120	TXEN {1:4}	I_{PD}	**Transmit Enable.** Active high. Indicates that the data nibble is valid on TXD[3:0].

Note: # = active low, I = digital input, O = digital output, I/O = bidirectional, I_A = analog input, O_A = analog output, I_{PU} = digital input w/ internal pull-up, I_{PD} = digital input w/ internal pull-down, O_{OD} = open-drain output, O_{3S} = three-state output, I/O_{PD} = bidirectional w/ internal pull-down, B = Bias. Bus Naming Convention: pin label followed by [MSB:LSB] followed by {Port #}.

Table 4: Pin Descriptions(Continued)

PIN	*PIN LABEL*	*TYPE*	*DESCRIPTION*
32, 207, 156, 125	TXER {1:4}	I_{PD}	**Transmit Error.** Active high. Asserting TXER when TXEN is asserted causes transmission of 100BASE-X's designated "bad code" in lieu of normal 4B5B encoded data on the wires. No action is taken in 10BASE-T mode if TXER is asserted. If not used, may be left open or pulled to ground.
17, 190, 172, 140	RXC {1:4}	O_{3S}	**Receive Clock.** 25 MHz output in 100BASE-X mode and 2.5 MHz output in 10BASE-T mode. This clock is recovered from the incoming data on the cable inputs. Becomes 10 MHz when RPTR=SER10=1. In DTE applications, RXC is a continuously running output clock resynchronized at the start of each incoming packet. This synchronization may result in an elongated period during one cycle when RXDV is low.
19, 20, 21, 23	RXD[3:0] {1}	O_{3S}	**Receive Data Outputs.** Nibble-wide receive data is driven out these pins synchronously to RXC. RXD[3] is the most significant bit.
192, 193, 194, 195	RXD[3:0] {2}		
170, 169 168, 167	RXD[3:0] {3}		
138, 137 136, 134	RXD[3:0] {4}		
24,196, 166, 133	RXDV {1:4}	O_{3S}	**Receive Data Valid.** Active high. Indicates that a receive frame is in progress, and that the data stream present on the RXD output pins is valid.
18, 191, 171, 139	RXER {1:4}	O_{3S}	**Receive Error Detected.** Active high. Indicates that there has been an error during a receive frame.
26, 206, 157, 131	CRS {1:4}	O_{3S}	**Carrier Sense.** Active high. Indicates traffic on link. In 100BASE-X modes, CRS is asserted when a non-idle condition is detected in the receive data stream and deasserted when idle or a valid end of stream delimiter is detected. In 10BASE-T mode, CRS is asserted when a valid preamble is detected and deasserted when end-of-file or an idle condition is detected. In DTE mode, CRS is also asserted during transmission of packets. CRS is an asynchronous output signal.
25, 205, 151, 132	COL/RXEN {1:4}	I/O_{PD}	**Collision Detect.** In half-duplex DTE modes, active high output indicates that a collision has occurred. In full-duplex mode, COL remains low. COL is an asynchronous output signal. **Receive Enable.** In Repeater mode, RXEN is an active high input. Enables BCM5208 to drive MII bus. MII outputs are forced high-Z when RXEN is low.
118	MDIO	I/O_{PD}	**Management Data I/O.** This serial input/output bit is used to read from and write to the MII registers. The data value on the MDIO pin is valid and latched on the rising edge of MDC.
117	MDC	I_{PD}	**Management Data Clock.** The MDC clock input must be provided to allow MII management functions. Clock frequencies up to 12.5 MHz are supported.
119	RESET#	I_{PU}	**Reset.** Active Low. Resets the BCM5208. Pin not included in NAND chain.
MODE			
38, 39, 40	PHYAD [4:2]	I_{PD}	**PHY Address Selects.** These inputs set the three MSB's for the MII management PHY addresses. The two LSB's, PHYAD [1:0], are internally wired to each of the four ports: PHYAD [00] = Port 1,..., PHYAD [11] = Port 4. Also serve as test control inputs along with TESTEN and NANDMD[1:0] to select the NAND-chain test mode.

Note: # = active low, I = digital input, O = digital output, I/O = bidirectional, I_A = analog input, O_A = analog output, I_{PU} = digital input w/ internal pull-up, I_{PD} = digital input w/ internal pull-down, O_{OD} = open-drain output, O_{3S} = three-state output, I/O_{PD} = bidirectional w/ internal pull-down, B = Bias. Bus Naming Convention: pin label followed by [MSB:LSB] followed by {Port #}.

Table 4: Pin Descriptions(Continued)

PIN	*PIN LABEL*	*TYPE*	*DESCRIPTION*
41	RPTR	I_{PD}	**Repeater Mode Select.** Active high input places all four PHY's into repeater mode; selects DTE mode when low.
52	SER10	I_{PD}	**Serial 10BASE-T Repeater Mode.** For any PHY operating at 10 Mbps in repeater mode (RPTR = 1), selects serial repeater mode when high, selects MII repeater mode when low. ORed with Register 1E(hex) bit 1.
42	FDXEN/CIMEN	I_{PD}	**Full-Duplex Mode Enable.** This pin's function applies only to DTE mode when Auto-Negotiation is disabled. The FDXEN pin is logically OR'ed with the MII Control register bit 8 to generate an internal full-duplex enable signal. When Auto-Negotiation is enabled, the FDXEN is ignored. **Carrier Integrity Monitor Enable.** In repeater mode, CIMEN enables the CIM function. When low, the CIM function will be disabled. In either case, the CIM function may be enabled or disabled under software control (Register 10h, bit 12).
104	F100	I_{PU}	**Force 100BASE-X Operation.** When F100 is high and ANEN is low, all transceivers will be forced to 100BASE-X operation. When F100 is low and ANEN is low, all transceivers are forced to 10BASE-T operation. When ANEN is high, F100 has no effect on operation.
105	ANEN	I_{PU}	**Auto-Negotiation Enable.** When pulled high, Auto-Negotiation begins immediately after reset. When low, Auto-Negotiation is disabled after reset. Auto-Negotiation is always under software control (Register "0", bit 12).
58, 57, 56, 55	TXJAM {1:4}	I_{PD}	**Transmit JAM.** Active high; valid during repeater mode only. When asserted during transmission (TXEN active), forces PHY to ignore transmit data inputs (TXD[3:0]) and transmit a jam pattern instead. Equivalent data value of jam pattern is 5h.
116, 115	ER[1:0]	I_{PU}	**Transmit DAC Edge Rate Control.** These pins control the slew rate of each of the transmit DACs. The 10-90% rise time is set by the value on ER[1:0] as follows: "00" = 1 ns; "01" = 2 ns; "10" = 3 ns; "11" = 4 ns.
43	TESTEN	I_{PD}	**Test Enable.** Active-high test control input used along with NANDMD[1:0] and PHYA[4:2] to select the NAND-chain test mode. This test mode is latched when TESTEN is pulsed high then low, with PHYA[4:2]=101 and NANDMD[1:0] = 11. This pin is not included in the NAND chain and must be pulled low or left unconnected during normal operation.
54, 53	NANDMD[1:0]	I_{PD}	**NAND Mode.** Active-high test control inputs used along with TESTEN and PHYA[4:2] to select the NAND-chain test mode. Both inputs must be driven high during latching of the test-mode. Must be pulled low or left unconnected during normal operation.
BIAS			
78	RDAC	B	**DAC Bias Resistor.** Adjusts the current level of each of the transmit DACs. A resistor of 1.24 KΩ ±1% must be connected between the RDAC pin and AGND.
79	VREF	B	**Voltage Reference.** Low-impedance bias pin driven by the internal band-gap voltage reference. This pin must be left unconnected during normal operation.
LED			
203, 184, 178, 159	LNKLED# {1:4} Ser SFRM# {2}	O	**Link Integrity LED.** Active low. This output signal indicates the link status of the PHY. LNKLED is driven low when the link to the PHY is good. In repeater mode, this pin may be connected directly to the repeater controller. When the Serial LED mode is enabled, pin 184 becomes the Serial LED mode frame signal.

Note: # = active low, I = digital input, O = digital output, I/O = bidirectional, I_A = analog input, O_A = analog output, I_{PU} = digital input w/ internal pull-up, I_{PD} = digital input w/ internal pull-down, O_{OD} = open-drain output, O_{3S} = three-state output, I/O_{PD} = bidirectional w/ internal pull-down, B = Bias. Bus Naming Convention: pin label followed by [MSB:LSB] followed by {Port #}.

Table 4: Pin Descriptions(Continued)

PIN	*PIN LABEL*	*TYPE*	*DESCRIPTION*
204, 185, 177, 158	SP100LED# {1:4}	O	**Speed 100 LED.** Driven low when operating in 100BASE-X modes and high when operating in 10BASE-T modes.
202, 183, 179, 160	XMTLED# {1:4} INTR# {1:4} FDXLED# {1:4} Ser SDO# {2}	O_{OD}	**Transmit Activity LED.** Active low output. The transmit activity LED is driven low for approximately 80ms each time there is transmit activity while in the link pass state. When INTR mode is enabled, the pin becomes an interrupt output. When FDX LED mode is enabled, the pin becomes FDXLED output. When the Serial LED mode is enabled, pin 183 becomes the Serial LED mode data output signal.
201, 182, 180, 161	RCVLED# {1:4} ACTLED# {1:4} Ser SCLK# {2}	O_{OD}	**Receive Activity LED.** Active low output. The receive activity LED is driven low for approximately 80ms each time there is receive activity while in the link pass state. When in either INTR or FDXLED modes, this pin becomes ACTLED output for either receive or transmit activity. When the Serial LED mode is enabled, pin 182 becomes the Serial LED mode clock signal.
JTAG			
99	TDI	I_{PU}	**Test Data Input.** Serial data input to the JTAG TAP Controller. Sampled on the rising edge of TCK. If unused, may be left unconnected.
100	TDO	O_{3S}	**Test Data Output.** Serial data output from the JTAG TAP Controller. Updated on the falling edge of TCK. Actively driven both high and low when enabled; high impedance otherwise.
101	TMS	I_{PU}	**Test Mode Select.** Single control input to the JTAG TAP Controller used to traverse the test-logic state machine. Sampled on the rising edge of TCK. If unused, may be left unconnected.
102	TCK	I_{PU}	**Test Clock.** Clock input used to synchronize JTAG control and data transfers. If unused, may be left unconnected.
103	TRST#	I_{PU}	**Test Reset.** Asynchronous active-low reset input to the JTAG TAP Controller. Must be held low during power-up to insure the TAP Controller initializes to the test-logic-reset state. May be pulled low continuously when JTAG functions are not used.
44	DLLTEST	I_{PU}	**DLT Bypass Test Enable.** This pin is for factory test only, and must be connected to DVDD or left floating.
POWER			
181	IVDD		**Input VDD.** +5.0 V or +3.3V. If any of the inputs are driven to 5.0V, this pin must be connected to the 5.0V supply. If none of the inputs are driven above 3.3V, this pin may be connected to the 3.3V supply.
7	PLLVDD		**Phase Locked Loop VDD**
8	PLLGND		**Phase Locked Loop GND**
77	BIASVDD		**Bias VDD**
80	BIASGND		**Bias GND**
59, 63, 72, 76, 81, 85, 94, 98	AVDD		**Analog VDD**

Note: # = active low, I = digital input, O = digital output, I/O = bidirectional, I_A = analog input, O_A = analog output, I_{PU} = digital input w/ internal pull-up, I_{PD} = digital input w/ internal pull-down, O_{OD} = open-drain output, O_{3S} = three-state output, I/O_{PD} = bidirectional w/ internal pull-down, B = Bias. Bus Naming Convention: pin label followed by [MSB:LSB] followed by {Port #}.

Table 4: Pin Descriptions(Continued)

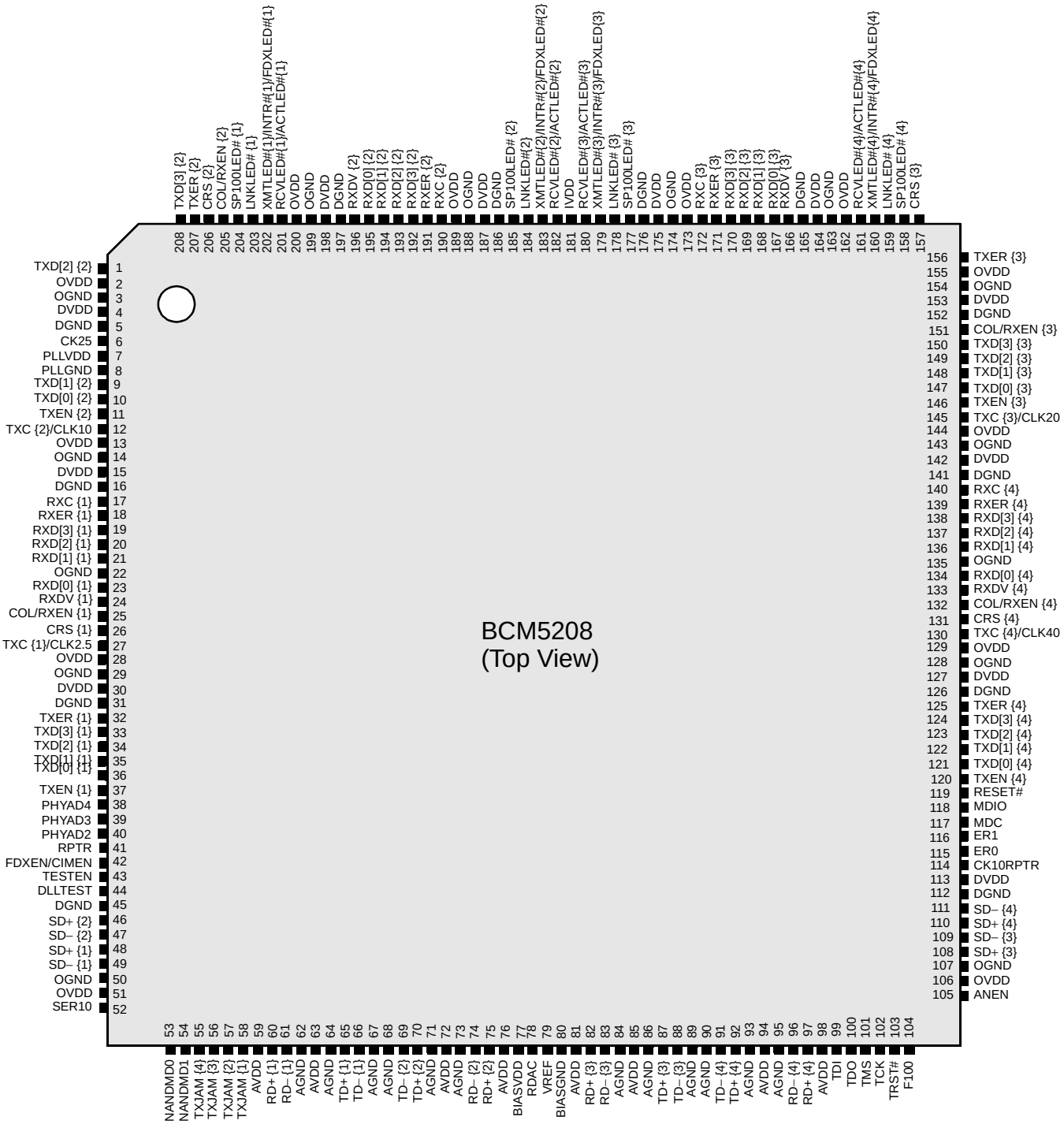
PIN	*PIN LABEL*	*TYPE*	*DESCRIPTION*
62, 64, 67, 68, 71, 73, 84, 86, 89, 90, 93, 95	AGND		**Analog GND**
4, 15, 30, 113, 127, 142, 153, 164, 175, 187, 198	DVDD		**Digital Core VDD**
5, 16, 31, 45, 112, 126, 141, 152, 165, 176, 186, 197	DGND		**Digital Core GND**
2, 13, 28, 51, 106, 129, 144, 155, 162, 173, 189, 200	OVDD		**Digital Periphery (Output Buffer) VDD**
3, 14, 22, 29, 50, 107, 128, 135, 143, 154, 163, 174, 188, 199	OGND		**Digital Periphery (Output Buffer) GND**

Note: # = active low, I = digital input, O = digital output, I/O = bidirectional, I_A = analog input, O_A = analog output, I_{PU} = digital input w/ internal pull-up, I_{PD} = digital input w/ internal pull-down, O_{OD} = open-drain output, O_{3S} = three-state output, I/O_{PD} = bidirectional w/ internal pull-down, B = Bias. Bus Naming Convention: pin label followed by [MSB:LSB] followed by {Port #}.

SECTION 3: PINOUT DIAGRAM

Figure 2 provides the pinout diagram for the BCM5208.

Figure 2: Pinout Diagram



SECTION 4: OPERATIONAL DESCRIPTION

RESETTING THE BCM5208

There are two ways to reset each transceiver in the BCM5208. A hardware reset pin has been provided which resets all internal nodes inside the chip to a known state. The reset pulse must be asserted for at least 400 ns. Hardware reset should always be applied to a BCM5208 after power-up.

Each transceiver in the BCM5208 also has an individual software reset capability. To perform software reset, a “1” must be written to bit 15 of the transceiver’s MII Control Register (see MII Register Definitions). This bit is self-clearing, meaning that a second write operation is not necessary to end the reset. There is no effect if a “0” is written to the MII Control Register reset bit.

ISOLATE MODE

Each transceiver in the BCM5208 may be isolated from the MII. When a transceiver is put into isolate mode, all MII inputs (TXD[3:0], TXEN, and TXER) are ignored, and all MII outputs (TXC, COL, CRS, RXC, RXDV, RXER, and RXD[3:0]) are set at high impedance. Only the MII management pins (MDC, MDIO) operate normally. Upon resetting the chip, the isolate mode is off. Writing a “1” to bit 10 of the MII Control Register puts the transceiver into isolate mode. Writing a “0” to the same bit removes it from isolate mode.

LOOPBACK MODE

The loopback mode allows in-circuit testing of the BCM5208 chip. All packets sent in through the TXD pins are looped-back internally to the RXD pins, and are not sent out to the cable. Incoming packets on the cable are ignored. Because of this, the COL pin will normally not be activated during loopback mode. In order to test that the COL pin is actually working, the BCM5208 may be placed into collision test mode. This mode is enabled by writing a “1” to bit 7 of the MII Control Register. Asserting TXEN will cause the COL output to go high, and deasserting TXEN will cause the COL output to go low.

The loopback mode may be entered by writing a “1” to bit 14 of the MII Control Register. In order to resume normal operation, bit 14 of the MII Control Register must be “0”.

Several function bypass modes are also supported which can provide a number of different combinations of feedback paths during loopback testing. These bypass modes include: bypass scrambler, bypass MLT3 encoder and bypass 4B5B encoder.

FULL-DUPLEX MODE

The BCM5208 supports full-duplex operation. While in full-duplex mode, a transceiver may simultaneously transmit and receive packets on the cable. The COL signal is never activated while in full-duplex mode. By default, each transceiver in the BCM5208 powers up in half-duplex mode.

When Auto-Negotiation is disabled, full-duplex operation can be enabled either by a pin (FDXEN) or by an MII register bit (Register “0”’ bit 8).

When Auto-Negotiation is enabled in DTE mode, full-duplex capability is advertised by default but can be overridden by a write to the Auto-Negotiation Advertisement Register (04h). In repeater mode full-duplex capability can never be advertised.

REPEATER MODE

The BCM5208 will operate in repeater mode when the repeater mode select pin is pulled high. In repeater mode, carrier sense will not be asserted for transmit events. Full-duplex mode will be disabled. The collision outputs are replaced by MII port enable inputs (RXEN {1:4}), allowing the MII ports from multiple BCM5208’s to be bussed. When RXEN is low, RXD[3:0], RXDV, RXER and RXC outputs will be tri-stated. CRS is always driven.

MULTI-SEGMENT REPEATERS

The BCM5208 supports multi-segment repeaters by allowing each transceiver to connect to any of the MII interfaces. Interface selection is programmed through the Auxiliary Mode register (1Dh). When multiple transceivers are connected to the same MII interface, the BCM5208 will multiplex the active port onto the MII bus. RXD[3:0], RXDV, RXER, RXC, TXD[3:0], and TXER are multiplexed; CRS, TXEN, TXJAM, and RXEN are dedicated per port, and are not affected by port multiplexing. Only one RXEN may be active at a time for PHY's that are connected to the same MII interface. Each MII interface will drive out when any transceiver connected to it is enabled (RXEN asserted). An MII interface will be disabled when none of the receive enables for ports connected to it are active.

If the RPTR pin = "1" at reset, all transceivers are isolated by default, until enabled and segmented to an MII interface by writing to the Aux Mode register. If the RPTR pin ="0" at reset, all transceivers are active by default and each is segmented to it's own MII interface.

After operation is established at a certain speed, any loss of link followed by a new link at a different speed results in the transceiver being isolated from its MII interface until it is re-segmented by an MII write to the Aux Mode register.

100BASE-FX MODE

Any of the BCM5208 transceivers may interface with an external 100BASE-FX fiber-optic driver and receiver instead of the magnetics module used with twisted-pair cable. The differential transmit and receive data pairs will operate at PECL voltage levels instead of those required for twisted-pair transmission. The data will be encoded using two-level NRZI instead of three-level MLT3. The data stream is not scrambled for fiber-optic transmission. The stream cipher function is bypassed when 100BASE-FX mode is selected.

The external fiber-optic receiver will detect signal status and communicate it to the BCM5208 through the SD± pins. In this mode, the internal signal detect function is bypassed. The 100BASE-FX mode is automatically selected whenever a valid differential signal is detected at the SD± input pins during a Hard or Soft Reset. Pulling both SD+ and SD- low simultaneously, during Hard or Soft Reset, disables the 100BASE-FX mode. The Hard Reset condition sets the entire BCM5208 quad into the FX mode, whereas, the Soft Reset condition may be used to set any individual slice into the FX mode.

10BASE-T MODE

The same magnetics module is used to interface the twisted-pair cable in 10BASE-T mode and in 100BASE-TX mode. The data will be two-level Manchester coded instead of three-level MLT3 and no scrambling/descrambling or 4B5B coding is performed.

Data and clock rates are decreased by a factor of 10, with the MII interface operating at 2.5 MHz. An exception to this occurs when the 10 Base-T repeater serial interface is enabled (SER10 pin is high). In this mode, data is exchanged only on RXD[0] and TXD[0] at the rate of 10 Mbps.

PHY ADDRESS

Each transceiver in the BCM5208 will have a unique PHY address for MII management. The addresses will be set through the PHY address pins. The pins are latched at the trailing end of reset. Transceiver 1 will have the address AAA00, where AAA=PHYAD[4:2]. Transceivers 2-4 will have addresses AAA01, AAA10 and AAA11, respectively.

Every time an MII write or read operation is executed, the transceiver compares the PHY address with its own PHY address definition. The operation is executed only when the addresses match.

SECTION 5: REGISTER SUMMARY

MEDIA INDEPENDENT INTERFACE (MII) MANAGEMENT INTERFACE: REGISTER PROGRAMMING

The BCM5208 fully complies with the IEEE 802.3u Media Independent Interface (MII) specification. The MII management interface registers of each port are serially written-to and read-from using a common set of MDIO and MDC pins. A single clock waveform must be provided to the BCM5208 at a rate of 0-12.5 MHz through the MDC pin. The serial data is communicated on the MDIO pin. Every MDIO bit must have the same period as the MDC clock. The MDIO bits are latched on the rising edge of the MDC clock.

See Table 5 for the fields in every MII read or write instruction frame.

Table 5: MII Management Frame Format

OPERATION	*PRE*	*ST*	*OP*	*PHYAD*	*REGAD*	*TA*	*DATA*	*IDLE*	*DIRECTION*
READ	1 ... 1	01	10	AAAAA	RRRRR	ZZ Z0	Z ... Z D ... D	Z Z	Driven to BCM5208 Driven by BCM5208
WRITE	1 ... 1	01	01	AAAAA	RRRRR	10	D ... D	Z	Driven to BCM5208

Preamble (PRE). Thirty two consecutive “1” bits must be sent through the MDIO pin to the BCM5208 to signal the beginning of an MII instruction. Fewer than 32 “1” bits will cause the remainder of the instruction to be ignored.

Start of Frame (ST). A “01” pattern indicates that the start of the instruction follows.

Operation Code (OP). A READ instruction is indicated by “10”, while a WRITE instruction is indicated by “01”.

PHY Address (PHYAD). A 5-bit PHY address follows next, with the MSB transmitted first. The PHY address allows a single MDIO bus to access multiple PHY chips. The BCM5208 supports the full 32-PHY address space with PHYAD[4:2] input-pin controlled and PHYAD[1:0] internally decoded to select one of the four transceivers.

Register Address (REGAD). A 5-bit Register Address follows, with the MSB transmitted first. The register map of the BCM5208, containing register addresses and bit definitions, are provided on the following pages.

Turnaround (TA). The next two bit times are used to avoid contention on the MDIO pin when a Read operation is performed. For a Write operation, “10” must be sent to the BCM5208 chip during these two bit times. For a Read operation, the MDIO pin must be placed into High-Impedance during these two bit times. The chip will drive the MDIO pin to “0” during the second bit time.

Data. The last 16 bits of the frame are the actual data bits. For a Write operation, these bits are sent to the BCM5208, whereas, for a Read operation, these bits are driven by the BCM5208. In either case, the MSB is transmitted first.

When writing to the BCM5208, the data field bits must be stable 10 ns before the rising-edge of MDC, and must be held valid for 10 ns after the rising edge of MDC. When reading from the BCM5208, the data field bits are valid after the rising-edge of MDC until the next rising-edge of MDC.

Idle. A high impedance state of the MDIO line. All tri-state drivers are disabled and the PHY’s pull-up resistor pulls the MDIO line to logic “1”. Note that at least one or more clocked idle states are required between frames.Following are two examples of MII write and read instructions:

- To put a transceiver with PHY address 00001 into Loopback mode, the following MII write instruction must be issued:
  1111 1111 1111 1111 1111 1111 1111 1111 0101 00001 00000 10 0100 0000 0000 0000 1...
- To determine if a PHY is in the link pass state, the following MII read instruction must be issued:
  1111 1111 1111 1111 1111 1111 1111 1111 0110 00001 00001 ZZ ZZZZ ZZZZ ZZZZ ZZZZ 1...

For the MII read operation, the BCM5208 will drive the MDIO line during the TA and Data fields (the last 17 bit times). A final 65th clock pulse must be sent to close the transaction, and cause a write operation to take place.

MII REGISTER MAP SUMMARY

Table 6 contains the MII register summary for each port of the BCM5208. The register addresses are specified in hex form, and the name of register bits have been abbreviated. When writing to the reserved bits, always write a “0” value, and when reading from these bits, ignore the output value. Never write any value to an undefined register address. The reset value of the registers are shown in the INIT column.

Table 6: MII Register Map Summary

ADDR	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	INIT
00h	**CONTROL**	Soft Reset	Loopback	Force100	AutoNeg Enable	Power Down	Isolate	Restart AutoNeg	Full Duplex	Collision Test	Reserved							3000h
01h	**STATUS**	T4 Capable (0)	TX FDX Capable	TX Capable	10BT FDX Capable	10BT Capable	Reserved				MF pream suppress	AutoNeg Complete	Remote Fault	AutoNeg Capable	Link Status	Jabber Detect	Extd Reg Capable	7809h
02h	**PHYID HIGH**	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0040h
03h	**PHYID LOW**	0	1	1	0	0	0	Model # 0	1	0	0	1	1	Revision # 0	1	1	0	6163h
04h	**AUTONEG ADVERTISE**	Next Page 0	Reserved	Remote Fault	Reserved Technologies		Pause	Adv T4 (0)	Adv TX FDX	Adv TX	Adv BT FDX	Adv BT	Advertised Selector Field [4:0] 0	0	0	0	1	01E1h
05h	**LINK PARTNER ABILITY**	LP Next Page	LP Acknowlg	LP Remote Fault	Reserved Technologies		LP Pause	LP T4	LP TX FDX	LP TX	LP BT FDX	LP BT	Link Partner Selector Field [4:0]					0000h
06h	**AUTONEG EXPANSION**	Reserved											ParDet Fault	LP Next Pg Able	Next Pg Able	Page Recvd	LP Auto Neg Able	0000h
07h	**NEXT PAGE**	Reserved																0000h
10h	**100BASE-X AUX CONTROL**	Reserved		Trans Disable	CIM Disable	Reserved	Bypass 4B5B enc/dec	Bypass Scram/ Descram	Bypass NRZI enc/dec	Bypass rcv sym alignment	Baseline Wander cor Disable	FEF Enable	Reserved					
11h	**100BASE-X AUX STATUS**	- Reserved					FX Mode	Locked	Current 100 Link Status	Current Remote Fault	DISCNCT State (Note 1)	False Carrier Detected	Bad ESD Detected	RCV Error Detected	XMT Error Detected	Lock Error Detected	MLT3 Error Detected	
12h	**100BASE-X RCV ERROR COUNTER**	Reserved								Receive Error Counter								0000h
13h	**100BASE-X FALSE CARRIER COUNTER**	Reserved								False Carrier Sense Counter								0000h

Note 1: Reg 11h: Only bit 6 is qualified with TX Link. Other bits may be set in non-TX operation.

Table 6: MII Register Map Summary(Continued)

ADDR	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	INIT
14h	**100BASE-X DISCONNECT COUNTER**	Reserved								Disconnect Counter								0000h
15h	**Reserved**	Reserved																
16h	**Reserved**	Reserved																
17h	**PTEST**	Reserved - Write as Zero															DISCNCT State (Note 2)	0000h
18h	**AUXILIARY CONTROL/STATUS**	Jabber Disable	Force Link	Reserved					Rsvd.	HSQ	LSQ	Edge Rate [1:0]		AutoNeg Enable Indicator	Force 100 Indicator	SP100 Indicator	FDX Indicator	003xh
19h	**AUXILIARY STATUS SUMMARY**	AutoNeg Complete	AutoNeg FLP-Link Good-Chk	AutoNeg Ack Detect	AutoNeg Ability Detect	AutoNeg Pause	AutoNeg HCD			AutoNeg ParDet Fault	LP Remote Fault	LP Page Rcvd	LP AutoNeg Able	SP100 Indicator	Link Status	Internal AutoNeg Enabled	Jabber Detect	0000h
1Ah	**INTERRUPT**	FDX LED Enable	INTR Enable	Reserved		FDX Mask	SPD Mask	Link Mask	INTR Mask	Reserved				FDX Change	SPD Change	Link Change	INTR Status	0F00h
1Bh	**AUXILLIARY MODE 2**	Reserved								Block 10BASE T Echo Mode	Traffic Meter LED Mode	Activity LED Force ON	Serial LED Mode	SQE Disable Mode	Reserved	Qual Parallel Detect Mode	Reserved	FF00h
1Ch	**10BASE-T AUX. ERROR & GENERAL STATUS**	Reserved					Manchstr Code Err (10BT)	EOF Err (10BT)	Polarity Err (10BT)	0	Revision # 0	1	Repeater Mode Indicator	AutoNeg Enable Indicator	Force 100 Indicator	SP100 Indicator	FDX Indicator	00xxh
1Dh	**AUXILIARY MODE**	Segmentation Control [1:0]		PHY Enable	SEG Enable	Reserved							Activity LEDs Force Inactive	Link LED Force Inactive	Reserved	Block TXEN Mode	Reserved	x000h
1Eh	**AUXILIARY MULTI-PHY**	HCD TX FDX	HCD T4 (0)	HCD TX	HCD 10BT FDX	HCD 10BT	Reserved		Restart AutoNeg	AutoNeg Complete	FLP-Link Good-Chk	ACK Detect	Ability Detect	Super Isolate	Reserved	10BASE T Serial Mode	RXER Code Mode	0000h
1Fh	**BROADCOM Test**	Reserved - Do Not Write																

Note 2: Bit 0 is qualified with TX Link.

MII CONTROL REGISTER

The MII control register bit descriptions are shown in Table 7.

Table 7: MII Control Register (Address 00d, 00h)

BIT	*NAME*	*R/W*	*DESCRIPTION*	*DEFAULT*
15	Reset	R/W (S/C)	1 = PHY reset 0= normal operation	0
14	Loopback	R/W	1 = loopback mode 0 = normal operation	0
13	Forced Speed Selection	R/W	1 = 100 Mbps 0 = 10 Mbps	1
12	Auto-Negotiation Enable	R/W	1 = Auto-Negotiation enable 0 = Auto-Negotiation disable	1
11	Power Down	RO	0 = normal operation	0
10	Isolate	R/W	1 = electrically isolate PHY from MII 0 = normal operation	0
9	Restart Auto-Negotiation	R/W (S/C)	1 = restart Auto-Negotiation 0 = normal operation	0
8	Duplex Mode	R/W	1 = full-duplex 0 = half-duplex	0
7	Collision Test Enable	R/W	1 = collision test mode enable 0 = collision test mode disable	0
6:0	Reserved	RO	Ignore when Read	0
Note: R/W = Read/Write, RO = Read Only, SC = Self Clear				

RESET. In order to reset the BCM5208 by software control, a “1” must be written to bit 15 of the Control Register using an MII write operation. The bit clears itself after the reset process is complete, and need not be cleared using a second MII write. Writes to other Control Register bits will have no effect until the reset process is completed, which requires approximately 1 μs. Writing a “0” to this bit has no effect. Since this bit is self-clearing, after a few cycles from a write operation, it will return a “0” when read.

LOOPBACK. The BCM5208 may be placed into loopback mode by writing a “1” to bit 14 of the Control Register. The loopback mode may be cleared by writing a “0” to bit 14 of the control register, or by resetting the chip. When this bit is read, it will return a “1” when the chip is in software-controlled loopback mode, otherwise it will return a “0”.

FORCED SPEED SELECTION. If Auto-Negotiation is enabled, this bit has no effect on the speed selection. However, if Auto-Negotiation is disabled by software control, the operating speed of the BCM5208 can be forced by writing the appropriate value to bit 13 of the Control Register. Writing a “1” to this bit forces 100BASE-X operation, while writing a “0” forces 10BASE-T operation. When this bit is read, it returns the value of the software-controlled forced speed selection only. In order to read the overall state of forced speed selection, including both hardware and software control, use bit 8 of the Auxiliary Control Register.

AUTO-NEGOTIATION ENABLE. Auto-Negotiation can be disabled by one of two methods: hardware or software control. If the ANEN input pin is driven to a logic “0”, Auto-Negotiation is disabled by hardware control. If bit 12 of the Control Register is written with a value of “0”, Auto-Negotiation is disabled by software control. When Auto-Negotiation is disabled in this manner, writing a “1” to the same bit of the Control Register or resetting the chip will re-enable Auto-Negotiation. Writing to this bit has no effect when Auto-Negotiation has been disabled by hardware control. When read, this bit will return the value most recently written to this location, or “1” if it has not been written since the last chip reset.

POWER DOWN. The BCM5208 does not implement a low power mode.

ISOLATE. Each individual PHY may be isolated from its Media Independent Interface by writing a “1” to bit 10 of the Control Register. All MII outputs will be tri-stated and all MII inputs will be ignored. Since the MII management interface is still active, the isolate mode may be cleared by writing a “0” to bit 10 of the control register, or by resetting the chip. When this bit is read, it will return a “1” when the chip is in isolate mode, otherwise it will return a “0”.

RESTART AUTO-NEGOTIATION. Bit 9 of the Control Register is a self-clearing bit that allows the Auto-Negotiation process to be restarted, regardless of the current status of the Auto-Negotiation state machine. In order for this bit to have an effect, Auto-Negotiation must be enabled. Writing a “1” to this bit restarts the Auto-Negotiation, while writing a “0” to this bit has no effect. Since the bit is self-clearing after only a few cycles, it always returns a “0” when read. The operation of this bit is identical to bit 9 of the Auxiliary Multiple PHY Register.

DUPLEX MODE. By default, the BCM5208 powers up in half-duplex mode. The chip can be forced into full-duplex mode by writing a “1” to bit 8 of the Control Register while Auto-Negotiation is disabled. Half-duplex mode can be resumed by writing a “0” to bit 8 of the control register, or by resetting the chip.

COLLISION TEST. The COL pin may be tested during loopback by activating the Collision Test mode. While in this mode, asserting TXEN will cause the COL output to go high within 512 bit times. Deasserting TXEN will cause the COL output to go low within 4 bit times. Writing a “1” to bit 7 of the Control Register enables the Collision Test mode. Writing a “0” to this bit or resetting the chip disables the Collision Test mode. When this bit is read, it will return a “1” when the Collision Test mode has been enabled, otherwise it will return a “0”. This bit should only be set while in loopback test mode.

RESERVED BITS. All reserved MII register bits must be written as “0” at all times. Ignore the BCM5208 output when these bits are read.

MII STATUS REGISTER

The MII status register bit descriptions are shown in Table 8.

Table 8: MII Status Register (Address 01d, 01h)

BIT	*NAME*	*R/W*	*DESCRIPTION*	*DEFAULT*
15	100BASE-T4 Capability	RO	0 = Not 100BASE-T4 capable	0
14	100BASE-TX FDX Capability	RO	1 = 100BASE-TX full-duplex capable	1
13	100BASE-TX Capability	RO	1 = 100BASE-TX half-duplex capable	1
12	10BASE-T FDX Capability	RO	1 = 10BASE-T full-duplex capable	1
11	10BASE-T Capability	RO	1 = 10BASE-T half-duplex capable	1
10:7	Reserved	RO	Ignore when Read	0
6	MF Preamble Suppression	R/W	1 = Preamble may be suppressed 0 = Preamble always required	0
5	Auto-Negotiation Complete	RO	1 = Auto-Negotiation process completed 0 = Auto-Negotiation process not completed	0
4	Remote Fault	RO LH	1 = Far-end fault condition detected 0 = No far-end fault condition detected	0
3	Auto-Negotiation Capability	RO	1 = Auto-Negotiation capable 0 = Not Auto-Negotiation capable	1
2	Link Status	RO LL	1 = Link is up (Link Pass state) 0 = Link is down (Link Fail state)	0
1	Jabber Detect	RO LH	1 = Jabber condition detected 0 = No jabber condition detected	0
0	Extended Capability	RO	1 = Extended register capable	1
Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High, (LL and LH clear after read operation)				

100BASE-T4 CAPABILITY. The BCM5208 is not capable of 100BASE-T4 operation, and will return a “0” when bit 15 of the status register is read.

100BASE-X FULL-DUPLEX CAPABILITY. The BCM5208 is capable of 100BASE-X full-duplex operation, and will return a “1” when bit 14 of the Status Register is read.

100BASE-X HALF-DUPLEX CAPABILITY. The BCM5208 is capable of 100BASE-X half-duplex operation, and will return a “1” when bit 13 of the Status Register is read.

10BASE-T FULL-DUPLEX CAPABILITY. The BCM5208 is capable of 10BASE-T full-duplex operation, and will return a “1” when bit 12 of the Status Register is read.

10BASE-T HALF-DUPLEX CAPABILITY. The BCM5208 is capable of 10BASE-T half-duplex operation, and will return a “1” when bit 11 of the Status Register is read.

RESERVED BITS Ignore the BCM5208 output when these bits are read.

MF PREAMBLE SUPPRESSION. This bit is the only writable bit in the Status Register. Setting this bit to a “1” allows subsequent MII management frames to be accepted with or without the standard preamble pattern. When Preamble Suppression is enabled, only 2 preamble bits are required between successive Management Commands, instead of the normal 32.

AUTO-NEGOTIATION COMPLETE. Bit 5 of the Status Register will return a “1” if the Auto-Negotiation process has been completed and the contents of registers 4, 5 and 6 are valid.

REMOTE FAULT. The PHY will return a “1” in bit 4 of the Status Register when its link partner has signalled a far-end fault condition. When a far-end fault occurs, the bit will be latched at “1” and will remain so until the register is read and the remote fault condition has been cleared; this only applies to the FX mode of operation.

AUTO-NEGOTIATION CAPABILITY. The BCM5208 is capable of performing IEEE Auto-Negotiation, and will return a “1” when bit 4 of the Status Register is read, regardless of whether or not the Auto-Negotiation function has been disabled.

LINK STATUS. The BCM5208 will return a “1” on bit 2 of the Status Register when the link state machine is in Link Pass, indicating that a valid link has been established. Otherwise, it will return “0”. When a link failure occurs after the Link Pass state has been entered, the Link Status bit will be latched at “0” and will remain so until the bit is read. After the bit is read, it becomes “1” if the Link Pass state has been entered again.

JABBER DETECT. 10BASE-T operation only. The BCM5208 will return a “1” on bit 1 of the Status Register if a jabber condition has been detected. After the bit is read, or if the chip is reset, it reverts to “0”.

EXTENDED CAPABILITY. The BCM5208 supports extended capability registers, and will return a “1” when bit 0 of the Status Register is read. Several extended registers have been implemented in the BCM5208, and their bit functions are defined later in this section.

PHY IDENTIFIER REGISTERS

The physical indentifier registers bit descriptions are shown in Table 9.

Table 9: PHY Indentifier Registers (Address 02d, 02h, 03d, and 03h)

BIT	*NAME*	*R/W*	*DESCRIPTION*	*VALUE*
15:0	MII Address 00010	RO	PHYID HIGH	0040h
15:0	MII Address 00011	RO	PHYID LOW	6136h

Broadcom Corporation has been issued an Organizationally Unique Identifier (OUI) by the IEEE. It is a 24 bit number, 00-10-18, expressed as hex values. That number, along with the Broadcom Model Number for the BCM5208 part, 13h, and Broadcom Revision number, 01h, is placed into two MII Registers. The translation from OUI, Model Number and Revision Number to PHY Identifier Register occurs as follows:

PHYID HIGH [15:0] = OUI[21:6]
PHYID LOW [15:0] = OUI[5:0] + MODEL[5:0] + REV[3:0]

Note: The two most significant bits of the OUI are not represented (OUI[23:22]).

Table 9 shows the result of concatenating these values in order to form the MII Identifier Registers PHYID HIGH and PHYID LOW.

AUTO-NEGOTIATION ADVERTISEMENT REGISTER

Table 10 shows the auto-negotiation advertisement register bit descriptions.

Table 10: Auto-Negotiation Advertisement Register (Address 04d and 04h)

BIT	*NAME*	*R/W*	*DESCRIPTION*	*DEFAULT*
15	Next Page	R/W	(Not Implemented)	0
14	Reserved	RO	Ignore when Read	
13	Remote Fault	R/W	1 = Transmit Remote Fault	0
12:11	Reserved Technologies	RO	Ignore when Read	
10	Advertise Pause Capability	R/W	1 = Pause Operation for Full-Duplex	0
9	Advertise 100BASE-T4	R/W	0 = Do Not Advertise T4 Capability	0
8	Advertise 100BASE-X FDX	R/W	1 = Advertise 100BASE-X Full-Duplex 0 = Do Not Advertise 100BASE-X Full-Duplex	1 if RPTR = 0 0 if RPTR = 1
7	Advertise 100BASE-X	R/W	1 = Advertise 100BASE-X	1
6	Advertise 10BASE-T FDX	R/W	1 = Advertise 10BASE-T Full-Duplex 0 = Do Not Advertise 10BASE-T Full-Duplex	1 if RPTR = 0 0 if RPTR = 1
5	Advertise 10BASE-T	R/W	1 = Advertise 10BASE-T	1
4:0	Advertise Selector Field	RO	Fixed value: indicates 802.3	00001

NEXT PAGE. The BCM5208 does not implement the Next Page function. Thus, bit 15 of the Advertisement Register must always be written “0”.

REMOTE FAULT. Writing a “1” to bit 13 of the Advertisement Register causes a Remote Fault indicator to be sent to the Link Partner during Auto-Negotiation. Writing a “0” to this bit or resetting the chip clears the Remote Fault transmission bit. This bit returns the value last written to it, or else “0” if no write has been completed since the last chip reset.

RESERVED BITS. Ignore output when read.

PAUSE OPERATION FOR FULL-DUPLEX LINKS. The use of this bit is independent of the negotiated data rate, medium, or link technology. The setting of this bit indicates the availability of additional DTE capability when full-duplex operation is in use. This bit is used by one MAC to communicate Pause Capability to its Link Partner and has no effect on PHY operation.

ADVERTISEMENT BITS. Bits 9:5 of the Advertisement Register allow the user to customize the ability information transmitted to the Link Partner. The default value for each bit reflects the abilities of the BCM5208. By writing a “1” to any of the bits, the corresponding ability will be transmitted to the Link Partner. Writing a “0” to any bit causes the corresponding ability to be suppressed from transmission. Resetting the chip restores the default bit values. Reading the register returns the values last written to the corresponding bits, or else the default values if no write has been completed since the last chip reset. Even though that bit 9, Advertise 100BASE-T4 is writable, it should never be set since the BCM5208 is incapable of the T4 operation.

SELECTOR FIELD. Bits 4:0 of the Advertisement register contain the fixed value “00001”, indicating that the chip belongs to the 802.3 class of PHY transceivers.

AUTO-NEGOTIATION LINK PARTNER (LP) ABILITY REGISTER

Table 11 shows the auto-negotiation link partner ability register bit descriptions.

Table 11: Auto-Negotiation Link Partner Ability Register (Address 05d, 05h)

BIT	*NAME*	*R/W*	*DESCRIPTION*	*DEFAULT*
15	LP Next Page	RO	Link Partner next page bit	0
14	LP Acknowledge	RO	Link Partner acknowledge bit	0
13	LP Remote Fault	RO	Link Partner remote fault indicator	0
12:11	Reserved Technologies	RO	Ignore when Read	000
10	LP Advertise Pause	RO	Link Partner has Pause Capability	0
9	LP Advertise 100BASE-T4	RO	Link Partner has 100BASE-T4 capability	0
8	LP Advertise 100BASE-X FDX	RO	Link Partner has 100BASE-X FDX capability	0
7	LP Advertise 100BASE-X	RO	Link Partner has 100BASE-X capability	0
6	LP Advertise 10BASE-T FDX	RO	Link Partner has 10BASE-T FDX capability	0
5	LP Advertise 10BASE-T	RO	Link Partner has 10BASE-T capability	0
4:0	Link Partner Selector Field	RO	Link Partner selector field	00000

Note that the values contained in the Auto-Negotiation Link Partner Ability Register are only guaranteed to be valid once Auto-Negotiation has successfully completed, as indicated by bit 5 of the MII Status Register.

NEXT PAGE. Bit 15 of the Link Partner Ability Register returns a value of “1” when the Link Partner implements the Next Page function and has Next Page information that it wants to transmit. The BCM5208 does not implement the Next Page function, and thus ignores the Next Page bit, except to copy it to this register.

ACKNOWLEDGE. Bit 14 of the Link Partner Ability Register is used by Auto-Negotiation to indicate that a device has successfully received its Link Partner’s Link Code Word.

REMOTE FAULT. Bit 13 of the Link Partner Ability Register returns a value of “1” when the Link Partner signals that a remote fault has occurred. The BCM5208 simply copies the value to this register and does not act upon it.

RESERVED BITS. Ignore when Read.

PAUSE. Indicates that the link partner pause bit is set.

ADVERTISEMENT BITS. Bits 9:5 of the Link Partner Ability Register reflect the abilities of the Link Partner. A “1” on any of these bits indicates that the Link Partner is capable of performing the corresponding mode of operation. Bits 9:5 are cleared any time Auto-Negotiation is restarted or the BCM5208 is reset.

SELECTOR FIELD. Bits 4:0 of the Link Partner Ability Register reflect the value of the Link Partner’s selector field. These bits are cleared any time Auto-Negotiation is restarted or the chip is reset.

AUTO-NEGOTIATION EXPANSION REGISTER

Table 12 shows the auto-negotiation expansion register bit descriptions.

Table 12: Auto-Negotiation Expansion Register (Address 06d and 06h)

BIT	NAME	R/W	DESCRIPTION	DEFAULT
15:5	Reserved	RO	Ignore when Read	
4	Parallel Detection Fault	RO LH	1 = Parallel Detection fault. 0 = No Parallel Detection fault	0
3	Link Partner Next Page Able	RO	1 = Link Partner has Next Page capability 0 = Link Partner does not have Next Page	0
2	Next Page Able	RO	0 = BCM5208 does not have Next Page capability	0
1	Page Received	RO	1 = New page has been received 0 = New page has not been received	0
0	Link Partner Auto-Negotiation Able	RO LH	1 = Link Partner has Auto-Negotiation capability 0 = Link Partner does not have Auto-Negotiation	0
Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High, (LL and LH clear after read operation)				

PARALLEL DETECTION FAULT. Bit 4 of the Auto-Negotiation Expansion Register is a read-only bit that gets latched high when a parallel detection fault occurs in the Auto-Negotiation state machine. For further details, please consult the IEEE standard. The bit is reset to “0” after the register is read, or when the chip is reset.

LINK PARTNER NEXT PAGE ABLE. Bit 3 of the Auto-Negotiation Expansion Register returns a “1” when the Link Partner has Next Page capabilities. It has the same value as bit 15 of the Link Partner Ability Register.

NEXT PAGE ABLE. The BCM5208 does not have Next Page capabilities, thus it always returns “0” when bit 2 of the Auto-Negotiation Expansion Register is read.

PAGE RECEIVED. Bit 1 of the Auto-Negotiation Expansion Register is latched high when a new Link Code Word is received from the Link Partner, checked, and acknowledged. This bit is cleared when the link is lost or the chip is reset.

LINK PARTNER AUTO-NEGOTIATION ABLE. Bit 0 of the Auto-Negotiation Expansion Register returns a “1” when the Link Partner is known to have Auto-Negotiation capability. Before any Auto-Negotiation information is exchanged, or if the Link Partner does not comply with IEEE Auto-Negotiation, the bit returns a value of “0”.

AUTO-NEGOTIATION NEXT PAGE REGISTER

The BCM5208 does not implement the Next Page function, and thus the Next Page Transmit Register is not accessible. See Table 13 for the bit description.

Table 13: Next Page Transmit Register (Address 07d, 07h)

BIT	NAME	R/W	DESCRIPTION	DEFAULT
15:0	Reserved	RO	(not implemented)	

100BASE-X AUXILIARY CONTROL REGISTER

The 100BASE-X auxiliary control register bit descriptions are shown in Table 14.

Table 14: 100BASE-X Auxiliary Control Register (Address 16d, 10h)

BIT	NAME	R/W	DESCRIPTION	DEFAULT
15:14	Reserved			
13	Transmit Disable	R/W	1 = transmitter disabled in PHY 0 = normal operation	0
12	CIM Disable	R/W	1 = disable Carrier Integrity Monitor function 0 = enable Carrier Integrity Monitor function	1 if RPTR = 0 CIM PIN if RPTR = 1
11	Reserved			
10	Bypass 4B5B Encoder/ Decoder	R/W	1 = transmit and receive 5B codes over MII pins 0 = normal MII interface	0
9	Bypass Scrambler/ Descrambler	R/W	1 = scrambler and descrambler disabled 0 = scrambler and descrambler enabled	0
8	Bypass NRZI Encoder/ Decoder	R/W	1 = NRZI encoder and decoder is disabled 0 = NRZI encoder and decoder is enabled	0
7	Bypass Receive Symbol Alignment	R/W	1 = 5B receive symbols not aligned 0 = receive symbols aligned to 5B boundaries	0
6	Baseline Wander Correction Disable	R/W	1 = baseline wander correction disabled 0 = baseline wander correction enabled	0
5	FEF Enable	R/W	1 = Far End Fault enabled 0 = Far End Fault disabled	0
4:0	Reserved	R/W	Write as 0; Ignore on read	

TRANSMIT DISABLE. The transmitter may be disabled by writing a “1” to bit 13 of MII Register 10h. When the transmitter is disabled, in the TX mode, the transmitter output (TD±) will be forced into MLT3 zero value, and, in the FX mode, the transmitter generates the “OFF” state. The transmitter will be enabled at reset, as well as, when a “0” is written to this bit.

CIM DISABLE. The carrier integrity monitor for this port may be disabled by writing a “1” to bit 12 of MII Register 10h. The CIM function will be enabled when a “0” is written to this bit. The default value of this bit after reset will be determined by the CIM mode select pin, if RPTR=1. If RPTR=0 during reset, the CIM function is disabled by default.

BYPASS 4B5B ENCODER/DECODER. The 4B5B encoder and decoder may be bypassed by writing a “1” to bit 10 of MII Register 10h. The transmitter will send 5B codes from the TXER and TXD[3:0] pins directly to the scrambler. TXEN will be ignored and frame encapsulation (insertion of J/K and T/R codes) will not be performed. The receiver will place de-scrambled and aligned 5B codes onto the RXER and RXD[3:0] pins. CRS will still be asserted when a valid frame is received.

BYPASS SCRAMBLER/DESCRAMBLER. The stream cipher function may be disabled by writing a “1” to bit 9 of MII register 10h. The stream cipher function may be re-enabled by writing a “0” to this bit.

BYPASS NRZI ENCODER/DECODER. The NRZI encoder and decoder may be bypassed by writing a “1” to bit 8 of the MII Register 10h, causing 3-level NRZ data to be transmitted and received on the cable. Normal operation (3-level NRZI encoding and decoding) may be re-enabled by writing a “0” to this bit.

BYPASS RECEIVE SYMBOL ALIGNMENT. Receive symbol alignment may be bypassed by writing a “1” to bit 7 of MII Register 10h. When used in conjunction with the bypass 4B5B encoder/decoder bit, unaligned 5B codes will be placed directly on the RXER and RXD[3:0] pins.

BASELINE WANDER CORRECTION DISABLE. The baseline wander correction circuit may be disabled by writing a “1” to bit 6 of MII register 10h. The BCM5208 will correct for baseline wander on the receive data signal when this bit is cleared.

FEF Enable. Controls the Far End Fault mechanism associated with 100BASE-FX operation. A “1” enables the FEF function and a “0” disables it.

RESERVED BITS. The Reserved bits of the 100BASE-X Auxiliary Control Register must be written as “0” at all times. Ignore the BCM5208 outputs when these bits are read.

100BASE-X AUXILIARY STATUS REGISTER

See Table 15 for an explanation of the bit descriptions for the 100BASE-X auxiliary status register.

Table 15: 100BASE-X Auxiliary Status Register (Address 17d, 11h)

BIT	*NAME*	*R/W*	*DESCRIPTION*	*DEFAULT*
15:11	Reserved	RO	Ignore on Read	0
10	FX Mode	RO	1 = 100BASE-FX mode 0 = 100BASE-TX or 10BASE-T mode	SD+/- PIN
9	Locked	RO	1 = descrambler locked 0 = descrambler unlocked	0
8	Current 100BASE-X Link Status	RO	1 = link pass 0 = link fail	0
7	Remote Fault	RO	1 = remote fault detected 0 = no remote fault detected	0
6	Disconnect State	RO	1 = PHY link unstable, isolated by CIM 0 = PHY link stable	0
5	False Carrier Detected	RO LH	1 = false carrier detected since last read 0 =no false carrier since last read	0
4	Bad ESD Detected	RO LH	1 = ESD error detected since last read 0 = no ESD error since last read	0
3	Receive Error Detected	RO LH	1 = receive error detected since last read 0 = no receive error since last read	0
2	Transmit Error Detected	RO LH	1 = transmit error code received since last read 0 = no transmit error code received since last read	0
1	Lock Error Detected	RO LH	1 = lock error detected since last read 0 =no lock error since last read	0
0	MLT3 Code Error Detected	RO LH	1 = MLT3 code error detected since last read 0 = no MLT3 code error since last read	0
Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High, (LL and LH clear after read operation)				

FX MODE. The FX Mode is only enabled when, during a Hard or Soft Reset, the value derived from the SD± input pins are driven with a valid differential signal level. Returns a “0” when both SD+ and SD- are simultaneously driven low during the Hard or Soft Reset.

LOCKED. The PHY will return a “1” in bit 9 when the de-scrambler is locked to the incoming data stream. Otherwise it will return a “0”.

CURRENT 100BASE-X LINK STATUS. The PHY will return a “1” in bit 8 when the 100BASE-X link status is good. Otherwise it will return a “0”.

REMOTE FAULT. The PHY will return a “1” when its link partner signals a far-end fault condition, otherwise returns a “0”.

DISCONNECT STATE. The PHY will return a “1” in bit 6 when the link is unstable and the carrier integrity monitor has isolated the port. Otherwise it will return a “0”. This bit is qualified by 100BASE-X operation.

FALSE CARRIER DETECTED. The PHY will return a “1” in bit 5 of the extended status register if a false carrier has been detected since the last time this register was read. Otherwise it will return a “0”.

BAD ESD DETECTED. The PHY will return a “1” in bit 4 if an end of stream delimiter error has been detected since the last time this register was read. Otherwise it will return a “0”.

RECEIVE ERROR DETECTED. The PHY will return a “1” in bit 3 if a packet was received with an invalid code since the last time this register was read. Otherwise it will return a “0”.

TRANSMIT ERROR DETECTED. The PHY will return a “1” in bit 2 if a packet was received with a transmit error code since the last time this register was read. Otherwise it will return a “0”.

LOCK ERROR DETECTED. The PHY will return a “1” in bit 1 if the de-scrambler has lost lock since the last time this register was read. Otherwise it will return a “0”.

MLT3 CODE ERROR DETECTED. The PHY will return a “1” in bit “0” if an MLT3 coding error has been detected in the receive data stream since the last time this register was read. Otherwise it will return a “0”. ..

100BASE-X RECEIVE ERROR COUNTER

The 100BASE-X receive error counter will increment each time the BCM5208 receives a non-collision packet containing at least one receive error. The counter will automatically clear itself when read. When the counter reaches its maximum value, FFh, it stops counting Receive Errors until cleared. See Table 16 for the bit descriptions.

Table 16: 100BASE-X Receive Error Counter (Address 18d, 012h)

BIT	NAME	R/W	DESCRIPTION	DEFAULT
15:8	Reserved	RO	Write as 0; Ignore when Read	
7:0	Receive Error Counter	R/W	Number of Non-Collision packets with Receive Errors since last Read	00h

100BASE-X FALSE CARRIER SENSE COUNTER

The 100BASE-X false carrier sense counter will increment each time the BCM5208 detects a false carrier on the receive input. The counter will automatically clear itself when read. When the counter reaches its maximum value, FFh, it stops counting False Carrier Sense Errors until cleared. See Table 17 for the bit descriptions.

Table 17: 100BASE-X False Carrier Sense Counter (Address 19d, 13h)

BIT	NAME	R/W	DESCRIPTION	DEFAULT
15:8	Reserved	RO	Write as 0, Ignore when Read	
7:0	False Carrier Sense Counter	R/W	Number of False Carrier Sense events since last Read	00h

100BASE-X DISCONNECT COUNTER

The 100BASE-X disconnect counter will increment each time the carrier integrity monitor within the BCM5208 enters the “link unstable” state. The counter will automatically clear itself when read. When the counter reaches its maximum value, FFh, it stops counting Disconnects until cleared. See Table 18 for the bit descriptions.

Table 18: 100BASE-X Disconnect Counter (Address 20d, 14h)

BIT	NAME	R/W	DESCRIPTION	DEFAULT
15:8	Reserved	RO	Write as 0, Ignore when Read	
7:0	Disconnect Counter	R/W	Number of Disconnects since last Read	00h

AUXILIARY CONTROL/STATUS REGISTER

Table 19 shows the auxiliary control/status register bit descriptions.

Table 19: Auxiliary Control/Status Register (Address 24d, 18h)

BIT	*NAME*	*R/W*	*DESCRIPTION*	*DEFAULT*
15	Jabber Disable	R/W	1= Jabber function disabled in PHY 0 = Jabber function enabled in PHY	0
14	Link Disable	R/W	1= Link Integrity test disabled in PHY 0 = Link Integrity test is enabled in PHY	0
13:8	Reserved	RO	Ignore when Read	000000
7:6	HSQ : LSQ	R/W	These two bits define the Squelch Mode of the 10BASE-T Carrier Sense mechanism: 00 = normal squelch 01 = low squelch 10 = high squelch 11 = not allowed	00
5:4	Edge Rate [1:0]	R/W	00 = 1 ns 01 = 2 ns 10 = 3 ns 11 = 4 ns	11
3	Auto-Negotiation Indicator	RO	1 = Auto-Negotiation activated 0 = Speed forced manually	1
2	Force 100/10 Indication	RO	1 = Speed forced to 100BASE-X 0 = Speed forced to 10BASE-T	1
1	Speed Indication	RO	1 = 100BASE-X 0 = 10BASE-T	0
0	Full-Duplex Indication	RO	1 = Full-duplex active 0 = Full-duplex not active	0

JABBER DISABLE. 10BASE-T operation only. Bit 15 of the Auxiliary Control Register allows the user to disable the Jabber Detect function, defined in the IEEE standard. This function shuts off the transmitter when a transmission request has exceeded a maximum time limit. By writing a “1” to bit 15 of the Auxiliary Control Register, the Jabber Detect function is disabled. Writing a “0” to this bit or resetting the chip restores normal operation. Reading this bit returns the value of Jabber Detect Disable.

LINK DISABLE. Writing a “1” to bit 14 of the Auxiliary Control Register allows the user to disable the Link Integrity state machines, and place the BCM5208 into forced Link Pass status. Writing a “0” to this bit or resetting the chip restores the Link Integrity functions. Reading this bit returns the value of Link Integrity Disable.

TEST MODE. Active-high test mode control bit. Must be written with “0” for normal operation.

HSQ AND LSQ. Extend or decrease the squelch levels for detection of incoming 10BASE-T data packets. The default squelch levels implemented are those defined in the IEEE standard. The high- and low-squelch levels are useful for situations where the IEEE-prescribed levels are inadequate. The squelch levels are used by the CRS/LINK block to filter out noise and recognize only valid packet preambles and link integrity pulses. Extending the squelch levels allows the BCM5208 to operate properly over longer cable lengths. Decreasing the squelch levels may be useful in situations where there is a high level of noise present on the cables. Reading these two bits returns the value of the squelch levels.

EDGE RATE. Control bits used to program the transmit DAC output edge rate in 100BASE-TX mode. These bits are logically AND’ed with the ER[1:0] input pins to produce the internal edge-rate controls (Edge_Rate[1] AND ER[1], Edge_Rate[0] AND ER[0]).

AUTO-NEGOTIATION INDICATOR. A read-only bit that indicates whether Auto-Negotiation has been enabled or disabled on the BCM5208. A combination of a “1” in bit 12 of the Control Register and a logic “1” on the ANEN input pin is required to enable Auto-Negotiation. When Auto-Negotiation is disabled, bit 3 of the Auxiliary Control Register returns a “0”. At all other times, it returns a “1”.

FORCE100/10 INDICATION. A read-only bit that returns a value of “0” when one of following two cases is true:

1. The ANEN pin is low AND the F100 pin is low.
2. Bit 12 of the Control Register has been written “0” AND bit 13 of the Control Register has been written “0”. When bit 8 of the Auxiliary Control Register is “0”, the speed of the chip will be 10BASE-T. In all other cases, either the speed is not forced (Auto-Negotiation is enabled), or the speed is forced to 100BASE-X.

SPEED INDICATION. Bit 1 of the Auxiliary Control Register is a read-only bit that shows the true current operation speed of the BCM5208. A “1” bit indicates 100BASE-X operation, while a “0” indicates 10BASE-T. Note that while the Auto-Negotiation exchange is performed, the BCM5208 is always operating at 10BASE-T speed.

FULL-DUPLEX INDICATION. Bit 0 of the Auxiliary Control Register is a read-only bit that returns a “1” when the BCM5208 is in full-duplex mode. In all other modes, it returns a “0”.

AUXILIARY STATUS SUMMARY REGISTER

The Auxiliary Status Summary Register contains copies of redundant status bits found elsewhere within the MII register space. Descriptions for each of these individual bits can be found associated with their primary register descriptions. Bits 10:8, the Auto-Negotiation HCD, are only set for full Auto-Negotiation process, and not for either Parallel Detection or forced speed modes. Table 20 shows the bit descriptions.

Table 20: Auxiliary Status Summary Register (Address 25d, 19h)

BIT	*NAME*	*R/W*	*DESCRIPTION*	*DEFAULT*
15	Auto-Negotiation Complete	RO	1 = Auto-Negotiation process completed.	0
14	Auto-Negotiation Flp-Link Good-Check	RO LH	1 = Auto-Negotiation FLP-Link Good Check.	0
13	Auto-Negotiation Acknowledge Detected	RO LH	1 = Auto-Negotiation acknowledge detected.	0
12	Auto-Negotiation Ability Detect	RO LH	1 = Auto-Negotiation for link partner ability.	0
11	Auto-Negotiation Pause	RO	BCM5208 & link partner Pause Operation bit set.	0
10:8	Auto-Negotiation HCD	RO	000 = No Highest Common Denominator 001 = 10BASE-T 010 = 10BASE-T Full-Duplex 011 = 100BASE-TX 100 = 100BASE-T4 101 = 100BASE-TX Full-Duplex 11x = undefined	000
7	Auto-Negotiation Parallel Detection Fault	RO LH	1 = Parallel Detection fault.	0
6	Link Partner Remote Fault	RO		
5	Link Partner Page Received	RO LH	1 = New Page has been received.	0
4	Link Partner Auto-Negotiation Able	RO	1 = Link Partner is Auto-Negotiation capable.	0
3	Speed Indicator	RO	1 = 100 Mbps 0 = 10 Mbps	0
2	Link Status	RO LL	1 = Link is Up (link pass state)	0
1	Auto-Negotiation Enabled	RO	1 = Auto-Negotiation enabled.	1
0	Jabber Detect	RO LL	1 = Jabber condition detected.	0

Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High (LL and LH clear after read operation)

INTERRUPT REGISTER

Table 21 shows the bit descriptions for the interrupt register.

Table 21: Interrupt Register (Address 26d, 1Ah)

BIT	*NAME*	*R/W*	*DESCRIPTION*	*DEFAULT*
15	FDX LED Enable	R/W	Full-Duplex LED Enable	0
14	INTR Enable	R/W	Interrupt Enable	0
13:12	Reserved	RO		0
11	FDX Mask	R/W	Full-Duplex Interrupt Mask	1
10	SPD Mask	R/W	SPEED Interrupt Mask	1
9	LINK Mask	R/W	LINK Interrupt Mask	1
8	INTR Mask	R/W	Master Interrupt Mask	1
7:4	Reserved	RO		0
3	FDX Change	RO LH	Duplex Change Interrupt	0
2	SPD Change	RO LH	Speed Change Interrupt	0
1	LINK Change	RO LH	Link Change Interrupt	0
0	INTR Status	RO LH	Interrupt Status	0

Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High (LL and LH clear after read operation)

FDX LED ENABLE. Setting this bit enables the FDX LED mode. Bits 14 and 15 of this register are mutually exclusive. Only one may be set at a time. When FDXLED mode is enabled, XMTLED# becomes FDXLED# and RCVLED# becomes ACTLED#.

INTERRUPT ENABLE. Setting this bit enables Interrupt Mode. Bits 14 and 15 of this register are mutually exclusive. Only one may be set at a time. When Interrupt Mode is enabled, XMTLED# becomes INTR# and RCVLED# becomes ACTLED#. Side Note: if both bits 14 and 15 are set at the same time, the FDXLED# will override the INTR# output, even though the interrupt's FDX, SPD, and LINK change status bits will behave as in normal interrupt operation.

FDX MASK. When this bit is set, changes in Duplex mode will not generate an interrupt.

SPD MASK. When this bit is set, changes in operating speed will not generate an interrupt.

LINK MASK. When this bit is set, changes in Link status will not generate an interrupt.

INTERRUPT MASK. Master Interrupt Mask. When this bit is set, no interrupts will be generated, regardless of the state of the other MASK bits.

FDX CHANGE. A "1" indicates a change of Duplex status since last register read. Register read clears the bit.

SPD CHANGE. A "1" indicates a change of Speed status since last register read. Register read clears the bit.

LINK CHANGE. A "1" indicates a change of Link status since last register read. Register read clears the bit.

INTERRUPT STATUS. Represents status of the INTR# pin. A "1" indicates that the interrupt mask is off and that one or more of the change bits are set. Register read clears the bit.

AUXILIARY MODE 2 REGISTER

The bit descriptions for auxiliary mode 2 register are shown in Table 22.

Table 22: Auxiliary Mode 2 (Address 27d, 1Bh)

BIT	NAME	R/W	DESCRIPTION	DEFAULT
15:8	Reserved	RO	Ignore when Read	FFh
7	Block 10BASE-T Echo Mode	R/W	1=10BASE-T half-duplex TXEN won't echo onto RXDV 0=10BASE-T half-duplex TXEN will echo onto RXDV	0
6	Traffic Meter LED Mode	R/W	1=Traffic Meter LED Mode ON 0=Traffic Meter LED Mode OFF	0
5	Activity LED Force ON	R/W	1=Activity LEDs Forced ON 0=Activity LEDs not Forced	0
4	Serial LED Mode	R/W	1=Serial LED Mode enabled 0=Serial LED Mode disabled	0
3	SQE Disable Mode	R/W	1=SQE not transmitted in 10BASE-T half-duplex 0=SQE transmitted in 10BASE-T half-duplex	0
2	Reserved	RO	Ignore when Read	0
1	Qual Parallel Detect Mode	R/W	1=Parallel Detect Qualification Mode ON 0=Parallel Detect Qualification Mode OFF	0
0	Reserved	RO	Ignore when Read	0

BLOCK 10BASE-T ECHO MODE. Default 0. When enabled, during 10BASE-T half-duplex transmit operation, the TXEN signal will not echo onto the RXDV pin. The TXEN will echo onto the CRS pin, and the CRS deassertion directly follow the TXEN deassertion.

TRAFFIC METER LED MODE. Default 0. When asserted, the Receive and Transmit (Activity) LEDs (XMTLED# and RCVLED# pins) will not blink based on the internal LED-CLK (approximately 80ms ON time). Instead, they will blink based on the rate of Receive and Transmit activity. Each time a Receive or a Transmit operation occurs, the respective LED will turn on for a minimum of 5ms. With light traffic, the LEDs will blink at a low rate. During medium to heavy traffic (packets within 5ms of each other), the LEDs will remain on.

ACTIVITY LED FORCE ON. Default 0. When asserted, the Receive and Transmit (Activity) LEDs (XMTLED# and RCVLED# pins) will be turned on. When 0, will have no affect on the Activity LEDs. The Activity Force ON bit has higher priority than Activity LED Force Inactive, bit 4, Register 1Dh.

SERIAL LED MODE. Default 0. When asserted, the 4 slices' LED outputs will be serially shifted out on the 2nd slices' LED outputs.The sequence of outputs for the different Serial modes are: FDX, Global Interrupt, Speed, Link, Slice Interrupt, Activity when the Interrupt mode is set; FDX, '1', Speed, Link, FDX, Activity when the FDXLED mode is set and, FDX, '1', Speed, Link, Transmit, Receive when neither Interrupt nor FDXLED modes are selected. When this bit is 0, the four LED outputs per slice will be operated in parallel. See Table 3 and refer to the Functional Description section for more details.

SQE DISABLE MODE. Default 0. When asserted, will disable SQE pulses when operating in 10BASE-T half-duplex mode.

QUALIFIED PARALLEL DETECT MODE. This bit allows the Auto-Negotiation/Parallel Detection process to be qualified with information in the Advertisement Register. Default value is 0.

If this bit is not set, and the local BCM5208 device is enabled to Auto-Negotiate and the far-end device is a 10BASE-T or 100BASE-TX non-Auto-Negotiating legacy type, the local device will Auto-Negotiate/Parallel detect the far-end device, regardless of the contents of its Advertisement Register, 04h.

If this bit is set, the local device will compare the link speed detected to the contents of its Advertisement Register. If the particular link speed is enabled in the Advertisement register, the local device will assert link. If the link speed is disabled in this register, then the local device will not assert link and will continue monitoring for a matching capability link speed.

10BASE-T AUXILIARY ERROR & GENERAL STATUS REGISTER

The bit descriptions for the 10BASE-T auxiliary error and general status register are shown in Table 23.

All Error bits in the Auxiliary Error Status Register are read-only and are latched high. When certain types of errors occur in the BCM5208, one or more corresponding error bits become "1". They remain so until the register is read, or until a chip reset occurs. All such errors necessarily result in data errors, and are indicated by a high value on the RXER output pin at the time the error occurs.

Table 23: 10BASE-T Auxiliary Error and General Status Register (Address 28d, 1Ch)

BIT	*NAME*	*R/W*	*DESCRIPTION*	*DEFAULT*
15:11	Reserved	RO	Ignore when read	x
10	Manchester Code Error	RO	1 = Manchester code error (10BASE-T)	0
9	EOF Error	RO	1 = EOF detection error (10BASE-T)	0
8	Polarity Inversion	RO	1 = Channel Polarity Inverted 0 = Channel Polarity Correct	0
7:5	Revision	RO	Revision Number	001
4	Repeater Mode Indication	RO	1 = Repeater mode 0 = DTE mode	0
3	Auto-Negotiation Indication	RO	1 = Auto-Negotiation activated 0 = Speed forced manually	1
2	Force 100/10 Indication	RO	1 = Speed forced to 100BASE-X 0 = Speed forced to 10BASE-T	1
1	Speed Indication	RO	1 = 100BASE-X 0 = 10BASE-T	0
0	Full-Duplex Indication	RO	1 = Full-duplex active 0 = Full-duplex not active	0

MANCHESTER CODE ERROR. Indicates that a Manchester code violation was received. This bit is only valid during 10BASE-T operation.

EOF ERROR. Indicates that the EOF (end of frame) sequence was improperly received, or not received at all. This error bit is only valid during 10BASE-T operation.

POLARITY. Reflects the Polarity status of the receive channel pair. The BCM5208 is capable of automatically inverting the polarity of the receive channel. No data errors are reported to indicate that the automatic polarity inversion is occurring. Instead, this bit returns a "1" whenever the polarity of the receive channel is inverted.

REVISION. Read-only bits that return the revision number of the BCM5208. The current revision is labelled "001".

REPEATER MODE INDICATION. Returns the same value as the RPTR input pin. When the BCM5208 is in DTE mode, it returns a "0". When the BCM5208 is in Repeater mode, it returns a "1".

AUTO-NEGOTIATION INDICATION. A read-only bit that indicates whether Auto-Negotiation has been enabled or disabled on the BCM5208. A combination of a "1" in bit 12 of the Control Register and a logic "1" on the ANEN input pin is required to enable Auto-Negotiation. When Auto-Negotiation is disabled, bit 15 of the Auxiliary Mode Register returns a "0". At all other times, it returns a "1".

FORCE100/10 INDICATION. A read-only bit that returns a value of "0" when one of following two cases is true:

1. The ANEN pin is low AND the F100 pin is low.
2. Bit 12 of the Control Register has been written "0" AND bit 13 of the Control Register has been written "0".

When bit 8 of the Auxiliary Control Register is "0", the speed of the chip will be 10BASE-T. In all other cases, either the speed is not forced (Auto-Negotiation is enabled), or the speed is forced to 100BASE-X.

SPEED INDICATION. A read-only bit that shows the true current operation speed of the BCM5208. A “1” bit indicates 100BASE-X operation, while a “0” indicates 10BASE-T. Note that while the Auto-Negotiation exchange is performed, the BCM5208 is always operating at 10BASE-T speed.

FULL-DUPLEX INDICATION. A read-only bit that returns a “1” when the BCM5208 is in full-duplex mode. In all other modes, it returns a “0”.

AUXILIARY MODE REGISTER

The bit descriptions for the auxiliary mode register are shown in Table 24.

Table 24: Auxiliary Mode Register (Address 29d, 1Dh)

BIT	*NAME*	*R/W*	*DESCRIPTION*	*DEFAULT*
15:14	Segmentation Control	R/W	00 = connect PHY to MII I/F 1 01 = connect PHY to MII I/F 2 10 = connect PHY to MII I/F 3 11 = connect PHY to MII I/F 4	PHY1=00 PHY2=01 PHY3=10 PHY4=11 See Note.
13	PHY Enable	R/W	1 = PHY enabled in segmentation mode 0 = PHY disabled in segmentation mode	0
12	Segmentation Enable	R/W	1 = Segmentation Enabled 0 = Segmentation Disabled	0 if RPTR pin is LOW 1 if RPTR pin is HIGH
11:5	Reserved	RO		0
4	Activity LEDs Force Inactive		1 = Disable XMT/RCV Activity LED outputs 0 = Allow XMT/RCV Activity LED outputs	0
3	Link LED Force Inactive		1 = Disable Link LED output 0 = Allow Link LED output	0
2	Reserved	RO		0
1	Block TXEN Mode	R/W	1 = Enable Block TXEN mode 0 = Disable Block TXEN mode	0
0	Reserved	RO		0
Note: Default is 00 for all PHYs if RPTR pin is high during reset				

SEGMENTATION CONTROL. Applicable only when Segmentation Enable is active**.** These bits select which MII interface this PHY is connected to. If RPTR=1 during reset, these bits default to “00”. If RPTR=0 during reset, these bits default to the PHY number (00 for PHY1, etc.).

PHY ENABLE. Applicable only when Segmentation Enable is active**.** When set to a “1, this PHY is connected to the MII interface specified in the Segmentation Control Register. When “0”, this PHY is disconnected from the selected MII interface.

SEGMENTATION ENABLE. When set to a “1”, segmentation is enabled for this MII interface. When “0” this PHY connects to its default MII interface as specified by the Segmentation Control Register’s default setting. If RPTR=1 during reset, segmentation is enabled by default.

ACTIVITY LEDs FORCE INACTIVE. When set to “1”, the XMTLED# and RCVLED# output pins are forced into their inactive state regardless of the mode (normal, FDX, Interrupt, or Serial) these outputs are configured to. When “0”, XMTLED# and RCVLED# output pins are enabled.

LINK LED FORCE INACTIVE. When set to “1”, the Link LED output pin is forced into its inactive state. When “0”, Link LED output is enabled.

Block TXEN Mode. When this mode is enabled, short IPGs of 1, 2, 3 or 4 TXC cycles will all result in the insertion of two IDLEs before the beginning of the next packet’s JK symbols.

AUXILIARY MULTIPLE PHY REGISTER

The bit descriptions for the auxiliary multiple PHY register are shown in Table 25.

Table 25: Auxiliary Multiple PHY Register (Address 30d, 1Eh)

BIT	*NAME*	*R/W*	*DESCRIPTION*	*DEFAULT*
15	HCD_TX_FDX	RO	1 = Auto-Negotiation result is 100BASE-TX full-duplex	0
14	HCD_T4	RO	0 = BCM5208 doesn't support 100BASE-T4 ability	0
13	HCD_TX	RO	1 = Auto-Negotiation result is 100BASE-TX	0
12	HCD_10BASE-T_FDX	RO	1 = Auto-Negotiation result is 10BASE-T full-duplex	0
11	HCD_10BASE-T	RO	1 = Auto-Negotiation result is 10BASE-T	0
10:9	Reserved	RO	Ignore when Read	0
8	Restart Auto-Negotiation	R/W (SC)	1 = restart Auto-Negotiation process 0 = (No effect)	0
7	Auto-Negotiation Complete	RO	1 = Auto-Negotiation process Completed 0 = Auto-Negotiation process not Completed	0
6	FLP-Link Good-Check	RO	1 = Auto-Negotiation FLP-Link Good-Check	0
5	Acknowledge Detected	RO	1 = Auto-Negotiation Acknowledge Detected	0
4	Ability Detect	RO	1 = Auto-Negotiation waiting for LP Ability	0
3	Super Isolate	R/W	1 = Super Isolate mode 0 = Normal Operation	0
2	Reserved	RO	Ignore when Read	0
1	10BASE-T Serial Mode	R/W	1 = Enable 10BASE-T Serial Mode 0 = Disable 10BASE-T Serial Mode	0
0	RXER Code Mode	R/W	1 = Enable RXER Code Mode 0 = Disable RXER Code Mode	0

HCD BITS. Bits 15:11 of the Auxiliary Multiple PHY Register are five read-only bits that report the Highest Common Denominator (HCD) result of the Auto-Negotiation process. Immediately upon entering the Link Pass state after each reset or Restart Auto-Negotiation, only one of these five bits will be "1". The Link Pass state is identified by a "1" in bit 6 or 7 of this register. The HCD bits are reset to "0" every time Auto-Negotiation is restarted or the BCM5208 is reset. Note that for their intended application, these bits will uniquely identify the HCD only after the first Link Pass after reset or restart of Auto-Negotiation. On later Link Fault and subsequent re-negotiations, if the ability of the Link Partner is different, more than one of the above bits may be active. These bits are only set for full Auto-Negotiation hand-shake, and not for Parallel Detection of Forced speed modes. Note that bit 14, HCD_T4, will never be set in the BCM5208.

RESTART AUTO-NEGOTIATION. A self-clearing bit that allows the Auto-Negotiation process to be restarted, regardless of the current status of the state machine. For this bit to work, Auto-Negotiation must be enabled. Writing a "1" to this bit restarts Auto-Negotiation. Since the bit is self-clearing, it always returns a "0" when read. The operation of this bit is identical to bit 9 of the Control Register.

AUTO-NEGOTIATION COMPLETE. This read-only bit returns a "1" after the Auto-Negotiation process has been completed. It remains "1" until the Auto-Negotiation process is restarted, a Link Fault occurs, or the chip is reset. If Auto-Negotiation is disabled or the process is still in progress, the bit returns a "0".

FLP-Link Good-Check. This read-only bit returns a "1" when the Auto-Negotiation arbitrator state machine has entered the FLP-link Good-Check state. It remains this value until the Auto-Negotiation process is restarted, a Link Fault occurs, Auto-Negotiation is disabled, or the BCM5208 is reset.

ACKNOWLEDGE DETECTED. This read-only bit is set to "1" when the Arbitrator state machine exits the Acknowledged Detect state. It remains high until the Auto-Negotiation process is restarted, or the BCM5208 is reset.

ABILITY DETECT. This read-only bit returns a “1” when the Auto-Negotiation state machine is in the Ability Detect state. It enters this state a specified time period after the Auto-Negotiation process begins, and exits after the first FLP burst or link pulses are detected from the Link Partner. This bit returns a “0” any time the Auto-Negotiation state machine is not in the Ability Detect state.

SUPER ISOLATE. Writing a “1” to this bit places the BCM5208 into the Super Isolate mode. Similar to the Isolate mode, all MII inputs are ignored, and all MII outputs are tri-stated. Additionally, all link pulses are suppressed. This allows the BCM5208 to coexist with another PHY on the same adapter card, with only one being activated at any time.

10BASE-T SERIAL MODE. Writing a “1” to bit 1 of the Auxiliary Mode Register enables the 10BASE-T Serial mode. In the normal 10BASE-T mode of operation, as defined by the IEEE MII standard, transmit and receive data packets traverse the TXD[3:0] and RXD[3:0] busses at a rate of 2.5 MHz. In the special 10BASE-T Serial mode, data packets traverse to the MAC layer across only TXD[0] and RXD[0] at a rate of 10 MHz. Serial operation is not available in 100BASE-X mode. This bit is ORed with the SER10 pin.

RXER CODE MODE. Writing a “1” to bit 0 of the Auxiliary Mode Register enables the RXER Code mode during 10BASE-T operation. In this mode, when a receive data error occurs, indicated by pins RXDV=1 and RXER=1, the RXD[3:0] bus will contain a non-zero 4-bit encoded value indicating the type of error. This feature provides the user with more detailed information regarding the status of the system. Writing a “0” to this bit or resetting the chip restores normal operation. Note that this mode does not disrupt normal communication with the MAC layer, and can safely be used at all times. Also, please note that the RXER Code mode is not available in 10BASE-T Serial mode. In 100BASE-X operation, the RXER code mode is always active. See Table 2.

BROADCOM TEST REGISTER

The Broadcom test register bits are reserved and should never be written.

Table 26: Broadcom Test (Address 31d, 1Fh)

BIT	*NAME*	*R/W*	*DESCRIPTION*	*DEFAULT*
Reserved - Do Not Write				

SECTION 6: TIMING AND AC CHARACTERISTICS

All MII Interface pins comply with IEEE 802.3u timing specifications (See Reconciliation Sub-layer and Media Independent Interface in IEEE 802.3u timing specifications). All digital output timing specified at C_L = 30 pF.

Output rise/fall times measured between 10% and 90% of the output signal swing. Input rise/fall times measured between V_{IL} max. and V_{IH} min. Output signal transitions referenced to the midpoint of the output signal swing. Input signal transitions referenced to the midpoint between V_{IL} max. and V_{IH} min. See Table 27 and Table 28 for timing parameters. See Figure 3 for an illustration of clock and reset timing.

Table 27: Clock Timing

PARAMETER	*SYMBOL*	*MIN*	*TYP*	*MAX*	*UNIT*
CK25 Cycle Time	CK_CYCLE	39.998	40	40.002	ns
CK25 High/Low Time	CK_HI CK_LO	18	20	22	ns
CK25 Rise/Fall Time	CK_EDGE	–	–	4	ns
CK10RPTR (Serial) Cycle Time	CK_CYCLE		100		ns
CK10RPTR (Serial) High/Low Time	CK_HI CK_LO	40		60	ns
CK10RPTR (Serial) Rise/Fall Time	CK_EDGE			4	ns
CK10RPTR (Non-Serial) Cycle Time	CK_CYCLE		400		ns
CK10RPTR (Non-Serial) High/Low Time	CK_HI CK_LO	180		220	ns
CK10RPTR (Non-Serial) Rise/Fall Time	CK_EDGE			4	ns

Table 28: Reset Timing

PARAMETER	*SYMBOL*	*MIN*	*TYP*	*MAX*	*UNIT*
Reset Pulse Length with stable CK25 Input	RESET_LEN	400	–	–	ns
Activity after end of Reset	RESET_WAIT	100	–	–	µs
RESET Rise/Fall Time	RESET_EDGE	–	–	10	ns

Figure 3: Clock and Reset Timing

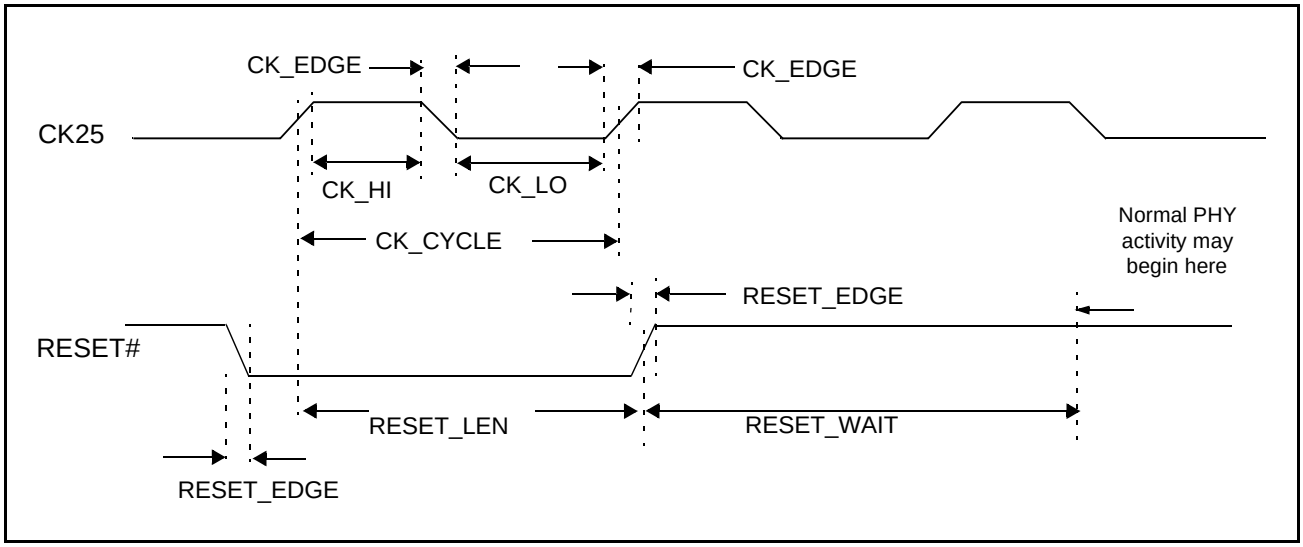


Table 29 provides the parameters for 100BASE-X transmit timing. Figure 4 illustrates 100BASE-TX transmit start of packet timing and Figure 5 shows the 100BASE-TX transmit end of packet timing.

Table 29: 100BASE-X Transmit Timing

PARAMETER	*SYMBOL*	*MIN*	*TYP*	*MAX*	*UNIT*
TXC Cycle Time			40		ns
TXC High/Low Time		16	20	24	ns
TXC Rise/Fall Time		2	–	5	ns
TXEN, TXER, TXJAM, TXD[3:0] Setup Time to TXC rising*	TXEN_SETUP	12	–		ns
TXEN, TXER, TXJAM, TXD[3:0] Hold Time from TXC rising*	TXEN_HOLD	0	–	–	ns
TD± after TXEN Assert	TXEN_TDATA	60	–	80	ns
TXD to TD± Steady State Delay	TXD_TDATA	60	–	80	ns
CRS Assert after TXEN Assert	TXEN_CRS	–	–	30	ns
CRS Deassert after TXEN Deassert	TXEN_CRS_EOP	–	–	30	ns
COL Assert after TXEN Assert (while RX)	TXEN_COL	–	–	30	ns
COL Deassert after TXEN Deassert (while RX)	TXEN_COL_EOP	–	–	30	ns
TXEN, TXER, TXJAM, TXD[3:0] Setup Time to CK25 rising*		2	–		ns
TXEN, TXER, TXJAM, TXD[3:0] Hold Time from CK25 rising*		10	–	–	ns

* The BCM5208 will function properly if the TXEN, TXER, TXJAM and TXD[3:0] inputs meet the setup and hold times to either the TXC (Switch) output or the CK25 (Repeater) input.

Figure 4: Transmit Start of Packet Timing (100BASE-TX)

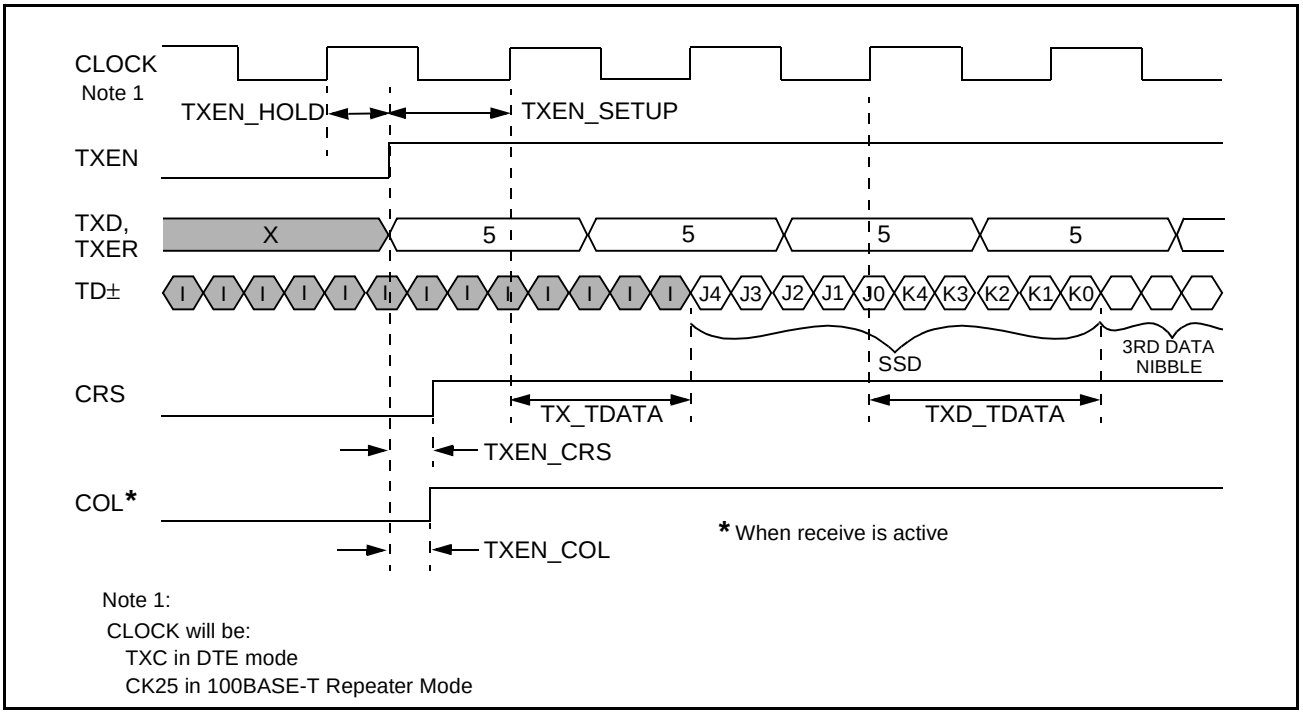


Figure 5: Transmit End of Packet Timing (100 Base-TX)

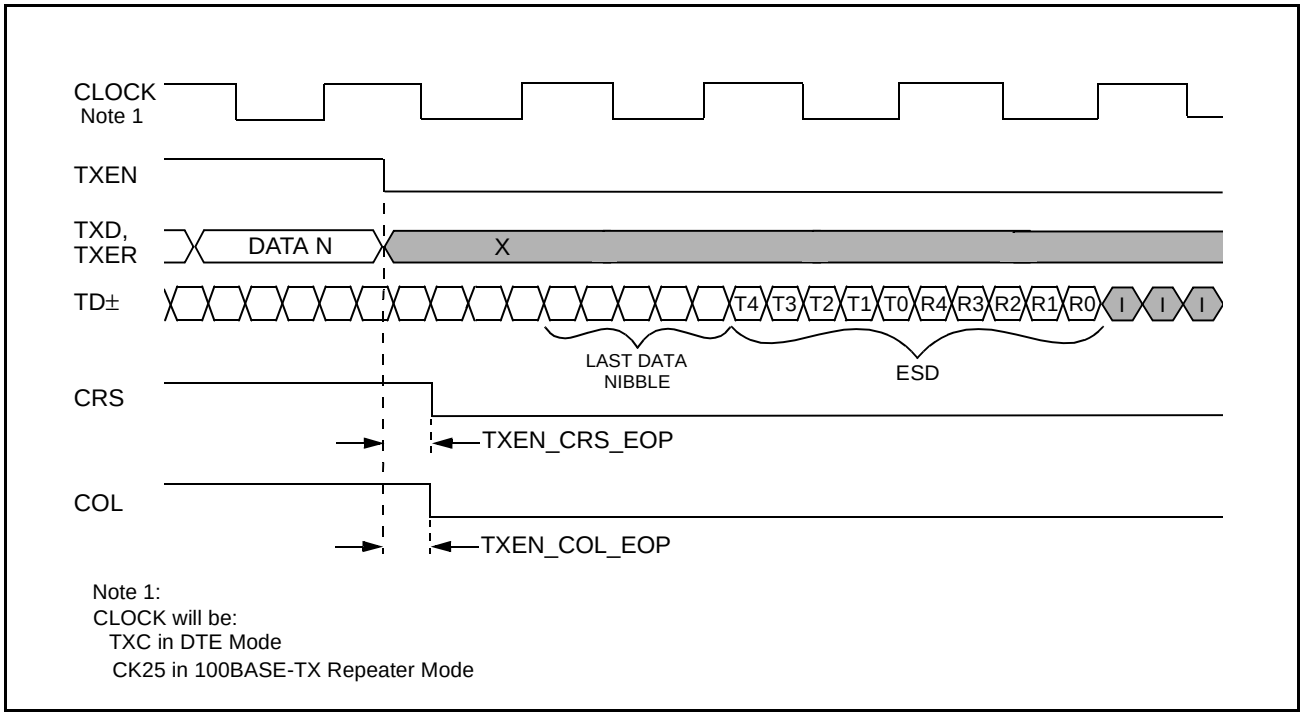


Figure 30 provides the parameters for 10BASE-T transmit timing.

Table 30: 10BASE-T Transmit Timing - Parallel Mode

PARAMETER	*SYMBOL*	*MIN*	*TYP*	*MAX*	*UNIT*
TXC Cycle Time (10BASE-T)	TXC_CYCLE	395	400	405	ns
TXC High/Low Time (10BASE-T)		197.5	200	202.5	ns
TXC Rise/Fall Time		2		5	ns
TXEN, TXD[3:0] valid after TXC rising*	TXEN_VALID			25	ns
TXEN, TXD[3:0] Hold after to TXC rising*	TXEN_HOLD_DTE	75			ns
TD+/- after TXEN Assert	TXEN_TDATA	–	400	450	ns
CRS Assert after TXEN Assert	TXEN_CRS	–	50	100	ns
CRS Deassert after TXEN Deassert	TXEN_CRS_EOP	–	770	1200	ns
COL Assert after TXEN Assert (while RX)	TXEN_COL				
COL Deassert after TXEN Deassert (while RX)	TXEN_COL_EOP				
TXEN, TXD[3:0] Setup Time to CK10RPTR rising*	TXEN_SETUP_RPTR	12			ns
TXEN, TXD[3:0] Hold Time to CK10RPTR rising*	TXEN_HOLD_RPTR	0			ns
Idle on Twisted Pair after TXEN De-Assert	TX_QUIET	-–	460	500	ns

* The BCM5208 will function properly if the TXEN and TXD[3:0] inputs meet the setup and hold times to either the TXC (Switch) output or the CK10RPTR (Repeater) input, respectively.

Figure 31 provides the parameters for 100BASE-X receive timing. Figure 6 illustrates 100BASE-TX receive start of packet timing and Figure 7 shows 100BASE-TX receive end of packet timing. Figure 8 shows 100BASE-TX receive packet premature end. Figure 9 illustrates link failure or stream cipher error during receive packet. False carrier sense timing is shown in Figure 10.

Table 31: 100BASE-X Receive Timing

PARAMETER	*SYMBOL*	*MIN*	*TYP*	*MAX*	*UNIT*
RXC Cycle Time		39.5	40	40.5	ns
RXC High/Low Time (RXDV asserted)		18	20	22	ns
RXC High Time (RXDV deasserted)		18	20	54	ns
RXC Low Time (RXDV deasserted)		18	20	38	ns
RXC Rise/Fall Time		2	–	5	ns
RXDV, RXER, RXD[3:0] Delay from RXC falling		-3	–	3	ns
CRS Deassert from RXC falling (valid EOP only)		-3	–	3	ns
CRS Assert after RD±	RX_CRS	90	–	120	ns
CRS Deassert after RD± (valid EOP)	RX_CRS_EOP	130	–	160	ns
CRS Deassert after RD± (premature end)	RX_CRS_IDLE	170	–	200	ns
RXDV Assert after RD±	RX_RXDV	130	–	160	ns
RXDV Deassert after RD±	RX_RXDV_EOP	130	–	160	ns
RXDV Assert after CRS		35	–	45	ns
RD± to RXD Steady State Delay	RX_RXD	150	–	180	ns
COL Assert after RD± (while TX)	RX_COL	90	–	120	ns
COL Deassert after RD± (valid EOP)	RX_COL_EOP	130	–	160	ns
COL Deassert after RD± (premature end)	RX_COL_IDLE	170	–	200	ns
RXEN high to RXC, RXDV, RXER, RXD[3:0] Delay		0		50	ns
RXC, RXDV, RXER, RXD[3:0] high-Z from RXEN low		20		70	ns

Note: RXC minimum high and low times are guaranteed when RXEN is asserted or deasserted. The MII port will always tri-state while RXC is low.

Figure 6: Receive Start of Packet Timing (100BASE-TX)

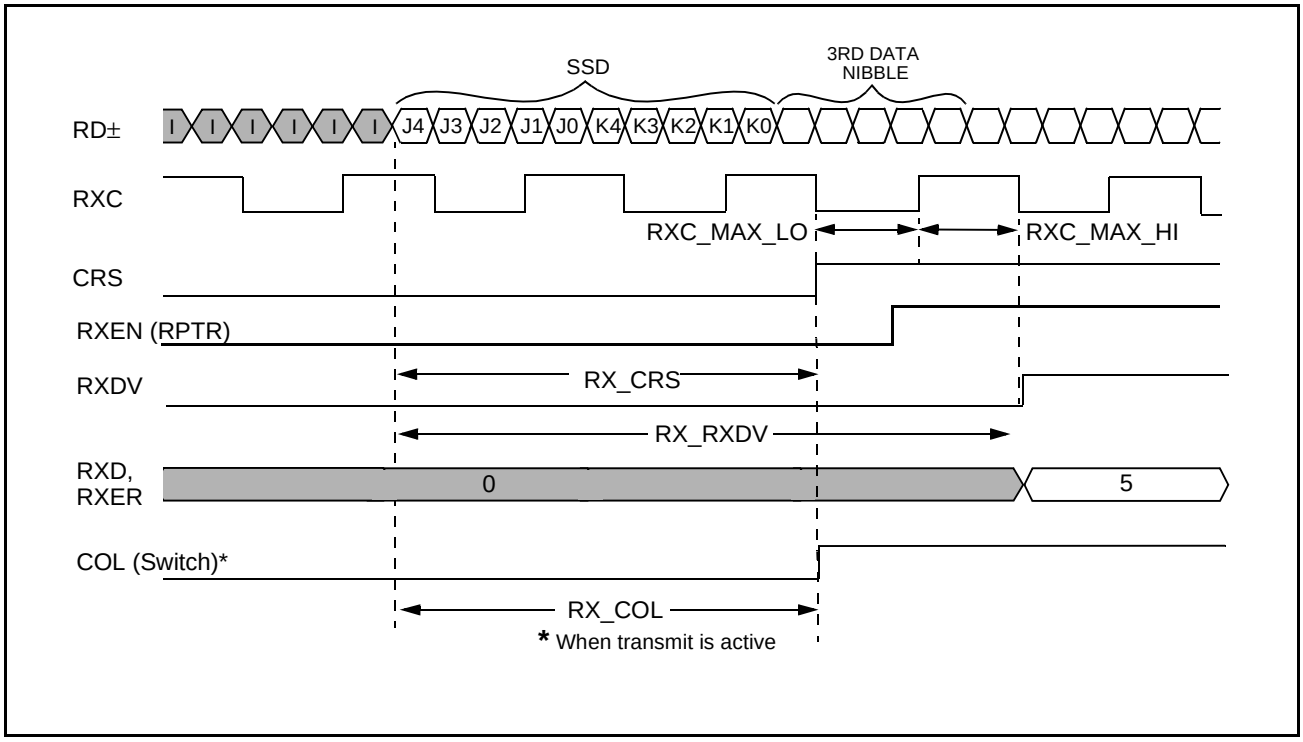


Figure 7: Receive End of Packet Timing (100BASE-TX)

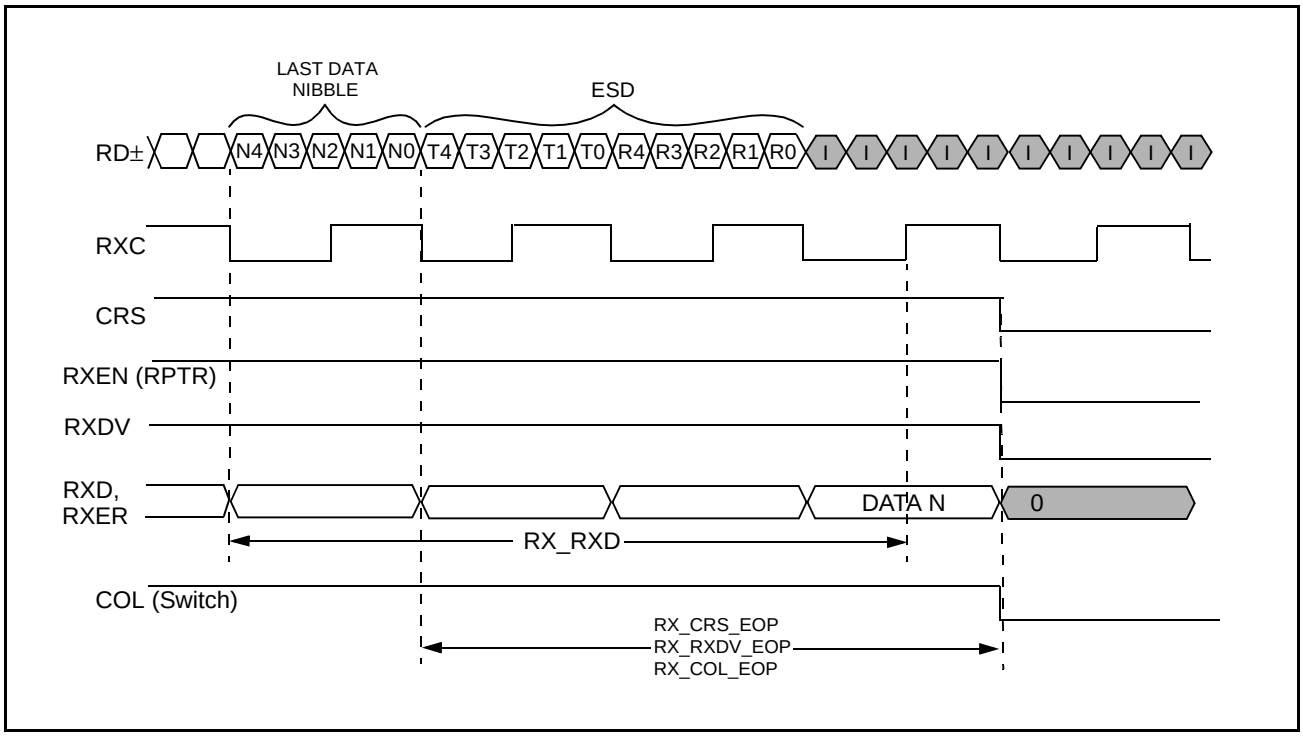


Figure 8: Receive Packet Premature End (100BASE-TX)

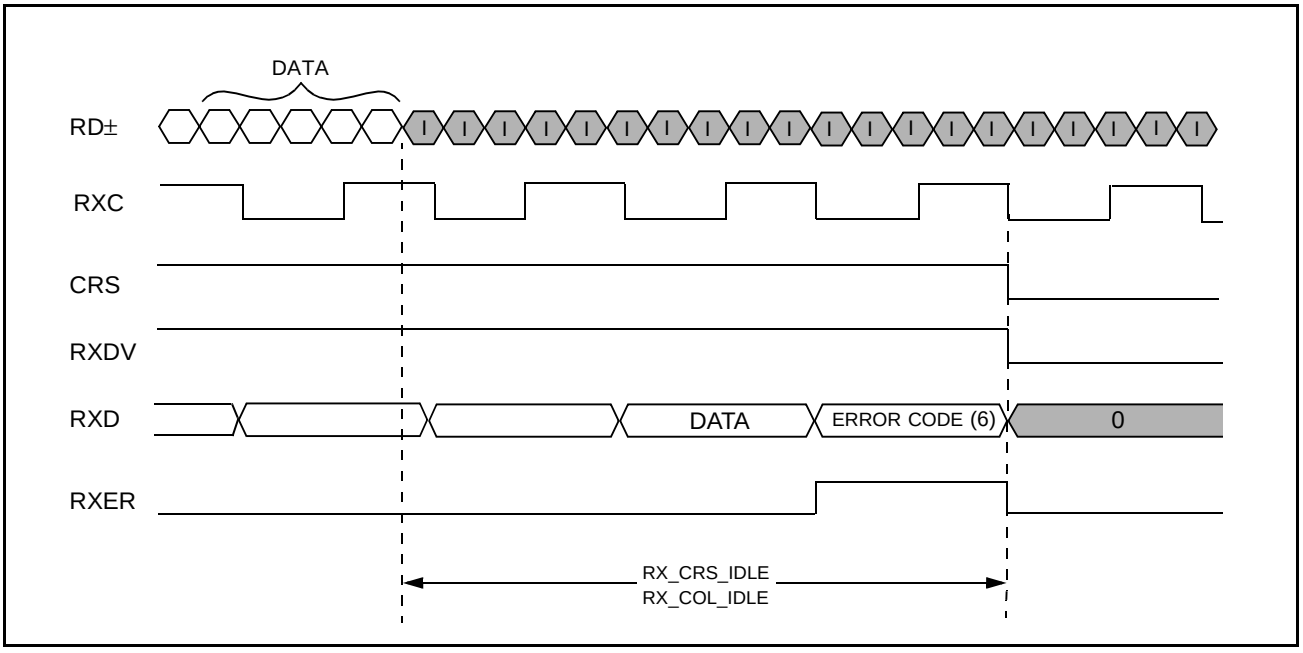


Figure 9: Link Failure or Stream Cipher Error During Receive Packet

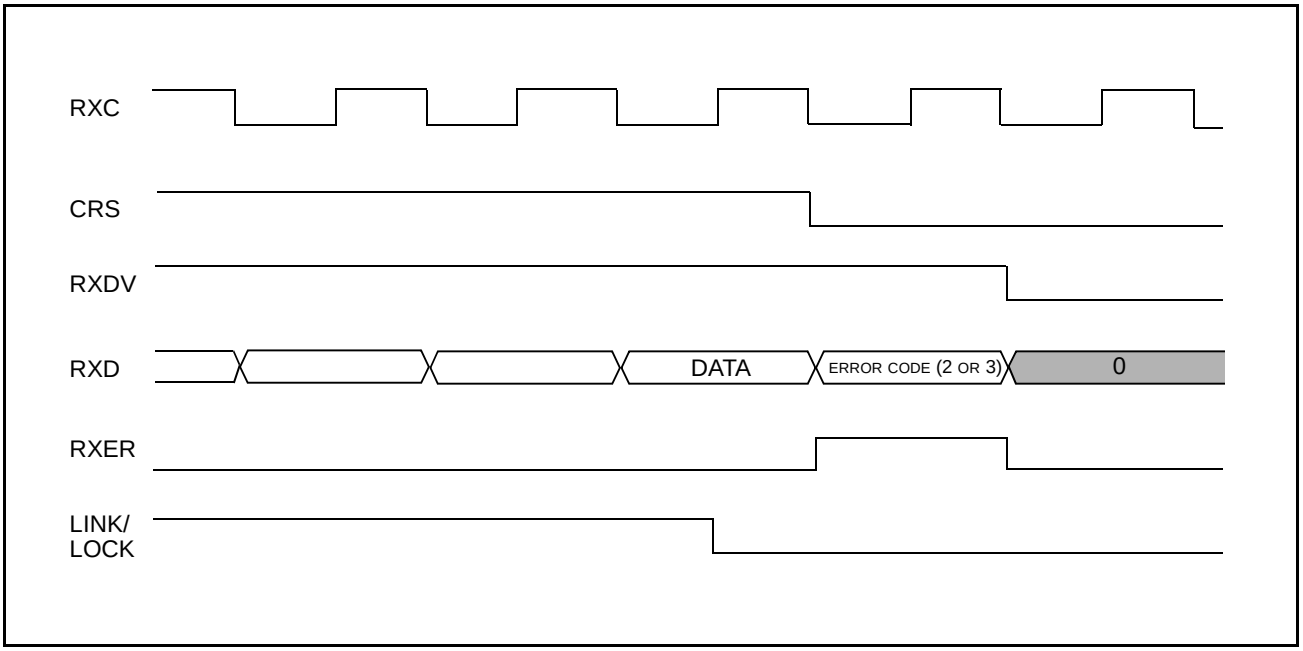


Figure 10: False Carrier Sense Timing (100BASE-TX)

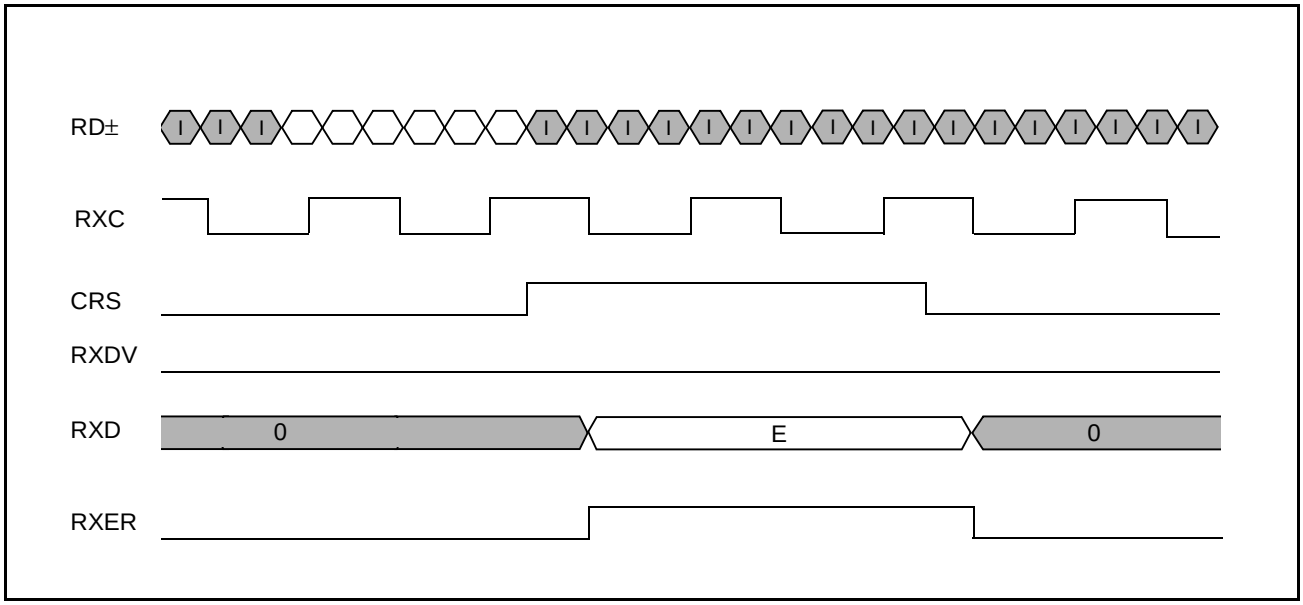


Table 32 provides the parameters for 10BASE-T receive timing. 10BASE-T collision timing parameters are shown in Table 33.

Table 32: 10BASE-T Receive Timing

PARAMETER	*SYMBOL*	*MIN*	*TYP*	*MAX*	*UNIT*
RXC Cycle Time	RXC_CYCLE	370.0	400	430.0	ns
RXC High/Low Time		150.5	200	240.5	ns
CRS Assert after First Rising Edge of Preamble with Positive Start-of-Idle	RX_CRS_BT	100	150	250	ns
CRS Assert after First Falling Edge of Preamble with Negative Start-of-Idle	RX_CRS_BT	100	150	250	ns
RXC Valid after CRS Assert	RXC_VALID	–	–	2000	ns
RXDV Assert after Receive Analog Data	RX_RXDV	–	1900	2300	ns
RXDV Deassert after Receive Analog EOP ends	RX_NOT_RXDV	–	510	560	ns
CRS Deassert after Receive Analog EOP ends	RX_NOT_CRS	–	510	560	ns
Note: Positive Start of Idle contains four “1” data samples, which implies correct polarity, and Negative Start-of-Idle contains four “0” data samples, which implies reversed polarity. Refer to IEEE 802.3, Clause 14, Figure 14-10.					

Table 33: 10BASE-T Collision Timing

PARAMETER	*SYMBOL*	*MIN*	*TYP*	*MAX*	*UNIT*
COL Assert after First Rising Edge of Preamble wit h positive Start-of-Idle	RX_COL	–	250	300	ns
COL Assert after First Falling Edge of Preamble with negative Start-of-Idle	RX_COL	–	250	300	ns
COL Deassert after TXEN Deassert (while receiving)	TXEN_NOT_COL	–	440	490	ns
COL Assert after TXEN Assert (while receiving)	TXEN_COL	–	50	100	ns
COL Deassert after Receive Analog ends (while transmitting)	RX_NOT_COL	–	400	450	ns

Table 34, Table 35, Table 36 and Table 37 provide the parameters for loopback timing, auto-negotiation, and LED timing. Figure 11 illustrates serial mode LED timing.

Table 34: Loopback Timing

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
TXD to RXD Steady State Propagation Delay		–	160	–	ns
LPBK Setup Time to TXEN		500	–	–	ns
LPBK Hold Time from TXEN		200	–	–	ns

Table 35: Auto-Negotiation Timing

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Link Test Pulse Width		–	100	–	ns
FLP Burst Interval		5.7	16	22.3	ms
Clock Pulse to Clock Pulse		111	123	139	us
Clock Pulse to Data Pulse (Data = 1)		55.5	62.5	69.5	us

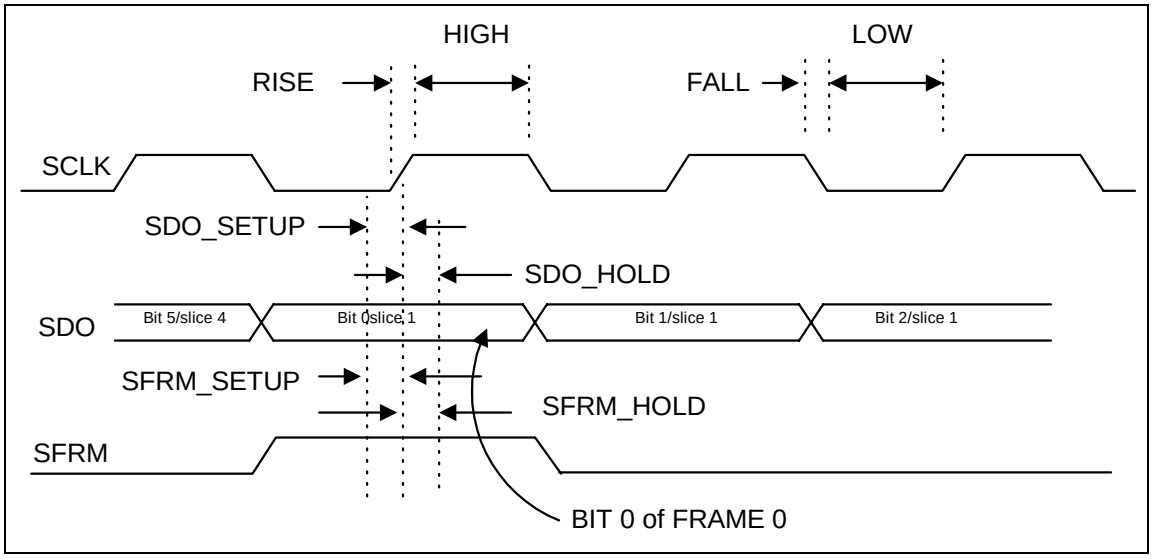
Table 36: LED Timing (Parallel Mode)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
LED On Time (XMTLED, RCVLED)		–	80	–	ms
LED Off Time (XMTLED, RCVLED)		–	80	–	ms

Table 37: LED Timing (Serial Mode)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Shift Clock	SCLK		1		MHz
LED Serial Mode Data Set-up	SDO_SETUP		200		ns
LED Serial Mode Data Hold	SDO_HOLD		200		ns
LED Frame Pulse Set-up	SFRM_SETUP		200		ns
LED Frame Pulse Hold	SFRM_HOLD		200		ns

Figure 11: LED Timing (Serial Mode)



Management data interface timing parameters are described in Table 38. Figure 12 and Figure 13 illustrate two types of management interface timing.

Table 38: Management Data Interface Timing

PARAMETER	*SYMBOL*	*MIN*	*TYP*	*MAX*	*UNIT*
MDC Cycle Time		80	-	-	ns
MDC High/Low		30	-	-	ns
MDC Rise/Fall Time		-	-	10	ns
MDIO Input Setup Time from MDC rising		10	-	-	ns
MDIO Input Hold Time from MDC rising		10	-	-	ns
MDIO Output Delay from MDC rising		0	-	50	ns

Figure 12: Management Interface Timing

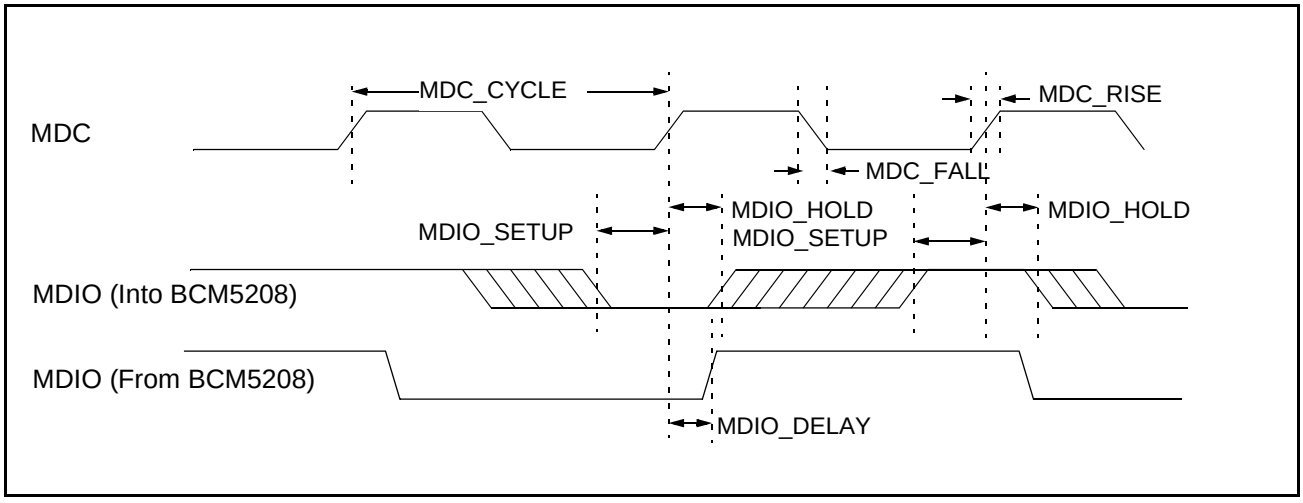


Figure 13: Management Interface Timing (with Preamble Suppression On)

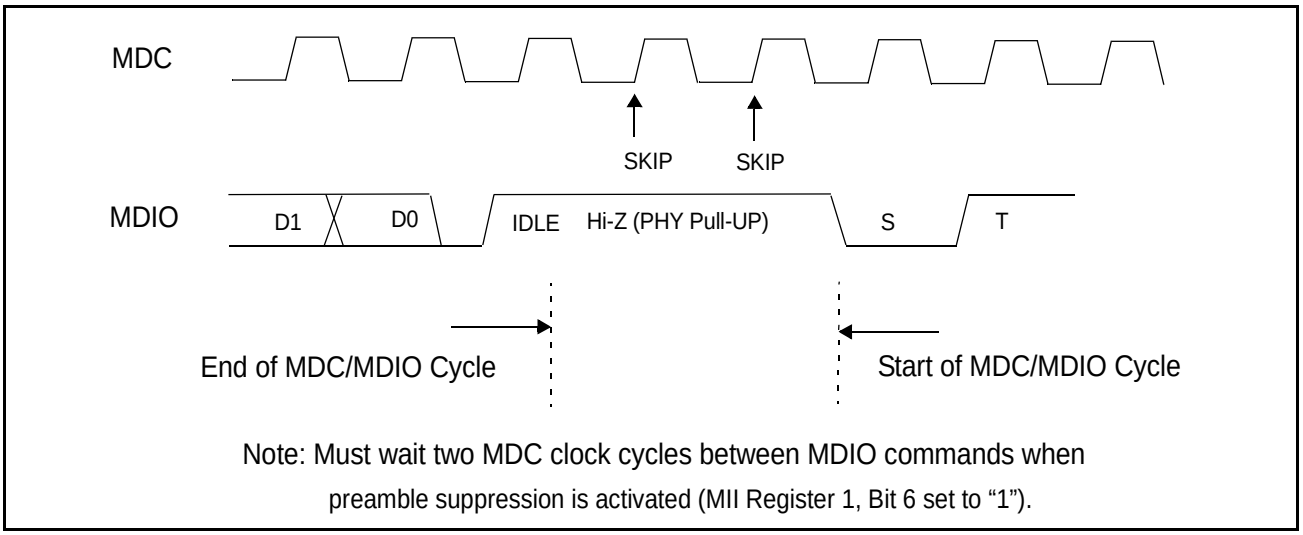


Table 39 and Figure 14 describe and illustrate 10BASE-T serial repeater mode receiver timing.

Table 39: 10BASE-T Serial Repeater Mode Receiver Timing

PARAMETER	*SYMBOL*	*MIN*	*TYP*	*MAX*	*UNIT*
RX+/- to CRS Assert	RX_CRS_BT	100	150	250	ns
CRS Assert to RXDV Assert	RX_RXDV		1800	1900	ns
CRS De-Assert after Receive Analog Ends	RX_NOT_CRS		400	500	ns
RXDV De-Assert after Receive Analog Ends	RX_NOT_RXDV		400	500	ns

Figure 14: 10BASE-T Serial Repeater Mode Receiver Timing

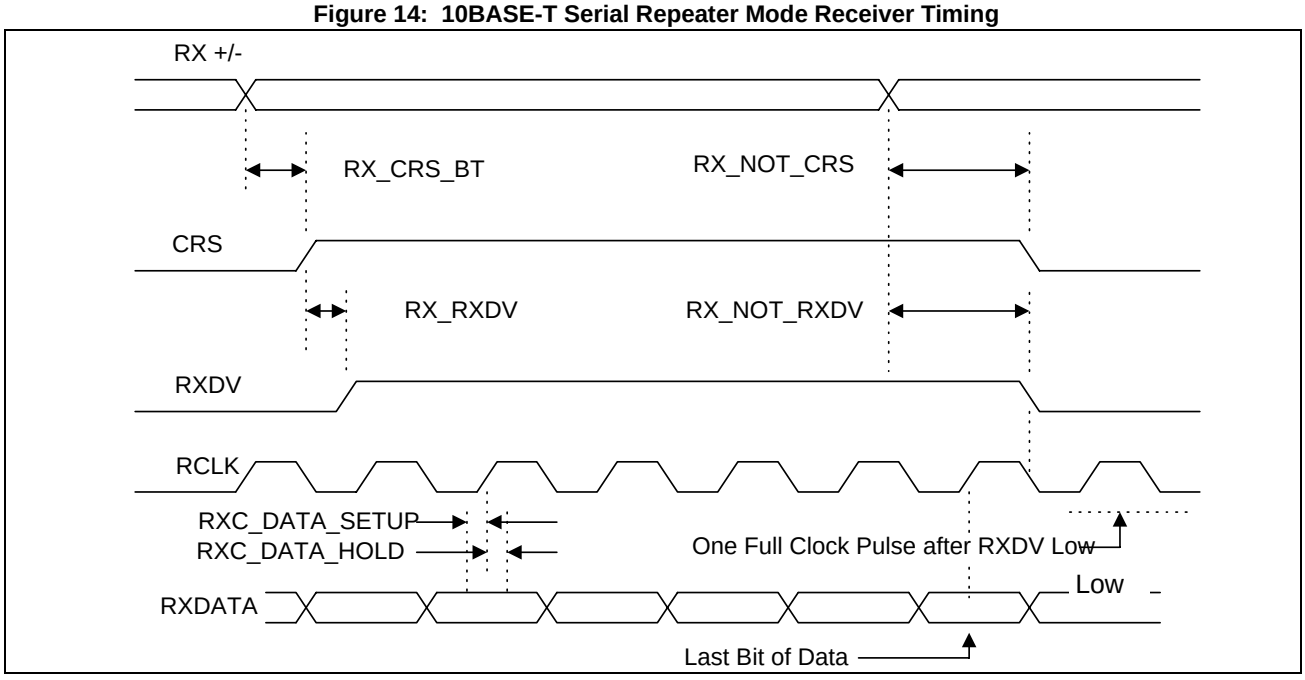
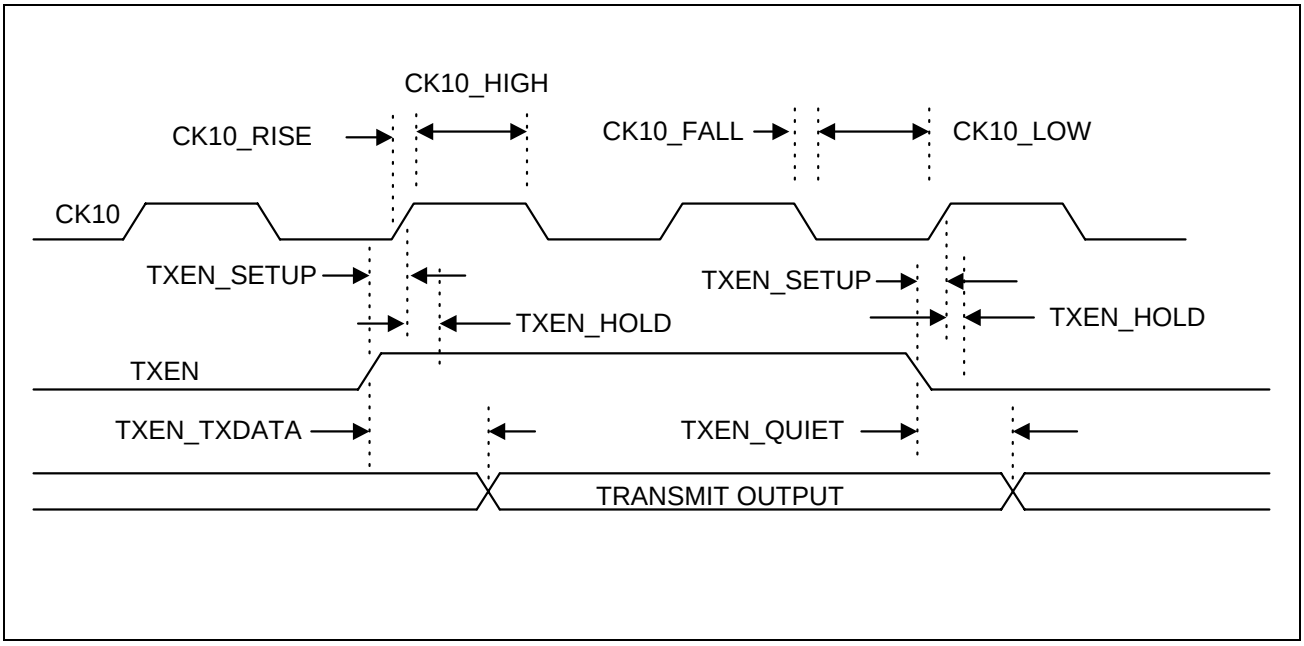


Table 40 and Figure 15 describe and show 10BASE-T serial repeater mode transmit timing.

Table 40: 10BASE-T Serial Repeater Mode Transmit Timing

PARAMETER	*SYMBOL*	*MIN*	*TYP*	*MAX*	*UNIT*
CK10 Cycle Time	CK10	95	100	105	ns
CK10 Low Time CK10 High Time	CK10_LO CK10-HIGH	97.5		102.5	ns
CK10 Rise Time CK10 Fall Time	CK10_RISE CK10_FALL	2		5	ns
TXEN to Rising Clock Setup Time	TXEN_SETUP	12			ns
TXEN Hold after rising Clock	TXEN_HOLD	0			ns
TXEN to Analog Output Start	TXEN_TDATA		400	500	ns
TXEN to Analog Output End	TXEN_QUIET		400	500	ns

Figure 15: 10BASE-T Serial Repeater Mode Transmit Timing



SECTION 7: ELECTRICAL CHARACTERISTICS

This section covers the electrical characteristics of the BCM5208.

Table 41 covers the absolute maximum ratings for the BCM5208. The recommended operating conditions are shown in Table 42. Table 43 gives the electrical characteristics of the BCM5208.

Table 41: Absolute Maximum Ratings

SYMBOL	*PARAMETER*	*MIN*	*MAX*	*UNITS*
V_{DD}	Supply Voltage	GND – 0.3	5.0	V
V_I	Input Voltage	GND – 0.3	IVDD + 0.3	V
I_I	Input Current		±10	mA
T_{STG}	Storage Temperature	–40	+125	°C
V_{ESD}	Electrostatic Discharge		1000	V
Note: These specifications indicate levels where permanent damage to the device may occur. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods may adversely affect long-term reliability of the device.				

Table 42: Recommended Operating Conditions

SYM	*PARAMETER*	*PINS*	*OPERATING MODE*	*MIN*	*MAX*	*UNITS*
V_{DD}	Supply Voltage	AVDD, DVDD, OVDD		3.135	3.465	V
		IVDD		3.135	5.25	V
V_{IH}	High-Level Input Voltage	All Digital Inputs		2.0		V
V_{IL}	Low-Level Input Voltage	All Digital Inputs			0.8	V
		SD± {1:4}	100BASE-TX		0.4	V
V_{IDIFF}	Differential Input Voltage	SD± {1:4}	100BASE-FX	100		mV
V_{ICM}	Common Mode Input Voltage	RD± {1:4}	100BASE-TX	1.55	1.95	V
		RD± {1:4}, SD± {1:4}	100BASE-FX	1.55	1.95	V
T_A	Ambient Operating Temperature			0	70	°C

Table 43: Electrical Characteristics

SYM	PARAMETER	PINS	CONDITIONS	MIN	TYP	MAX	UNITS
I_{DD}	Total Supply Current	AVDD, DVDD, OVDD, IVDD	100BASE-TX		715	780	mA
I_{DD}	Individual PHY Supply Current	AVDD, DVDD, OVDD, IVDD	Auto-Negotiation		150	160	mA
			10BASE-T Idle		110	120	mA
			10BASE-T Active		180[1]	190[1]	mA
			100BASE-TX		190[2]	210[2]	mA
V_{OH}	High-Level Output Voltage	All Digital Outputs	I_{OH} = –15 mA	2.4			V
		TD± {1:4}	driving loaded magnetics module			VDD + 1.5	V
V_{OL}	Low-Level Output Voltage	All Digital Outputs	I_{OL} = 8 mA			0.4	V
		TD± {1:4}	driving loaded magnetics module	VDD – 1.5			V
V_{ODIFF}	Differential Output Voltage	TD± {1:4}	100BASE-FX Mode	400			mV
I_I	Input Current	Digital Inputs w/ Pull-Up Resistors	V_I = IVDD			+100	µA
			V_I = DGND			-200	µA
		Digital Inputs w/ Pull-Down Resistors	V_I = IVDD			+200	µA
			V_I = DGND			-100	µA
		All other Digital Inputs	DGND ≤ V_I ≤ IVDD			±100	µA
I_{OZ}	High-Impedance Output Current	All Three-state Outputs	DGND ≤ V_O ≤ OVDD				µA
		All Open-drain Outputs	V_O = OVDD				µA
V_{BIAS}	Bias Voltage	VREF, RDAC		1.18		1.30	V

Note 1: Of this value, 70 mA flows through the transformer and output stage.
Note 2: Of this value, 40 mA flows through the transformer and output stage.

SECTION 8: APPLICATION EXAMPLES

Figure 16: Switch Application

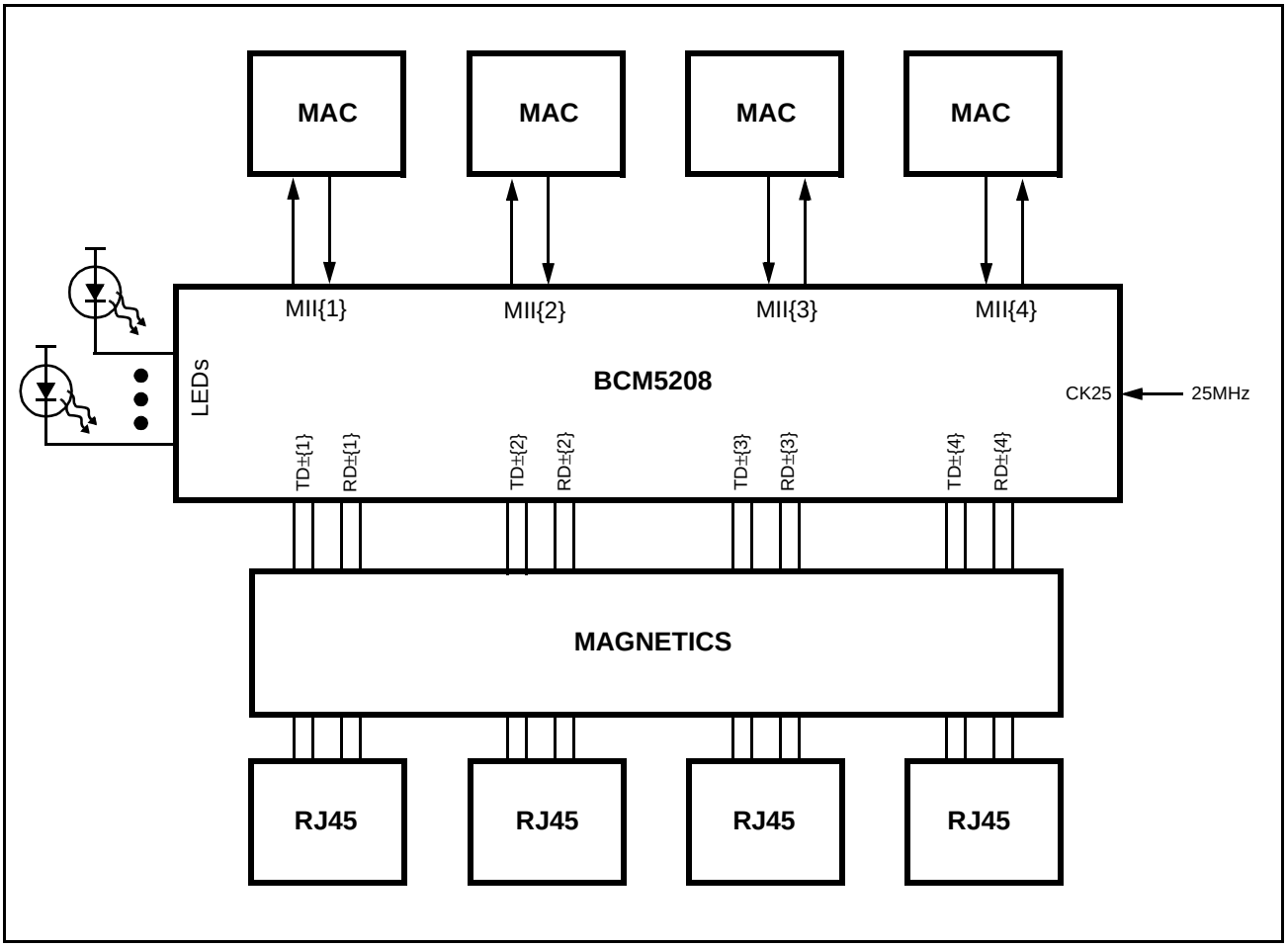
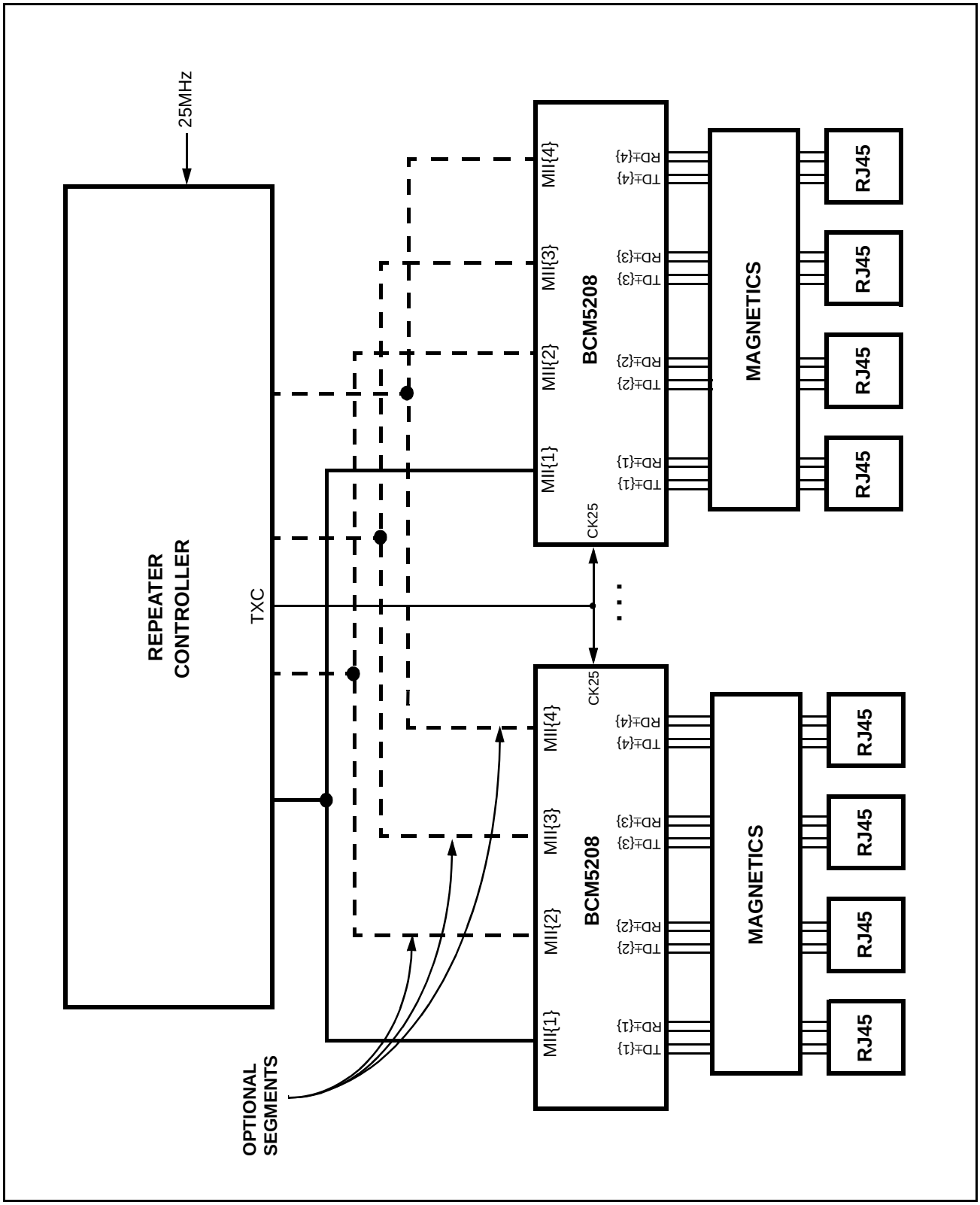
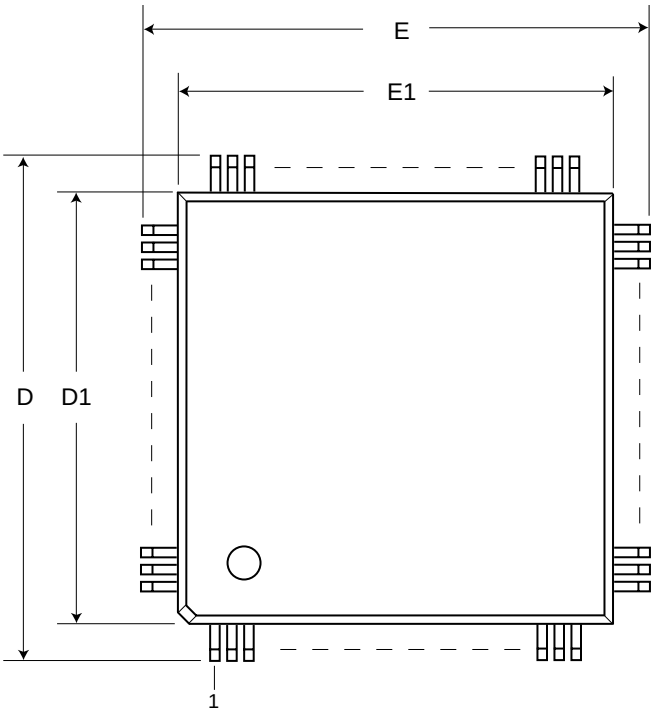


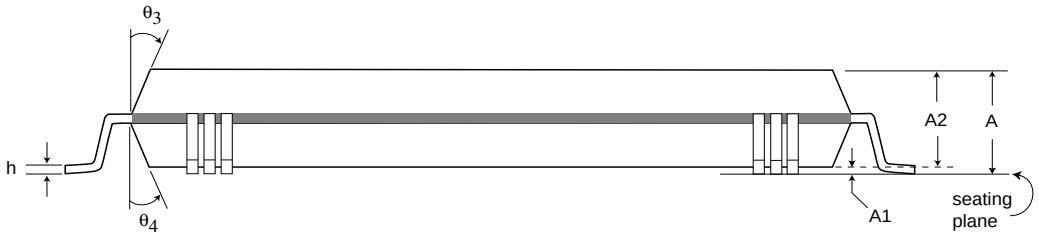
Figure 17: Repeater Application



SECTION 9: MECHANICAL INFORMATION

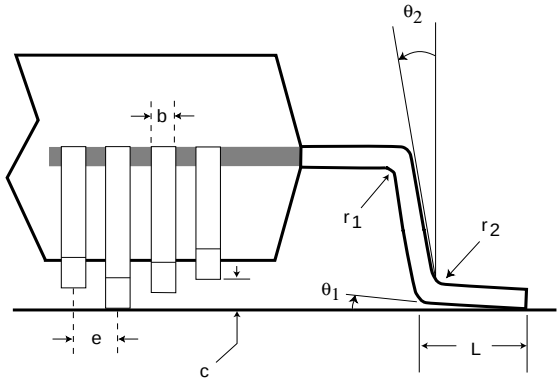
Figure 18: 208-Pin PQFP





Symbol	Millimeter		
	Min	Nom	Max
A	—	—	4.10
A1	0.25	0.37	0.50
A2	3.39	3.49	3.59
D	30.35	30.60	30.85
D1	27.90	28.00	28.10
E	30.35	30.60	30.85
E1	27.90	28.00	28.10
L	0.30	0.60	0.75
b	0.15	0.22	0.30
h	0.13		0.23
e	0.50 BSC		
c	—	0.08	0.102
r_1	—	0.20	—
r_2	—	0.30	—
θ_1	0°	—	7°
θ_2	2°	6°	10°
θ_3	—	10°	—
θ_4	—	10°	—

208-pin detail



Notes:

1. Drawings on this page are not to scale
2. All dimensions are in millimeters except where noted
3. Foot length "L" is measured at gage plane, 0.25mm above the seating plane
4. Seating plane is defined by three lowest lead tips

SECTION 10: ORDERING INFORMATION

Table 44: Ordering Information

PART NUMBER	*PACKAGE*	*AMBIENT TEMPERATURE*
BCM5208 KPF	208-PQFP	0° to 70° C (32° to 158° F)

Broadcom Corporation

16215 Alton Parkway
P.O. Box 57013
Irvine, California 92619-7013
Phone: 949-450-8700
Fax: 949-450-8710