

# CD40106B Types

# **CMOS Hex Schmitt Triggers**

High-Voltage Types (20-Volt Rating)

CD40106B consists of six Schmitttrigger circuits. Each circuit functions as an inverter with Schmitt-trigger action on the input. The trigger switches at different points for positive- and negative-going signals. The difference between the positive-going voltage (VP) and the negative-going voltage (VN) is defined ashysteresis voltage (VH) (see Fig.6). The CD40106B types are supplied in 14-lead hermetic dual-in-line ceramic packages (F3A suffix), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline packages (M, MT, M96, and NSR suffixes), and 14-lead thin shrink small-outline packages (PW and PWR suffixes).

#### Features:

- Schmitt-trigger action with no external components Hysteresis voltage (typ.) 0.9 V at VDD = 5 V, 2.3 V at
- VDD = 10 V, and 3.5 V at VDD = 15 V
- Noise immunity greater than 50%
- No limit on input rise and fall times
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 µA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Low VDD to VSS current during slow
- input ramp
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

- High-noise-environment systems

#### MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V <sub>DD</sub> )
Voltages referenced to V <sub>SS</sub> Terminal)
INPUT VOLTAGE RANGE, ALL INPUTS
DC INPUT CURRENT, ANY ONE INPUT
POWER DISSIPATION PER PACKAGE (PD):
For $T_A = -55^{\circ}C$ to $+100^{\circ}C$
For T <sub>A</sub> = +100°C to +125°C Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T <sub>A</sub> = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)
OPERATING-TEMPERATURE RANGE (T <sub>A</sub> )
STORAGE TEMPERATURE RANGE (T <sub>stg</sub> )65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max +265°C

#### **RECOMMENDED OPERATING CONDITIONS**

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

	LIN	UNITS	
CHARACTERISTIC	MIN.	MAX.	UNITS
Supply-Voltage Range (For TA Full Package-Temperature Range)	3	18	v

#### DYNAMIC ELECTRICAL CHARACTERISTICS

At  $T_A = 25^{\circ}C$ , Input  $t_r$ ,  $t_f = 20 \text{ ns}$ ,  $C_L = 50 \text{ pF}$ ,  $R_L = 200 \text{ k}\Omega$ 

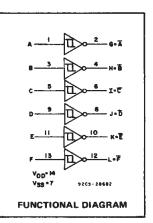
	TEST COND	ITIONS	LIN	LIMITS			
CHARACTERISTIC	VDD (V)		TYP.	MAX.	UNITS		
Propagation Delay Time:		5	140	280			
tPHL,		10	70	140	ns		
tPLH		15	60	120			
Transition Time:		5	100	200			
tTHL.		10	50	100	ns		
<b>TLH</b>		15	40	80			
Input Capacitance, CIN	Any Input		5	7.5	pF		

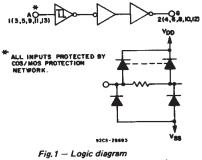




#### Applications:

- Wave and pulse shapers
- **Monostable multivibrators**
- Astable multivibrators





(1 of 6 Schmitt triggers).

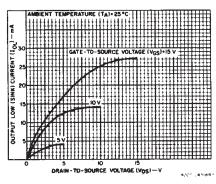
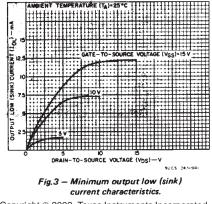
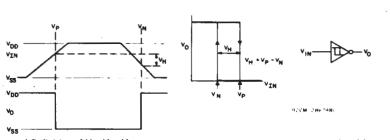


Fig.2 - Typical output low (sink) current characteristics.

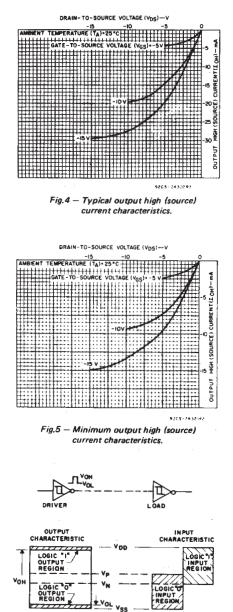


#### STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	Vo		VDD						+25	(~C)	UNITS	
	(V)	(V)	(V)	-55	-40	+85	+125	Min.	Typ.	Mex.		
0 ·	-	0,5	5	1	1	30	30		0.02	1	<u> </u>	
Quiescent Device Current, IDD	-	0,10	10	2	2	60	60	-	0.02	2	1.	
Max.	-	0,15	15	4	4	120	120	-	0.02	4	μA	
		0,20	20	20	20	600	600		0.04	20	1	
Positive Trigger	_	-	5	2.2	2.2	2.2	2.2	2.2	2.9	-		
Threshold Voltage	-	-	10	4.6	4.6	4.6	4.6	4.6	5.9	-		
V <sub>p</sub> Min.	-	-	15	6.8	6.8	6.8	6.8	6.8	8.8		1	
	-	-	5	3.6	3.6	3.6	3.6	-	2.9	3.6	V	
V <sub>D</sub> Max.	-	-	10	7.1	7.1	7.1	7.1	-	5.9	7.1	1	
F	-	-	15	10.8	10.8	10.8	10.8	-	8.8	.10,8	1	
Negative Trigger		-	5	0.9	0.9	0.9	0.9	0.9	1.9	-		
Threshold Voltage	_		10	2.5	2.5	2.5	2.5	2.5	3.9	_		
V <sub>N</sub> Min. V <sub>N</sub> Max.	-		15	4	4	4	4	4	5.8	-		
		_	5	2.8	2.8	2.8	2.8		1.9	2.8	• •	
	-		10	5.2	5.2	5.2	5.2		3.9	5.2	1	
	-	-	15	7.4	7.4	7.4	7.4		5.8	7.4		
Hysteresis Voltage V <sub>H</sub> Min.	· · ·	-	5	0.3	0.3	0.3	0.3	0.3	0.9	-		
	-	-	10	1.2	1.2	1.2	1.2	1.2	2.3	-	1	
	_	-	15	1.6	1.6	1.6	1.6	1.6	3.5	-		
		_	5	1.6	1.6	1.6	1.6	-	0.9	1.6	v	
V <sub>H</sub> Max.	-	-	10	3.4	3.4	3.4	3.4	_	2.3	3.4	1	
	-	-	15	5	5	5	5	-	3.5	5	1	
Output Low (Sink)	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	_		
Current,	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	-		
IOL Min.	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	-		
Output High	4.6	0,5	5	0.64	-0.61	-0.42	-0.36	-0.51	-1		mA	
(Source)	2.5	0.5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	-		
Current, IOH Min.	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	-		
	13.5	0,15	15	-4.2	-4	2.8	-2.4	-3.4	-6.8	-		
Output Voltage	-	5	5		0.	05			0	0.05		
Low-Level,	—	10	10		0.0	05			0	0.05	1	
VOL Max.	-	15	15		0.	05		-	0	0.05		
Output Voltage		0	5		4.	95		4.95	5	_	V	
High Level,	-	0	10		9.	95		9.95	10	-		
VOH Min.		0	15		14	.95		14.95	15	-		
Input Current, IIN Max.		0,18	18	±0.1	±0.1	±1	±1	_	±10-5	±0.1	μA	



a) Definition of Vp, V<sub>N</sub>, V<sub>H</sub> b) Transfer characteristics of 1 of 6 gates Fig.6 - Hysteresis definition, characteristics, and test set-up.

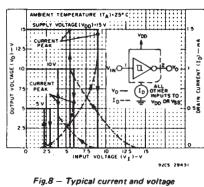


3

COMMERCIAL CMOS HIGH VOLTAGE ICs

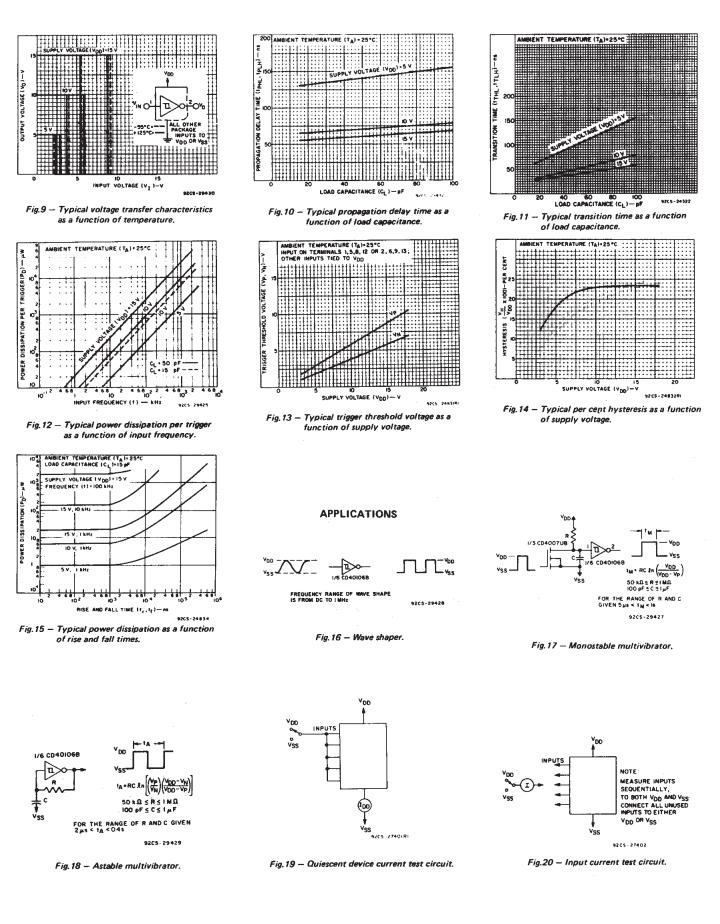
Fig.7 - Input and output characteristics.

9205-28680



transfer characteristics.

#### CD40106B Types



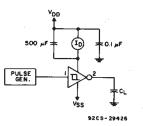
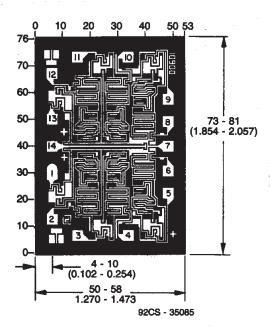


Fig.21 - Dynamic power dissipation test circuit.

TERMINAL ASSIGNMENT



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).

Dimensions and Pad Layout for CD40106BH

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#### **PACKAGING INFORMATION**

Texas Instruments

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
CD40106BE	ACTIVE	PDIP	Ν	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD40106BEE4	ACTIVE	PDIP	Ν	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD40106BF	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
CD40106BF3A	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
CD40106BK	OBSOLETE	CFP	WR	14		TBD	Call TI	Call TI
CD40106BM	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40106BM96	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40106BM96E4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40106BM96G4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40106BME4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40106BMG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40106BMT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40106BMTE4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40106BMTG4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40106BNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40106BNSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40106BNSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40106BPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40106BPWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40106BPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40106BPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40106BPWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40106BPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows: **ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect. NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design. **PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.



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15-Oct-2009

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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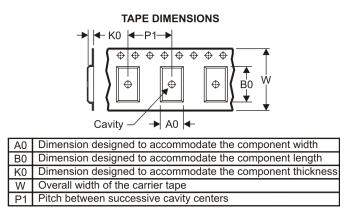
# PACKAGE MATERIALS INFORMATION

www.ti.com

Texas Instruments

#### TAPE AND REEL INFORMATION





#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



All dimensions are nominal <b>Device</b>	1	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD40106BM96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD40106BMT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD40106BNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD40106BPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TEXAS INSTRUMENTS

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# PACKAGE MATERIALS INFORMATION

6-Aug-2010



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD40106BM96	SOIC	D	14	2500	346.0	346.0	33.0
CD40106BMT	SOIC	D	14	250	346.0	346.0	33.0
CD40106BNSR	SO	NS	14	2000	346.0	346.0	33.0
CD40106BPWR	TSSOP	PW	14	2000	346.0	346.0	29.0

J (R-GDIP-T\*\*) 14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

# N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



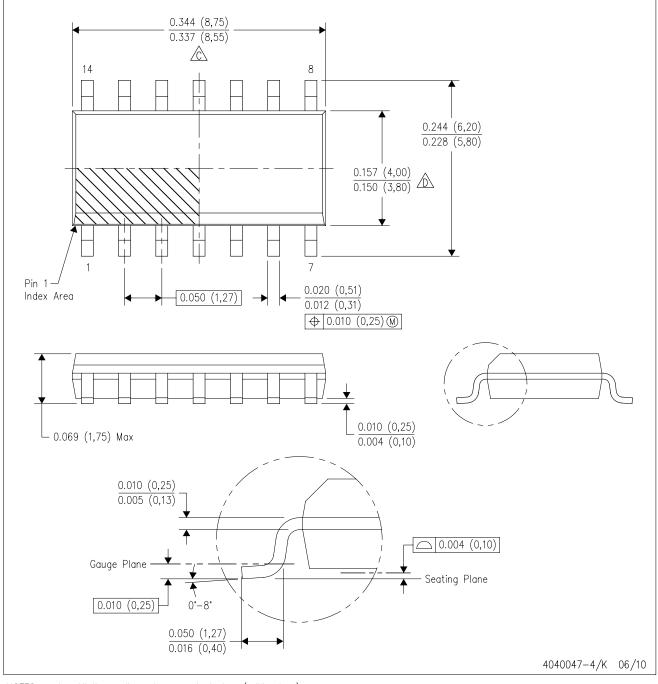
NOTES:

- A. All linear dimensions are in inches (millimeters).B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- $\triangle$  The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDSO-G14)

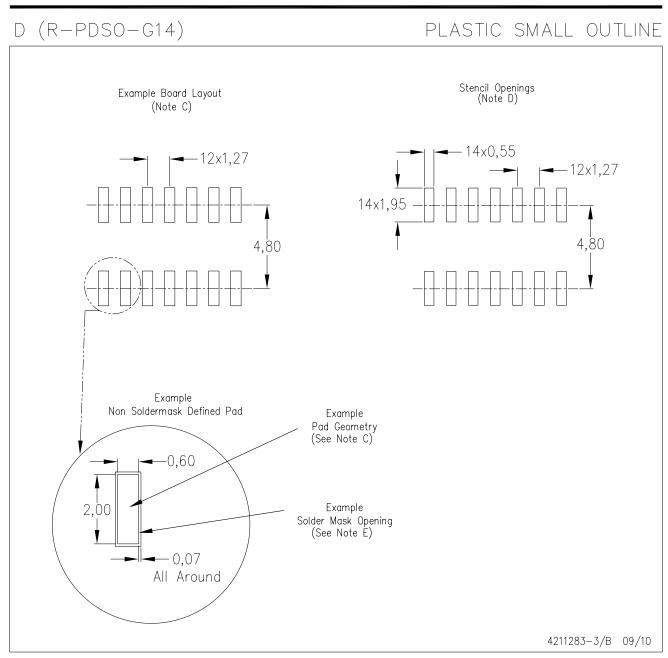
PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS-012 variation AB.





NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



### MECHANICAL DATA

#### PLASTIC SMALL-OUTLINE PACKAGE

#### 0,51 0,35 ⊕0,25⊛ 1,27 8 14 0,15 NOM 5,60 8,20 5,00 7,40 $\bigcirc$ Gage Plane ₽ 0,25 7 1 1,05 0,55 0°-10° Δ 0,15 0,05 Seating Plane — 2,00 MAX 0,10PINS \*\* 14 16 20 24 DIM 10,50 10,50 12,90 15,30 A MAX A MIN 9,90 9,90 12,30 14,70 4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.

NS (R-PDSO-G\*\*)

**14-PINS SHOWN** 

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



## **MECHANICAL DATA**

MTSS001C - JANUARY 1995 - REVISED FEBRUARY 1999

# PW (R-PDSO-G\*\*)

#### PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN

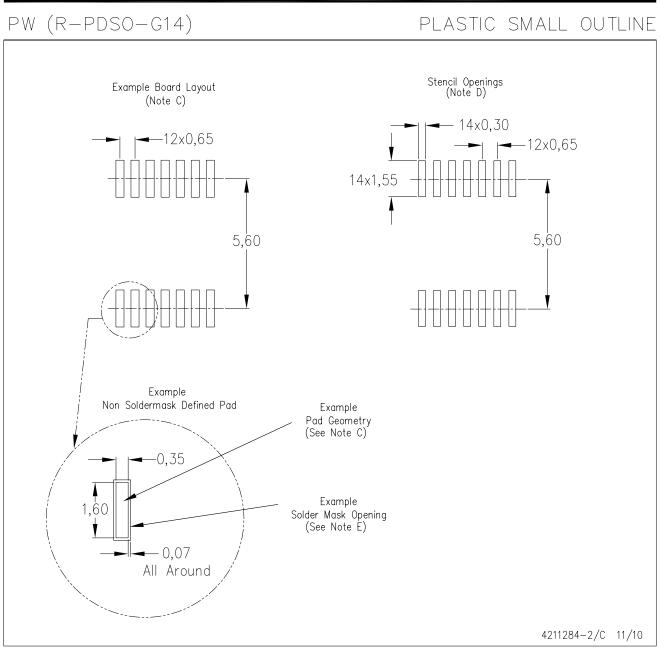


NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153



# LAND PATTERN DATA



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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