

LOW PHASE-NOISE TWO-CHANNEL CLOCK FAN-OUT BUFFER

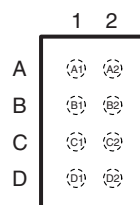
Check for Samples: [CDC3RL02](#)

FEATURES

- **Low Additive Noise:**
 - **-149 dBc/Hz at 10-kHz Offset Phase Noise**
 - **0.37-ps (RMS) Output Jitter**
- **Limited Output Slew Rate for EMI Reduction (1- to 5-ns/Rise/Fall Time for 10-pF to 50-pF Loads)**
- **Adaptive Output Stage Controls Reflection**
- **Regulated 1.8-V Externally Available I/O Supply**
- **Ultra-Small 8-bump YFP 0.4-mm Pitch WCSP (0.8 mm × 1.6 mm)**
- **EESD Performance Exceeds JESD 22**
 - **2000-V Human-Body Model (A114-A)**
 - **1000-V Charged-Device Model (JESD22-C101-A Level III)**

APPLICATIONS

- **Cellular Phones**
- **Global Positioning Systems (GPS)**
- **Wireless LAN**
- **FM Radio**
- **WiMAX**
- **W-BT**

**YFP PACKAGE
(TOP VIEW)**

Table 1. YFP PACKAGE TERMINAL ASSIGNMENTS

	1	2
A	V _{BATT}	CLK_OUT1
B	V _{LDO}	CLK_REQ1
C	MCLK_IN	CLK_REQ2
D	GND	CLK_OUT2

DESCRIPTION/ORDERING INFORMATION

The CDC3RL02 is a two-channel clock fan-out buffer. It buffers a single master clock, such as a temperature compensated crystal oscillator (TCXO) to multiple peripherals. The device has two clock request inputs (CLK_REQ1 and CLK_REQ2), each of which enable a single clock output.

The CDC3RL02 accepts square or sine waves at the master clock input (MCLK_IN), eliminating the need for an AC coupling capacitor. The smallest acceptable sine wave is a 0.3-V signal (peak-to-peak). CDC3RL02 has been designed to offer minimal channel-to-channel skew, additive output jitter, and additive phase noise. The adaptive clock output buffers offer controlled slew-rate over a wide capacitive loading range which minimizes EMI emissions, maintains signal integrity, and minimizes ringing caused by signal reflections on the clock distribution lines.

The CDC3RL02 has an integrated Low-Drop-Out (LDO) voltage regulator which accepts input voltages from 2.3 V to 5.5 V and outputs 1.8 V, 50 mA. This 1.8V supply is externally available to provide regulated power to peripheral devices such as a TCXO.

The CDC3RL02 is ideal for use in portable end-equipment, such as mobile phones, that require clock buffering with minimal additive phase noise and fan-out capabilities. It is offered in a 0.4-mm pitch wafer-level chip-scale (WCSP) package (0.8 mm × 1.6 mm) and is optimized for very low standby current consumption.



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ORDERING INFORMATION

T _A	PACKAGE ^{(1) (2)}		ORDERABLE PART NUMBER	TOP-SIDE MARKING ⁽³⁾
-40°C to 85°C	NanoStar™ WCSP – YFP	Tape and reel	CDC3RL02YFPR	__ _ 4 L _

- (1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
- (2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
- (3) YFP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the wafer fab/assembly site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, ● = Pb-free).

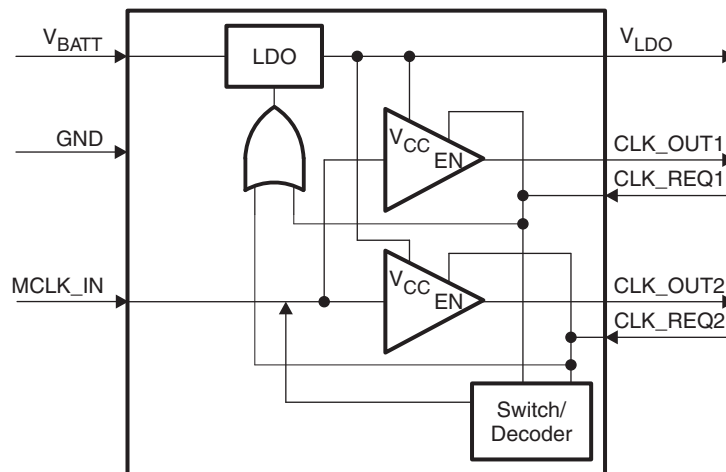
TERMINAL FUNCTIONS

NO.	NAME	I/O	DESCRIPTION
A1	V _{BATT}	I	Input to internal LDO
A2	CLK_OUT1	O	Clock output 1
B1	V _{LDO}	O	1.8 V I/O supply for CDC3RL02 and external TCXO
B2	CLK_REQ1	I	Clock request from peripheral 2
C1	MCLK_IN	I	Master clock input
C2	CLK_REQ2	I	Clock request from peripheral 1
D1	GND	–	Ground
D2	CLK_OUT2	O	Clock output 2

Table 2. FUNCTION TABLE

INPUTS			OUTPUTS	
CLK_REQ1	CLK_REQ2	MCLK_IN	CLK_OUT1	CLK_OUT2
L	L	X	L	L
L	H	CLK	L	CLK
H	L	CLK	CLK	L
H	H	CLK	CLK	CLK

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT	
V_{BATT} voltage range ⁽²⁾		-0.3	7	V	
Voltage range ⁽³⁾	CLK_REQ_1/2, MCLK_IN	-0.3	$V_{BATT} + 0.3$	V	
	V_{LDO} , CLK_OUT_1/2 ⁽²⁾	-0.3	$V_{BATT} + 0.3$		
I_{IK}	Input clamp current at V_{BATT} , CLK_REQ_1/2, and MCLK_IN	$V_I < 0$	-50	mA	
I_O	Continuous output current	CLK_OUT1/2	±20	mA	
Continuous current through GND, V_{BATT} , V_{LDO}			±50	mA	
ESD rating	Human-Body Model		2000	V	
	Charged-Device Model		1000		
	Machine Model		200		
T_J	Operating virtual junction temperature		-40	150	°C
T_A	Operating ambient temperature range		-40	85	°C
T_{stg}	Storage temperature range		-55	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) All voltage values are with respect to network ground terminal.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

		MIN	MAX	UNIT	
V_{BATT}	Input voltage	2.3	5.5	V	
V_I	Input voltage	MCLK_IN, CLK_REQ1/2	0	1.89	V
V_O	Output voltage	CLK_OUT1/2	0	1.8	V
V_{IH}	High-level input voltage	CLK_REQ1/2	1.3	1.89	V
V_{IL}	Low-level input voltage	CLK_REQ1/2	0	0.5	V
I_{OH}	High-level output current, DC current	-8		mA	
I_{OL}	Low-level output current, DC current		8	mA	

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LDO						
V _{OUT}	LDO output voltage	I _{OUT} = 50 mA	1.71	1.8	1.89	V
C _{LDO}	External load capacitance		1		10	μF
I _{OUT(SC)}	Short circuit output current	R _L = 0 Ω		100		mA
I _{OUT(PK)}	Peak output current	V _{BATT} = 2.3 V, V _{LDO} = V _{OUT} - 5%			100	mA
PSR	Power supply rejection	V _{BATT} = 2.3V, I _{OUT} = 2 mA,	f _{IN} = 217 Hz and 1 kHz	60		dB
			f _{IN} = 3.25 MHz	40		
t _{su}	LDO startup time	V _{BATT} = 2.3 V, C _{LDO} = 1 μF, CLK_REQ_n to V _{LDO} = 1.71 V		0.2		ms
		V _{BATT} = 5.5 V, C _{LDO} = 10 μF, CLK_REQ_n to V _{LDO} = 1.71 V			1	
Power Consumption						
I _{SB}	Standby current	Device in standby (all V _{CLK_REQ_n} = 0 V)		0.2	1	μA
I _{CCS}	Static current consumption	Device active but not switching		0.4	1	mA
I _{OB}	Output buffer average current	f _{IN} = 26 MHz, C _{LOAD} = 50 pF		4.2		mA
C _{PD}	Output power dissipation capacitance	f _{IN} = 26 MHz			44	pF
MCLK_IN Input						
I _l	MCLK_IN, CLK_REQ_1/2 leakage current	V _l = V _{LDO} or GND			1	μA
C _I	MCLK_IN capacitance	f _{IN} = 26 MHz		4.75		pF
R _I	MCLK_IN impedance	f _{IN} = 26 MHz		6		kΩ
f _{IN}	MCLK_IN frequency range		10	26	52	MHz
MCLK_IN LVCMOS Source						
	Additive phase noise	f _{IN} = 26 MHz, t _r /t _f ≤ 1 ns	1-kHz offset	-140		dBc/Hz
			10-kHz offset	-149		
			100-kHz offset	-153		
			1-MHz offset	-148		
	Additive jitter	f _{IN} = 26 MHz, V _{PP} = 0.8 V, BW = 10–5 MHz		0.37		ps (rms)
t _{DL}	MCLK_IN to CLK_OUT_n propagation delay			11		ns
DC _L	Output duty cycle	f _{IN} = 26 MHz, DC _{IN} = 50%	45	50	55	%

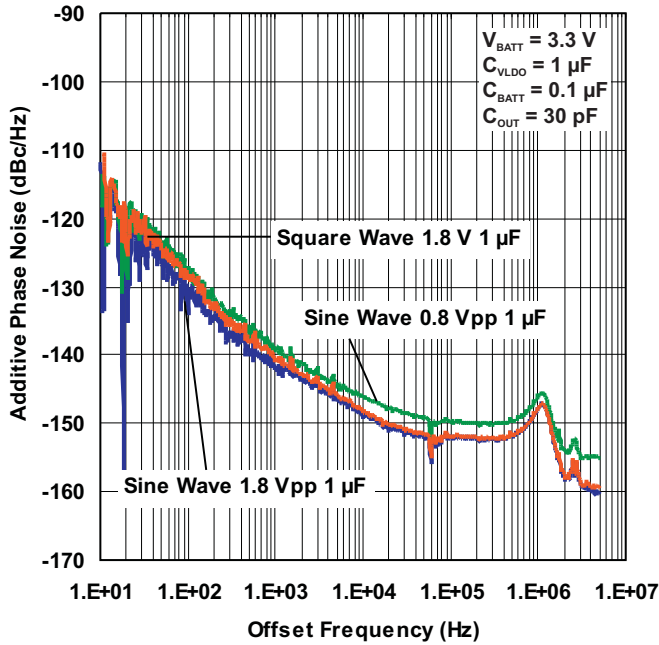
ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

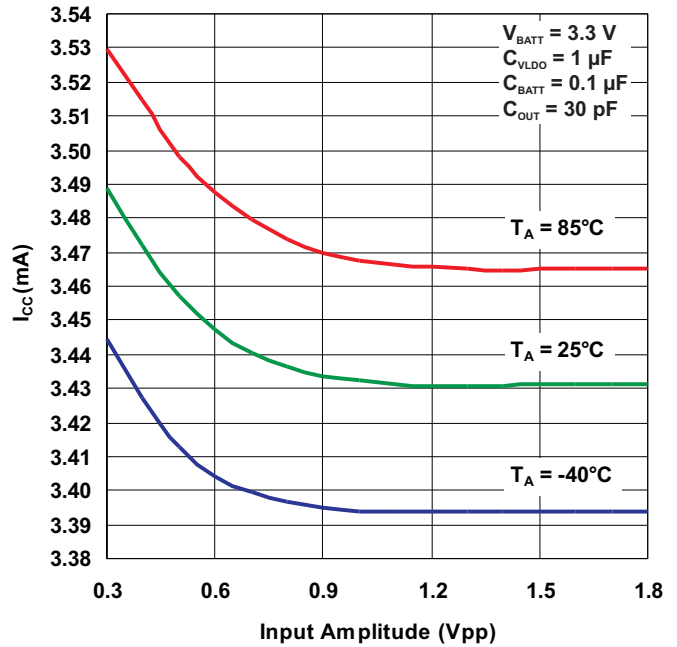
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
MCLK_IN Sinusoidal Source						
V_{MA}	Input amplitude		0.3		1.8	V
Additive phase noise	$f_{IN} = 26 \text{ MHz}, V_{MA} = 1.8 V_{PP}$	1-kHz offset		-141		dBc/Hz
		10-kHz offset		-149		
		100-kHz offset		-152		
		1-MHz offset		-148		
	$f_{IN} = 26 \text{ MHz}, V_{MA} = 0.8 V_{PP}$	1-kHz offset		-139		
		10-kHz offset		-146		
		100-kHz offset		-150		
		1-MHz offset		-146		
Additive jitter	$f_{IN} = 26 \text{ MHz}, V_{MA} = 1.8 V_{PP}, BW = 10\text{--}5 \text{ MHz}$		0.41		ps (RMS)	
t_{DS}	MCLK_IN to CLK_OUT_1/2 propagation delay		12		ns	
DC_s	Output duty cycle	$f_{IN} = 26 \text{ MHz}, V_{MA} > 1.8 V_{PP}$	45	50	55	%
CLK_OUT_N Outputs						
t_r	20% to 80% rise time	$C_L = 10 \text{ pF to } 50 \text{ pF}$	1		5.2	ns
t_f	20% to 80% fall time	$C_L = 10 \text{ pF to } 50 \text{ pF}$	1		5.2	ns
t_{sk}	Channel-to-channel skew	$C_L = 10 \text{ pF to } 50 \text{ pF} (C_{L1} = C_{L2})$	-0.5		0.5	ns
V_{OH}	High-level output voltage	$I_{OH} = -100 \mu\text{A}$, reference to V_{LDO}	-0.1			V
		$I_{OH} = -8 \text{ mA}$	1.2			
V_{OL}	Low-level output voltage	$I_{OL} = 20 \mu\text{A}$			0.2	V
		$I_{OL} = 8 \text{ mA}$			0.55	

TYPICAL PERFORMANCE

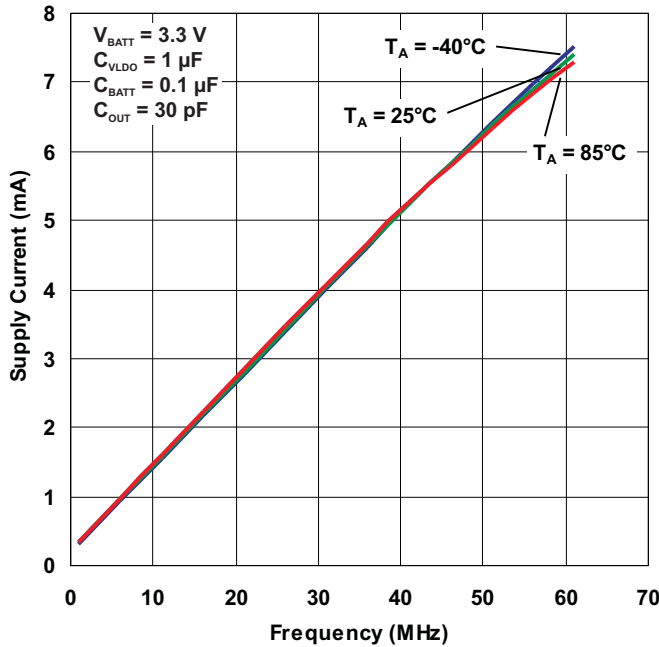
ADDITIVE PHASE NOISE
vs
OFFSET FREQUENCY



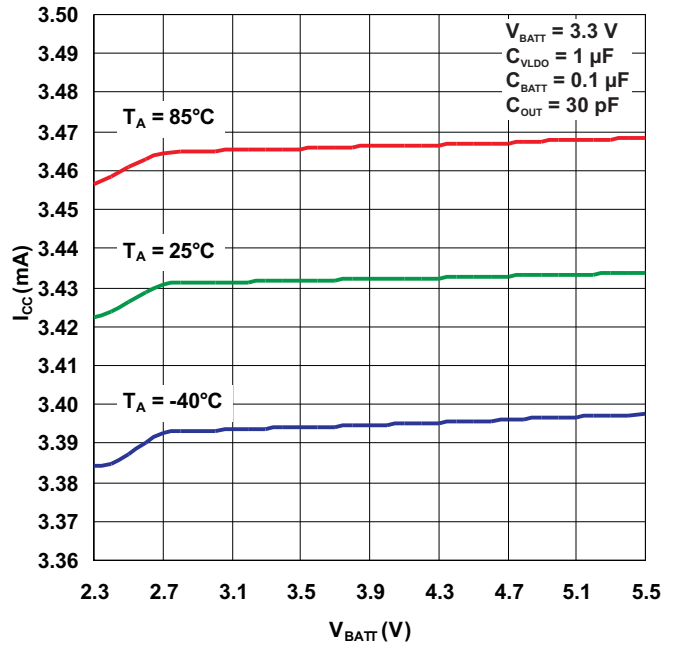
SUPPLY CURRENT
vs
INPUT AMPLITUDE



SUPPLY CURRENT
vs
INPUT FREQUENCY

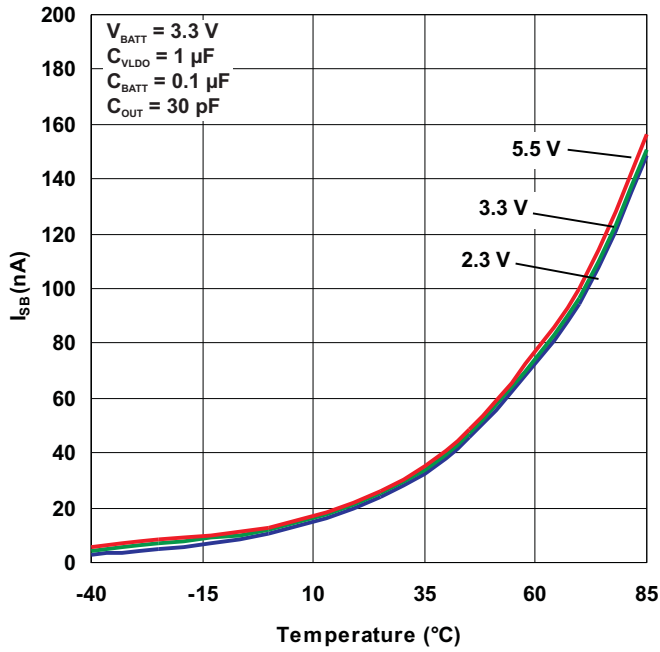


SUPPLY CURRENT
vs
SUPPLY VOLTAGE

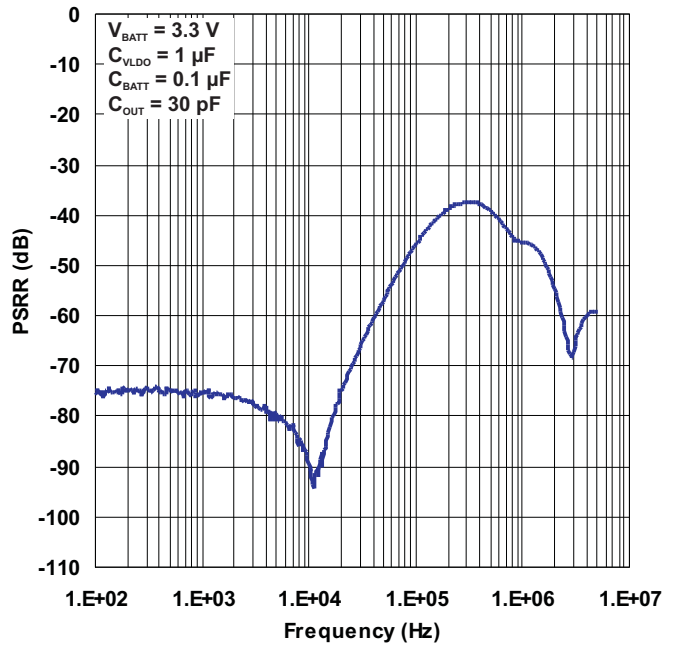


TYPICAL PERFORMANCE (continued)

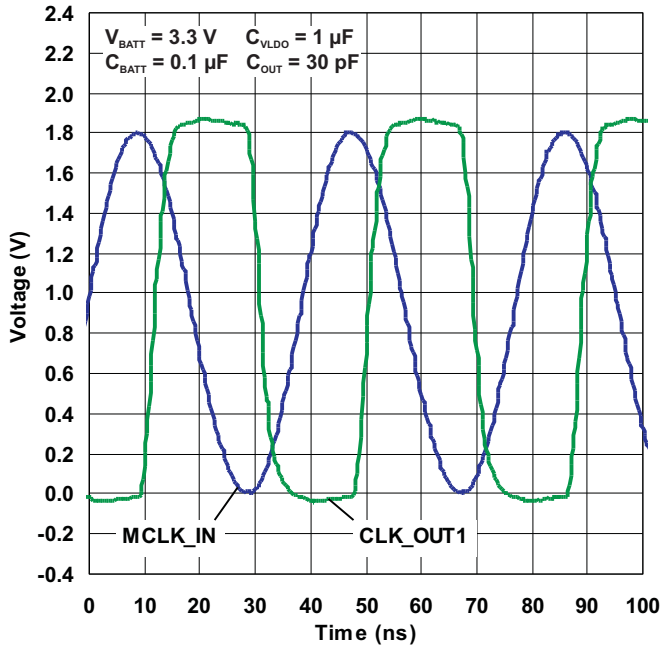
STANDBY CURRENT
VS
TEMPERATURE



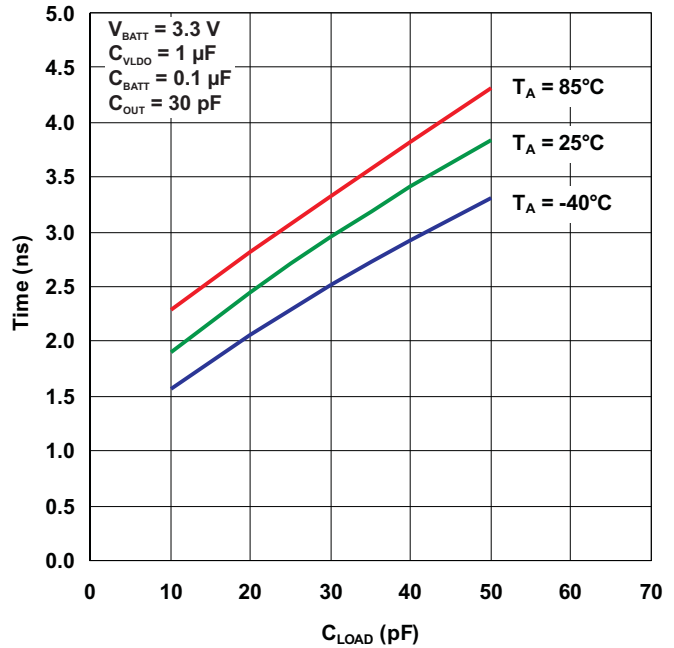
POWER SUPPLY REJECTION
VS
INPUT FREQUENCY



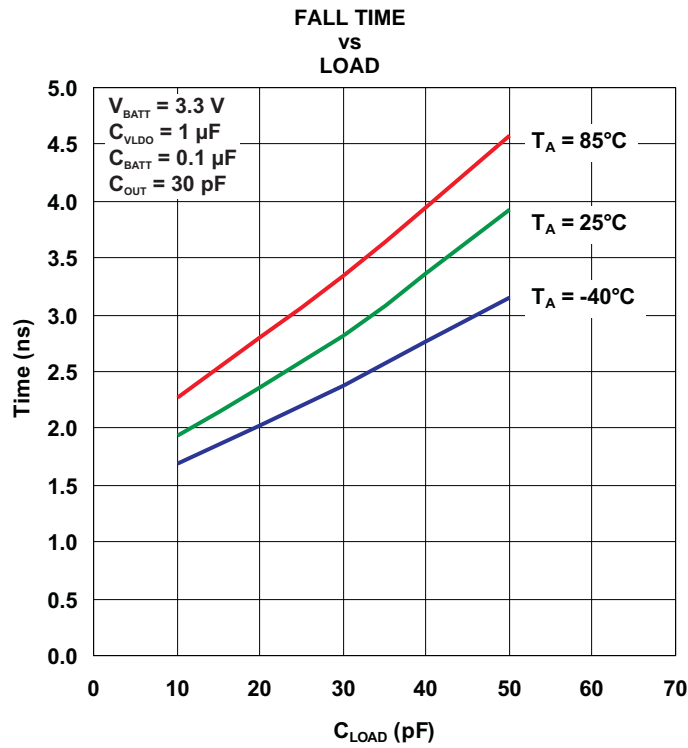
SINE-WAVE INPUT
VS
SQUARE-WAVE OUTPUT



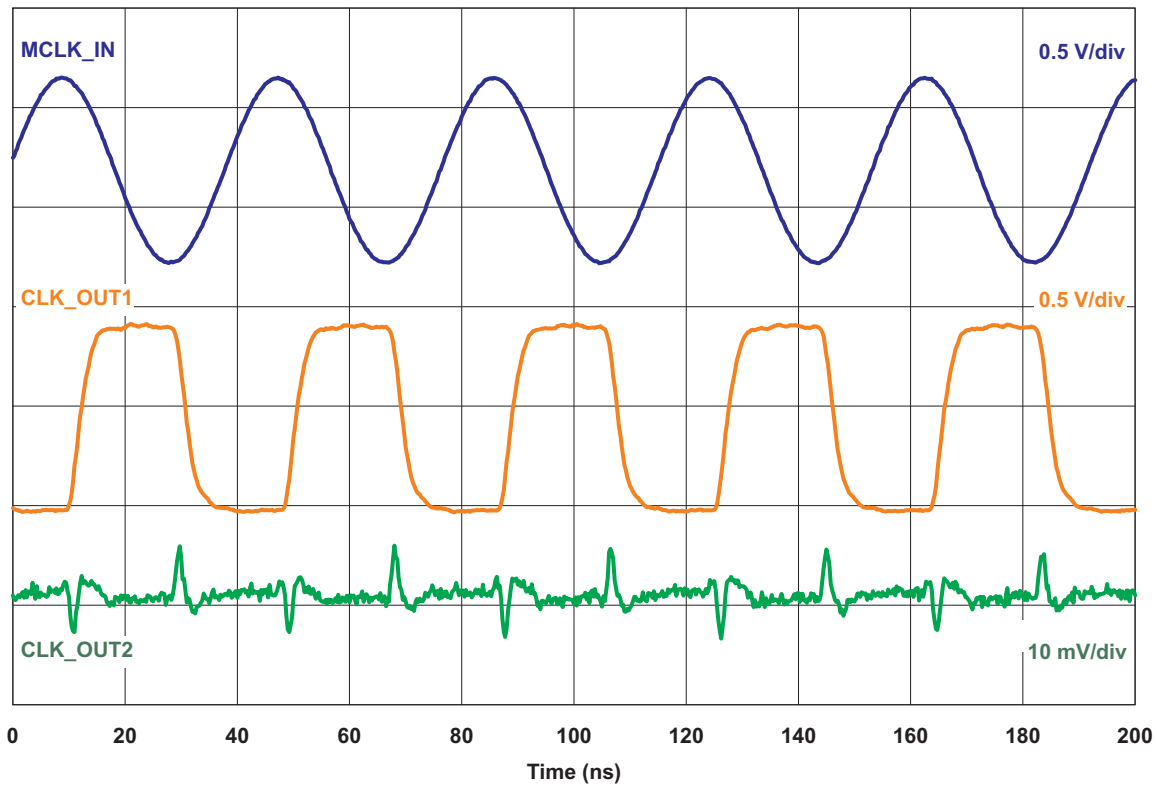
RISE TIME
VS
LOAD



TYPICAL PERFORMANCE (continued)



DIGITAL CROSS-TALK SCOPE SHOT



APPLICATION INFORMATION

Typical Application

The CDC3RL02 is ideal for use in mobile applications as shown in Figure 1. In this example, a single low noise TCXO system clock source is buffered to drive a mobile GPS receiver and WLAN transceiver. Each peripheral independently requests an active clock by asserting a single clock request line (CLK_REQ_1 or CLK_REQ_2). When both clock request lines are inactive, the CDC3RL02 enters a low current shutdown mode. In this mode, the LDO output, CLK_OUT_1, and CLK_OUT_2 are pulled to GND and the TCXO will be unpowered.

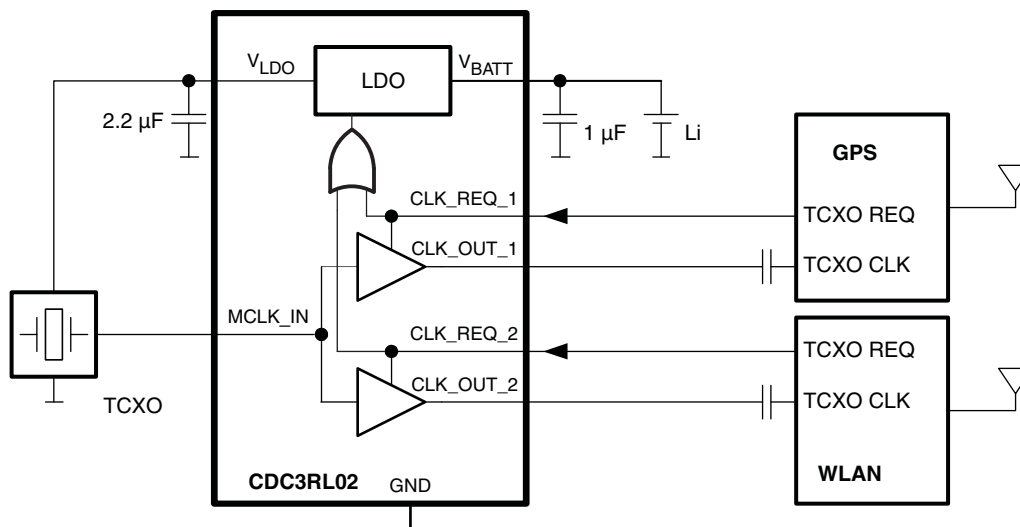


Figure 1. Mobile Application

When either peripheral requests the clock, the CDC3RL02 will enable the LDO and power the TCXO. The TCXO output (square wave, sine wave, or clipped sine wave) is converted to a square wave and buffered to the requested output.

Input Clock Squarer

Figure 2 shows the input stage of the CDC3RL02. The input signal at MCLK_IN can be a square wave or sine wave. CMCLK is an internal AC coupling capacitor that allows a direct connection from the TCXO to the CDC3RL02 without an external capacitor.

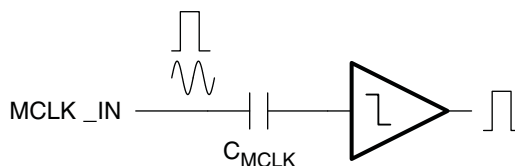


Figure 2. Input Stage

Any external component added in the series path of the clock signal will potentially add phase noise and jitter. The error source associated with the internal decoupling capacitor is included in the specification of the CDC3RL02. The recommended clock frequency band of the CDC3RL02 is 10 MHz to 52 MHz for specified functionality. All performance metrics are specified at 26 MHz. The lowest acceptable sinusoidal signal amplitude is 0.8 V_{PP} for specified performance. Amplitudes as low as 0.3 V_{PP} are acceptable but with reduced phase noise and jitter performance.

Output Stage

Each output drives 1.8-V LVCMOS levels. Adaptive output buffers limit the rise/fall time of the output to within 1 to 5ns with load capacitance between 10 pF and 50 pF. Fast slew rates introduce EMI into the system. Each output buffer limits EMI by keeping the rise/fall time above 1 ns. Slow rise/fall times can induce additive phase noise and duty cycle errors in the load device. The output buffer limits these errors by keeping the rise/fall time below 5 ns. In addition, the output stage dynamically alters impedance based on the instantaneous voltage level of the output. This dynamic change limits reflections keeping the output signal monotonic during transitions. Each output is active low when not requested to avoid false clocking of the load device.

LDO

A low noise 1.8-V LDO is integrated to provide the I/O supply for the output buffers. The LDO output is externally available to power a clock source such as a TCXO. A clean supply is provided to the clock buffers and the clock source for optimum phase noise performance. The input range of the LDO allows the device to be powered directly from a single cell Li battery. The LDO is enabled by either of the CLK_REQ_N signals. When disabled, the device enters a low power shutdown mode consuming less than 1 μ A from the battery. The LDO requires an output decoupling capacitor in the range of 1 μ F to 10 μ F for compensation and high frequency PSR. This capacitor must stay within the specified range over the entire operating temperature range. An input bypass capacitor of 1 μ F or larger is recommended.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CDC3RL02YFPR	ACTIVE	DSBGA	YFP	8	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDC3RL02YFPR	DSBGA	YFP	8	3000	180.0	8.4	0.9	1.75	0.6	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

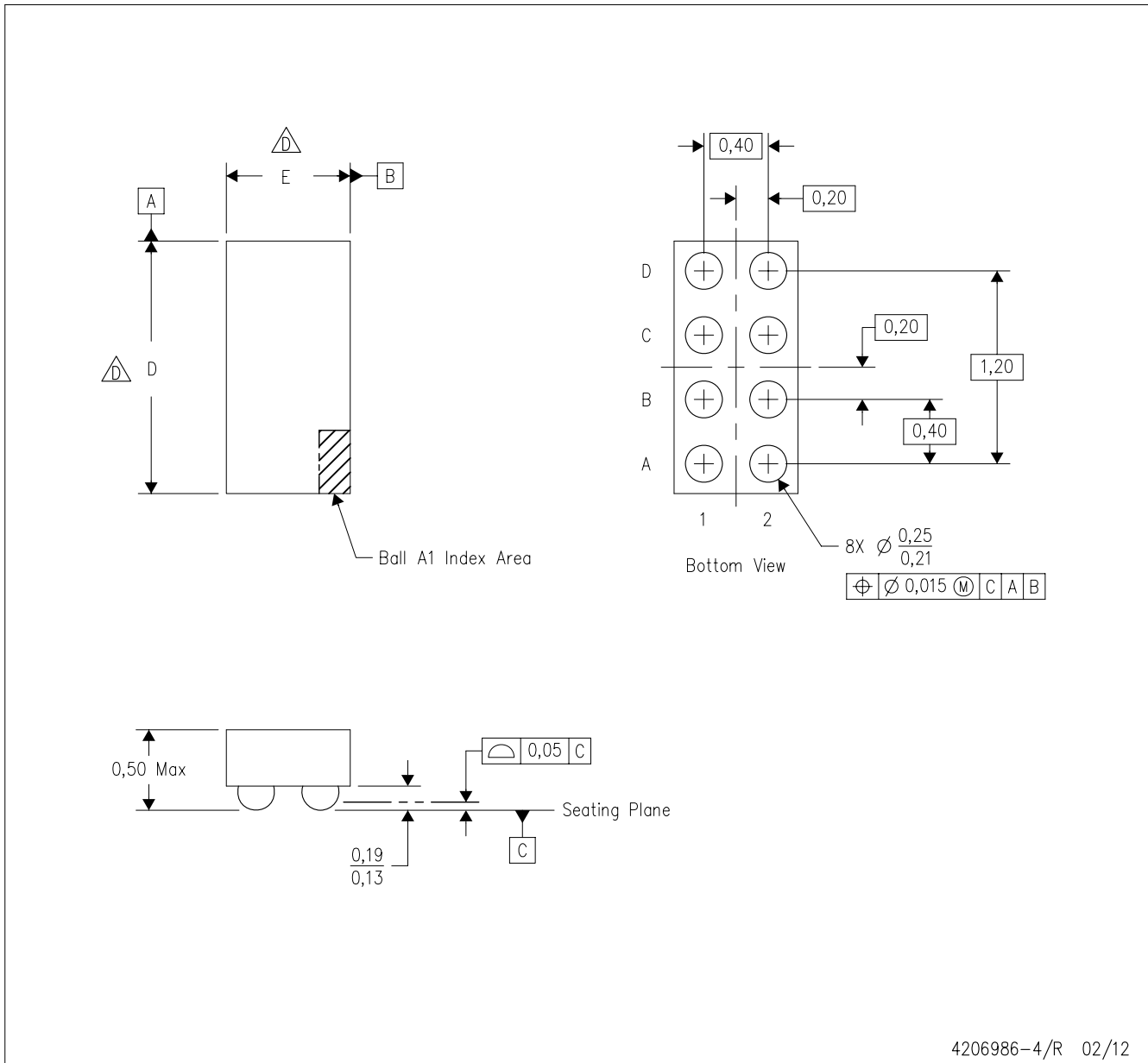


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDC3RL02YFPR	DSBGA	YFP	8	3000	220.0	220.0	34.0

YFP (R-XBGA-N8)

DIE-SIZE BALL GRID ARRAY



4206986-4/R 02/12

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.
 - $\triangle D$ The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
 - E. Reference Product Data Sheet for array population.
2 x 4 matrix pattern is shown for illustration only.
 - F. This package contains Pb-free balls.

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