N-Channel NexFET™ Power MOSFETs

Check for Samples: CSD16403Q5A

FEATURES

- **Ultra Low Q_g and Q_{gd}**
- **Low Thermal Resistance**
- **Avalanche Rated**
- **Pb Free Terminal Plating**
- **RoHS Compliant**
- **Halogen Free**
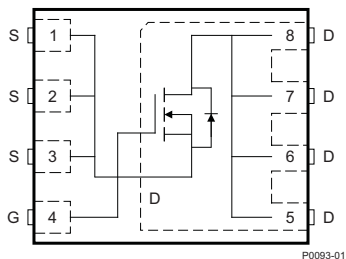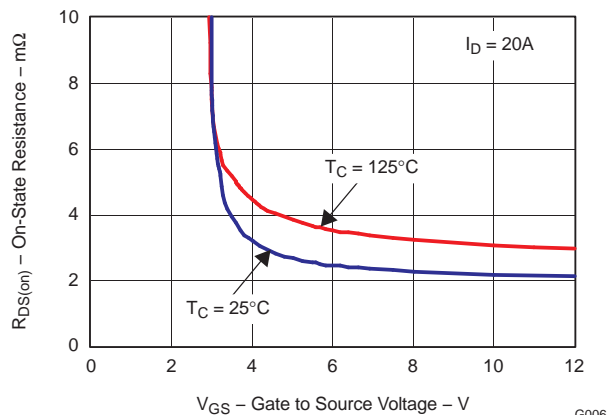- **SON 5mm x 6mm Plastic Package**

APPLICATIONS

- **Point-of-Load Synchronous Buck Converter for Applications in Networking, Telecom and Computing Systems**
- **Optimized for Control FET Applications**

DESCRIPTION

The NexFET™ power MOSFET has been designed to minimize losses in power conversion applications.

PRODUCT SUMMARY

V_{DS}	Drain to Source Voltage	25		V
Q_g	Gate Charge Total (4.5V)	13.3		nC
Q_{gd}	Gate Charge Gate to Drain	3.5		nC
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 4.5V	2.9	mΩ
		V_{GS} = 10V	2.2	mΩ
$V_{GS(th)}$	Threshold Voltage	1.6		V

ORDERING INFORMATION

Device	Package	Media	Qty	Ship
CSD16403Q5A	SON 5X6 Plastic Package	13-inch reel	2500	Tape and Reel

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise stated		VALUE	UNIT
V_{DS}	Drain to Source Voltage	25	V
V_{GS}	Gate to Source Voltage	+16 / −12	V
I_D	Continuous Drain Current, T_C = 25°C	100	A
	Continuous Drain Current[1]	28	A
I_{DM}	Pulsed Drain Current, T_A = 25°C[2]	184	A
P_D	Power Dissipation[1]	3.1	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	−55 to 150	°C
E_{AS}	Avalanche Energy, single pulse I_D = 67A, L = 0.1mH, R_G = 25Ω	224	mJ

(1) $R_{\theta JA}$ = 41°C/W on 1in^2 Cu FR4 PCB.

(2) Pulse width ≤300µs, duty cycle ≤2%
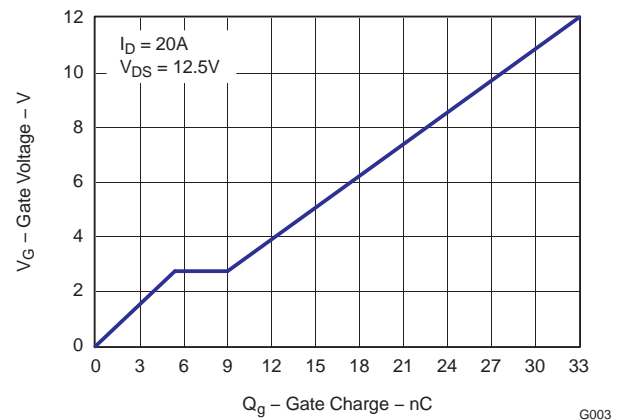
Top View

P0093-01

$R_{DS(ON)}$ vs V_{GS}

G006

Gate Charge

G003

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV_{DSS}	Drain to Source Voltage	V_{GS} = 0V, I_D = 250µA	25			V
I_{DSS}	Drain to Source Leakage Current	V_{GS} = 0V, V_{DS} = 20V			1	µA
I_{GSS}	Gate to Source Leakage Current	V_{DS} = 0V, V_{GS} = +16/-12V			100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 250µA	1.2	1.6	1.9	V
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 4.5V, I_D = 20A		2.9	3.7	mΩ
		V_{GS} = 10V, I_D = 20A		2.2	2.8	mΩ
g_{fs}	Transconductance	V_{DS} = 15V, I_D = 20A		91		S
Dynamic Characteristics						
C_{ISS}	Input Capacitance			2040	2660	pF
C_{OSS}	Output Capacitance	V_{GS} = 0V, V_{DS} = 12.5V , f = 1MHz		1600	2080	pF
C_{RSS}	Reverse Transfer Capacitance			115	160	pF
R_g	Series Gate Resistance			1.2	2.4	Ω
Q_g	Gate Charge Total (4.5V)			13.3	18	nC
Q_{gd}	Gate Charge Gate to Drain	V_{DS} = 12.5V, I_D = 20A		3.5		nC
Q_{gs}	Gate Charge Gate to Source			5.5		nC
$Qg(th)$	Gate Charge at Vth			3.1		nC
Q_{OSS}	Output Charge	V_{DS} = 13.5V, V_{GS} = 0V		33		nC
$t_{d(on)}$	Turn On Delay Time			11.8		ns
t_r	Rise Time	V_{DS} = 12.5V, V_{GS} = 4.5V, I_D = 20A, R_G = 2Ω		18.3		ns
$t_{d(off)}$	Turn Off Delay Time			15.2		ns
t_f	Fall Time			9.2		ns
Diode Characteristics						
V_{SD}	Diode Forward Voltage	I_S = 20A, V_{GS} = 0V		0.8	1.0	V
Q_{rr}	Reverse Recovery Charge	V_{DD} = 13.5V, I_F = 20A, di/dt = 300A/µs		47		nC
t_{rr}	Reverse Recovery Time	V_{DD} = 13.5V, I_F = 20A, di/dt = 300A/µs		35		ns

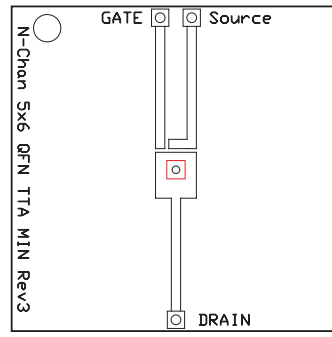## THERMAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

	PARAMETER	MIN	TYP	MAX	UNIT
$R_{θJC}$	Thermal Resistance Junction to Case[1]			1.8	°C/W
$R_{θJA}$	Thermal Resistance Junction to Ambient[1] [2]			51	°C/W

(1) $R_{θJC}$ is determined with the device mounted on a 1 inch square 2 oz. Cu pad on a 1.5 × 1.5 in 0.060 inch thick FR4 board. $R_{θJC}$ is specified by design while $R_{θJA}$ is determined by the user's board design.
(2) Device mounted on FR4 Material with 1 inch^2 of 2 oz. Cu.

Product Folder Link(s): *CSD16403Q5A*

Max $R_{\theta JA}$ = 51°C/W when mounted on 1 inch^2 of 2 oz. Cu.

Max $R_{\theta JA}$ = 118°C/W when mounted on minimum pad area of 2 oz. Cu.

TYPICAL MOSFET CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

Duty Cycle = t_1/t_2
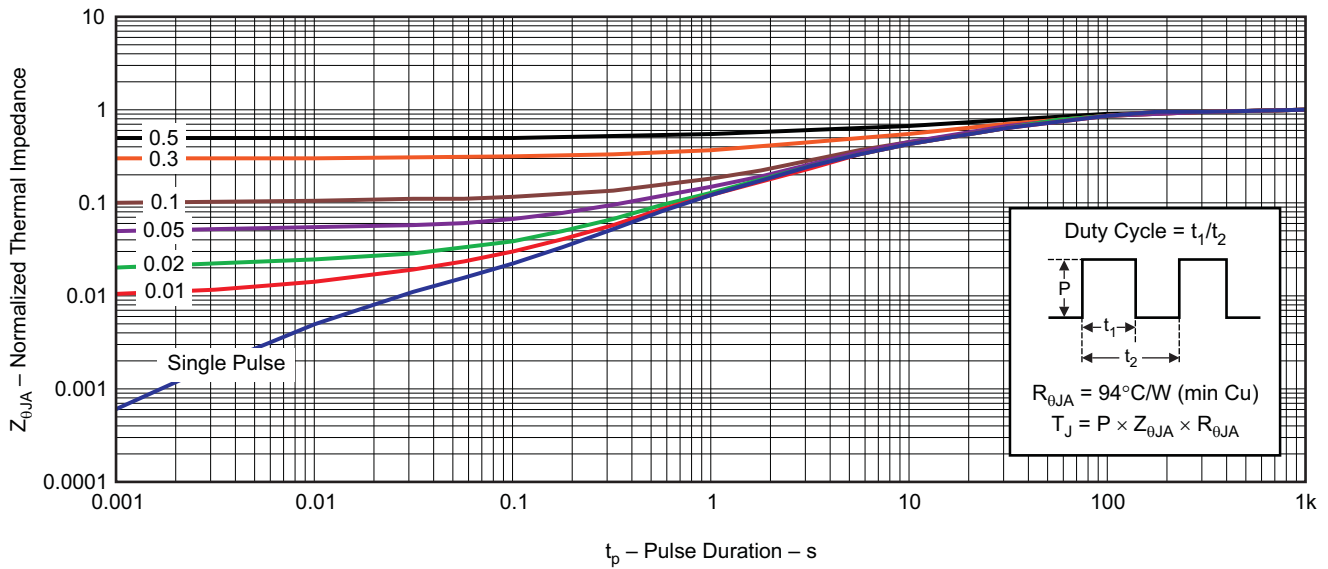
$R_{\theta JA}$ = 94°C/W (min Cu)

$T_J = P \times Z_{\theta JA} \times R_{\theta JA}$

Figure 1. Transient Thermal Impedance

Product Folder Link(s): *CSD16403Q5A*

TYPICAL MOSFET CHARACTERISTICS (continued)

(T_A = 25°C unless otherwise stated)
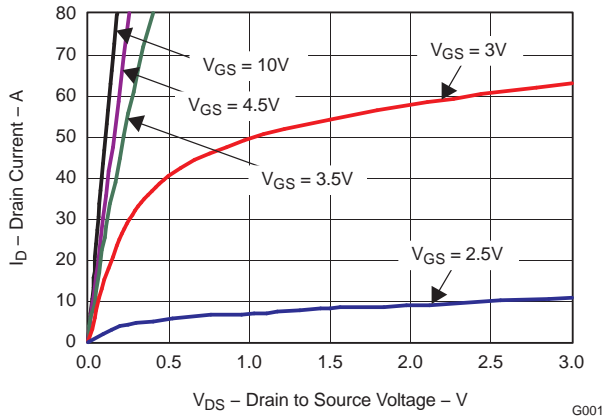
Figure 2. Saturation Characteristics
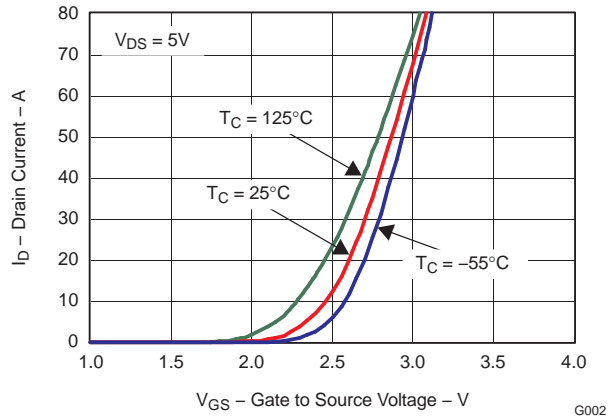
Figure 3. Transfer Characteristics
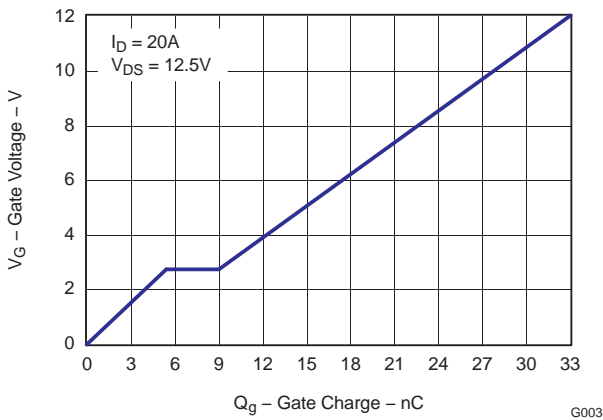
Figure 4. Gate Charge
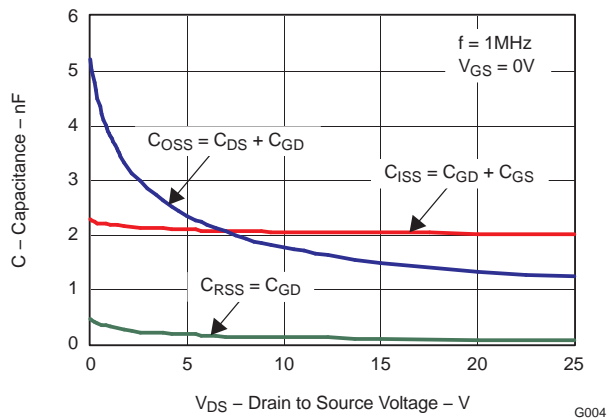
Figure 5. Capacitance
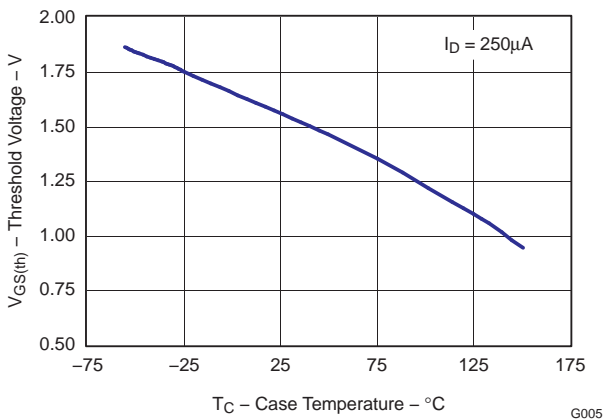
Figure 6. Threshold Voltage vs Temperature
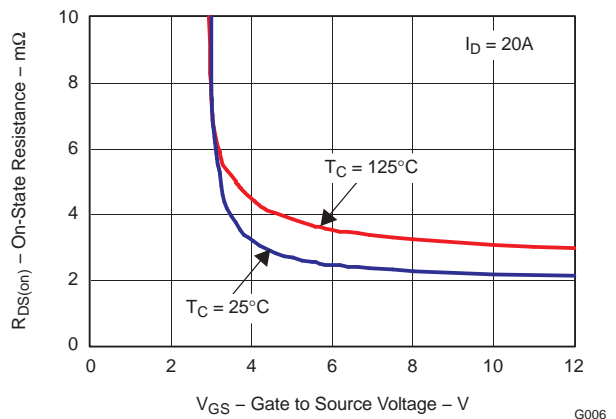
Figure 7. On Resistance vs Gate Voltage

Product Folder Link(s): CSD16403Q5A

TYPICAL MOSFET CHARACTERISTICS (continued)

(T_A = 25°C unless otherwise stated)
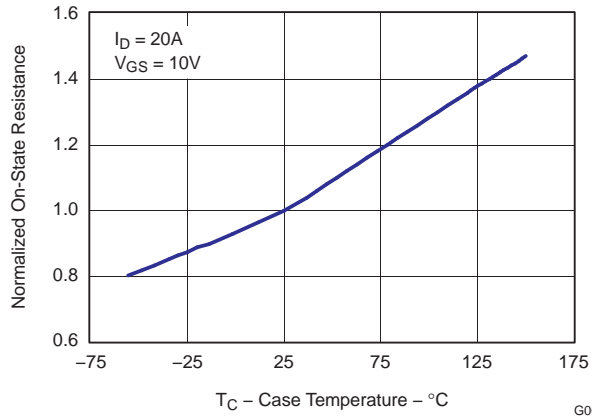
Figure 8. On Resistance vs Temperature
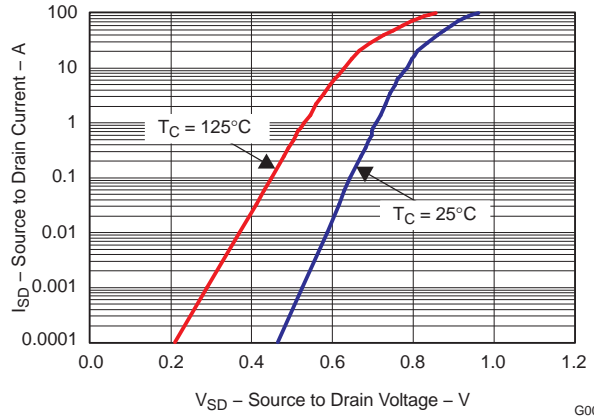
Figure 9. Typical Diode Forward Voltage
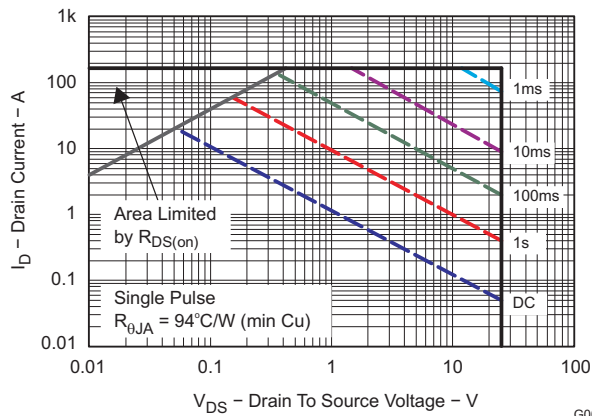
Figure 10. Maximum Safe Operating Area
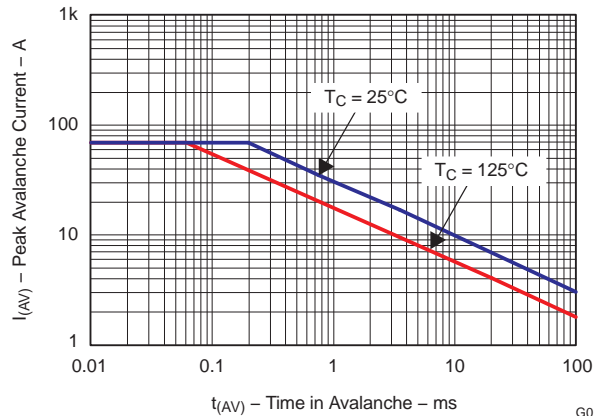
Figure 11. Single Pulse Unclamped Inductive Switching
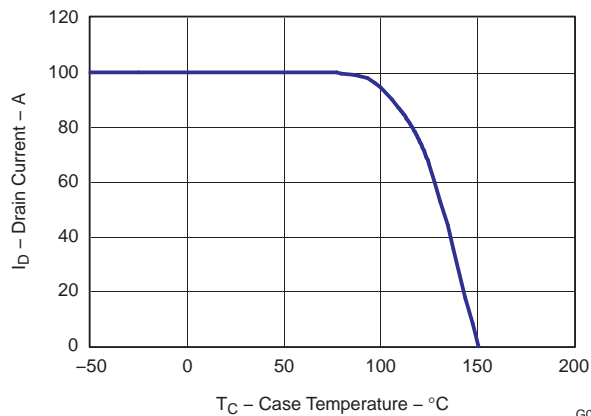
**Figure 12. Maximum Drain Current vs Temperature**

MECHANICAL DATA

Q5A Package Dimensions

Top View

Side View

Bottom View

Front View

M0135-01

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
b	0.33	0.41	0.51
c	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.81	3.96
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
e	1.27 BSC		
H	0.41	0.51	0.61
K	1.10		
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
θ	0°		12°

For recommended circuit layout for PCB designs, see application note SLPA005 – *Reducing Ringing Through PCB Layout Techniques*.

Product Folder Link(s): *CSD16403Q5A*

Recommended PCB Pattern
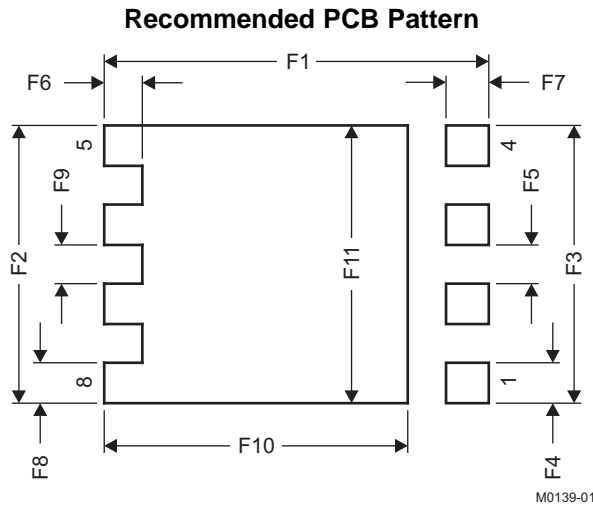
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
F1	6.205	6.305	0.244	0.248
F2	4.46	4.56	0.176	0.18
F3	4.46	4.56	0.176	0.18
F4	0.65	0.7	0.026	0.028
F5	0.62	0.67	0.024	0.026
F6	0.63	0.68	0.025	0.027
F7	0.7	0.8	0.028	0.031
F8	0.65	0.7	0.026	0.028
F9	0.62	0.67	0.024	0.026
F10	4.9	5	0.193	0.197
F11	4.46	4.56	0.176	0.18

M0139-01

Q5A Tape and Reel Information

A0 = 6.50 ±0.10
B0 = 5.30 ±0.10
K0 = 1.40 ±0.10

M0138-01
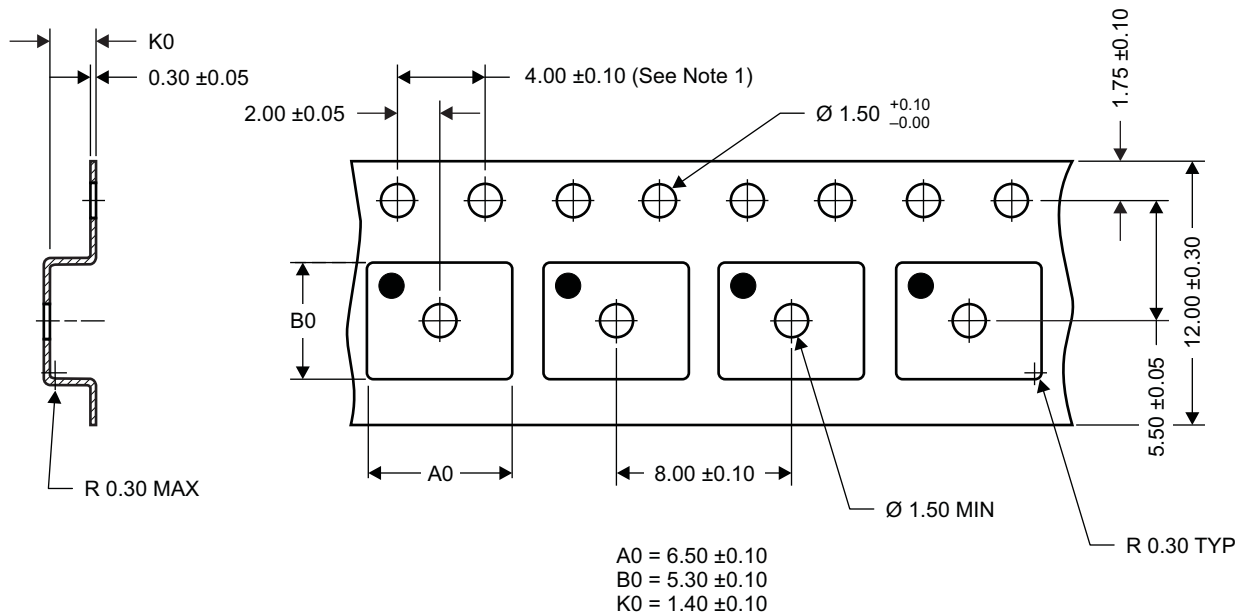
Notes:

1. 10 sprocket hole pitch cumulative tolerance ±0.2
2. Camber not to exceed 1mm IN 100mm, noncumulative over 250mm
3. Material:black static dissipative polystyrene
4. All dimensions are in mm (unless otherwise specified)
5. A0 and B0 measured on a plane 0.3mm above the bottom of the pocket
6. MSL1 260°C (IR and Convection) PbF Reflow Compatible

REVISION HISTORY

Changes from Original (August 2009) to Revision A **Page**

- Deleted the Package Marking Information section 7

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD16403Q5A	SON	DQJ	8	2500	330.0	12.4	6.3	5.3	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD16403Q5A	SON	DQJ	8	2500	340.0	340.0	38.0

IMPORTANT NOTICE

Products		Applications	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		