Quad SPST CMOS Analog Switches

DESCRIPTION

The DG441, DG442 monolithic quad analog switches are designed to provide high speed, low error switching of analog and audio signals. The DG441 has a normally closed function. The DG442 has a normally open function. Combining low on-resistance (50 Ω, typ.) with high speed (t_{ON} 150 ns, typ.), the DG441, DG442 are ideally suited for upgrading DG201A/202 sockets. Charge injection has been minimized on the drain for use in sample-and-hold circuits.

To achieve high voltage ratings and superior switching performance, the DG441, DG442 are built on Vishay Siliconix's high-voltage silicon-gate process. An epitaxial layer prevents latchup.

Each switch conducts equally well in both directions when on, and blocks input voltages to the supply levels when off.

FEATURES

- **Halogen-free according to IEC 61249-2-21 Definition**
- Low on-resistance: 50 Ω
- Low leakage: 80 pA
- Low power consumption: 0.2 mW
- Fast switching action - t_{ON}: 150 ns
- Low charge injection - Q: - 1 pC
- DG201A/DG202 upgrades
- TTL/CMOS-compatible logic
- Single supply capability
- **Compliant to RoHS Directive 2002/95/EC**

BENEFITS

- Less signal errors and distortion
- Reduced power supply requirements
- Faster throughput
- Improved reliability
- Reduced pedestal errors
- Simplifies retrofit
- Simple interfacing

APPLICATIONS

- Audio switching
- Battery powered systems
- Data acquisition
- Hi-Rel systems
- Sample-and-hold circuits
- Communication systems
- Automatic test equipment
- Medical instruments

Pb-free

RoHS COMPLIANT

HALOGEN FREE

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

Dual-In-Line and SOIC
DG441
Top View

LCC
DG441
Top View
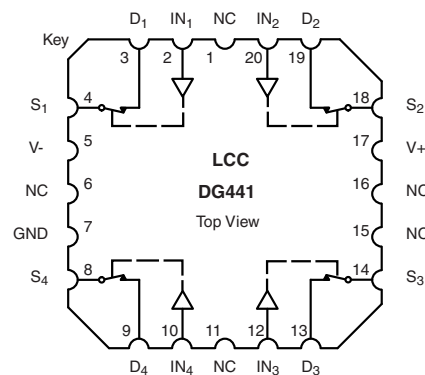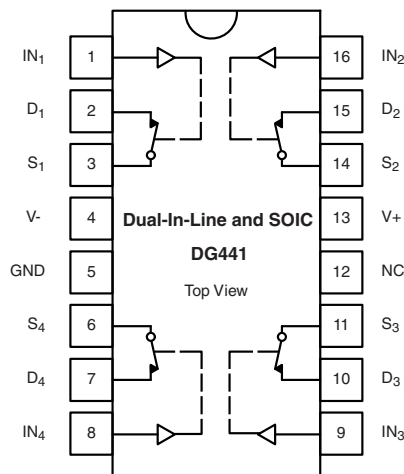
TRUTH TABLE		
Logic	**DG441**	**DG442**
0	On	Off
1	Off	On

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

ORDERING INFORMATION

Temp. Range	Package	Part Number
- 40 °C to 85 °C	16-pin plastic DIP	DG441DJ DG441DJ-E3
		DG442DJ DG442DJ-E3
	16-pin narrow SOIC	DG441DY DG441DY-E3 DG441DY-T1 DG441DY-T1-E3
		DG442DY DG442DY-E3 DG442DY-T1 DG442DY-T1-E3

ABSOLUTE MAXIMUM RATINGS

Parameter		Limit	Unit
V+ to V-		44	V
GND to V-		25	
Digital Inputs[a], V_S, V_D		(V-) - 2 to (V+) + 2 or 30 mA, whichever occurs first	
Continuous Current (any terminal)		30	mA
Current, S or D (pulsed at 1 ms, 10 % duty cycle)		100	
Storage Temperature	(AK suffix)	- 65 to 150	°C
	(DJ, DY suffix)	- 65 to 125	
Power Dissipation (Package)[b]	16-pin plastic DIP[c]	450	mW
	16-pin CerDIP[d]	900	
	16-pin narrow SOIC[d]	900	
	LCC-20[d]	1200	

Notes:
a. Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC board.
c. Derate 6 mW/°C above 75 °C.
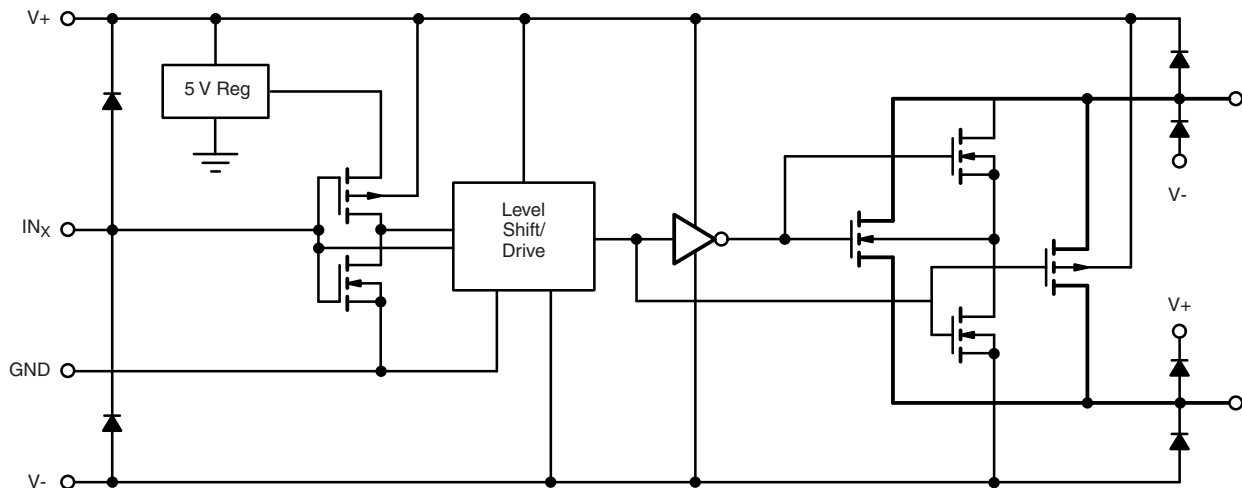d. Derate 12 mW/°C above 75 °C.

SCHEMATIC DIAGRAM Typical Channel

Figure 1.

SPECIFICATIONS[a] (Dual Supplies)

| Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V- = - 15 V V_{IN} = 2.4 V, 0.8 V[f]	Temp.[b]	Typ.[c]	A Suffix - 55 °C to 125 °C Min.[d]	Max.[d]	D Suffix - 40 °C to 85 °C Min.[d]	Max.[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		- 15	15	- 15	15	V
Drain-Source On-Resistance	$R_{DS(on)}$	I_S = - 10 mA, V_D = ± 8.5 V V+ = 13.5 V, V- = - 13.5 V	Room Full	50		85 100		85 100	Ω
On-Resistance Match Between Channels[e]	$\Delta R_{DS(on)}$	I_S = - 10 mA, V_D = ± 10 V V+ = 15 V, V- = - 15 V	Room Full			4 5		4 5	Ω
Switch Off Leakage Current	$I_{S(off)}$	V+ = 16.5, V- = - 16.5 V V_D = ± 15.5 V, V_S = ± 15.5 V	Room Full	± 0.01	- 0.5 - 20	0.5 20	- 0.5 - 5	0.5 5	nA
	$I_{D(off)}$		Room Full	± 0.01	- 0.5 - 20	0.5 20	- 0.5 - 5	0.5 5	nA
Channel On Leakage Current	$I_{D(on)}$	V+ = 16.5 V, V- = - 16.5 V V_S = V_D = ± 15.5 V	Room Full	± 0.08	- 0.5 - 40	0.5 40	- 0.5 - 10	0.5 10	nA
Digital Control									
Input Current V_{IN} Low	I_{IL}	V_{IN} under test = 0.8 V, All Other = 2.4 V	Full	- 0.01	- 500	500	- 500	500	nA
Input Current V_{IN} High	I_{IH}	V_{IN} under test = 2.4 V All Other = 0.8 V	Full	0.01	- 500	500	- 500	500	nA
Dynamic Characteristics									
Turn-On Time	t_{ON}	R_L = 1 kΩ, C_L = 35 pF V_S = ± 10 V See Figure 2	Room	150		250		250	ns
Turn-Off Time DG441	t_{OFF}		Room	90		120		120	ns
Turn-Off Time DG442			Room	110		210		210	
Charge Injection[e]	Q	C_L = 1 nF, V_S = 0 V V_{gen} = 0 V, R_{gen} = 0 Ω	Room	- 1					pC
Off Isolation[e]	OIRR	R_L = 50 Ω, C_L = 5 pF f = 1 MHz	Room	60					dB
Crosstalk (Channel-to-Channel)	X_{TALK}		Room	100					dB
Source Off Capacitance[e]	$C_{S(off)}$	f = 1 MHz	Room	4					pF
Drain Off Capacitance[e]	$C_{D(off)}$		Room	4					pF
Channel On Capacitance[e]	$C_{D(on)}$	V_{ANALOG} = 0 V	Room	16					pF
Power Supplies									
Positive Supply Current	I+	V+ = 16.5 V, V- = - 16.5 V V_{IN} = 0 or 5 V	Full	15		100		100	µA
Negative Supply Current	I-		Room Full	- 0.0001	- 1 - 5		- 1 - 5		µA
Ground Current	I_{GND}		Full	- 15	- 100		- 100		

SPECIFICATIONS[a] (Single Supply)

| Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 12 V, V- = 0 V V_{IN} = 2.4 V, 0.8 V[f]	Temp.[b]	Typ.[c]	A Suffix - 55 °C to 125 °C		D Suffix - 40 °C to 85 °C		Unit
					Min.[d]	Max.[d]	Min.[d]	Max.[d]	
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		0	12	0	12	V
Drain-Source On-Resistance	$R_{DS(on)}$	I_S = - 10 mA, V_D = 3 V, 8 V V+ = 10.8 V	Room Full	100		160 200		160 200	Ω
Dynamic Characteristics									
Turn-On Time	t_{ON}	R_L = 1 kΩ, C_L = 35 pF V_S = 8 V See Figure 2	Room	300		450		450	ns
Turn-Off Time	t_{OFF}		Room	60		200		200	
Charge Injection	Q	C_L = 1nF, V_{gen} = 6 V, R_{gen} = 0 Ω	Room	2					pC
Power Supplies									
Positive Supply Current	I+	V+ = 13.2 V, V- = 0 V V_{IN} = 0 or 5 V	Full	15		100		100	μA
Negative Supply Current	I-		Room Full	- 0.0001	- 1 - 100		- 1 - 100		
Ground Current	I_{GND}		Full	- 15	- 100		- 100		

Notes:
a. Refer to PROCESS OPTION FLOWCHART.
b. Room = 25 °C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
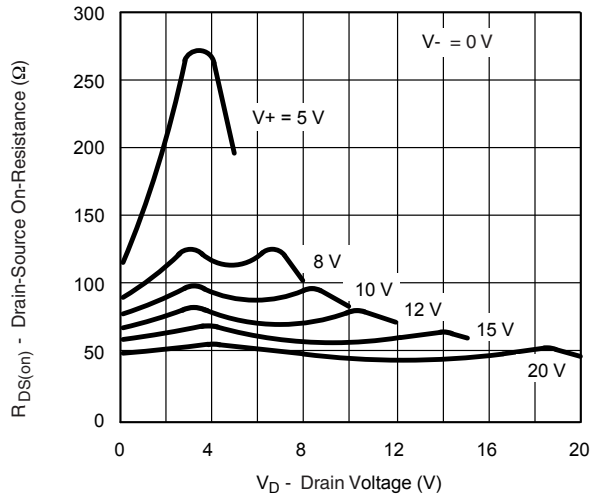
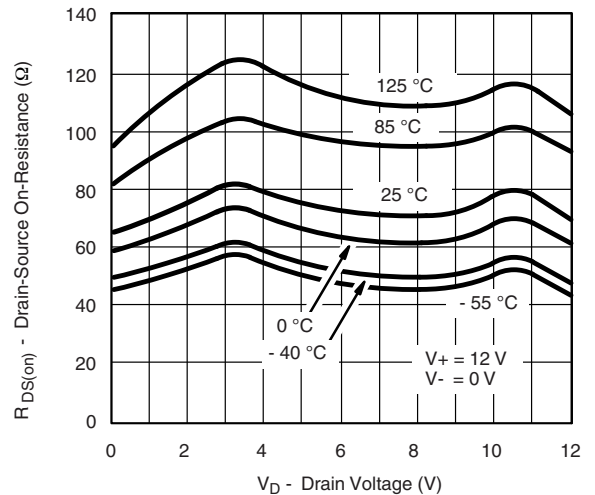## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)
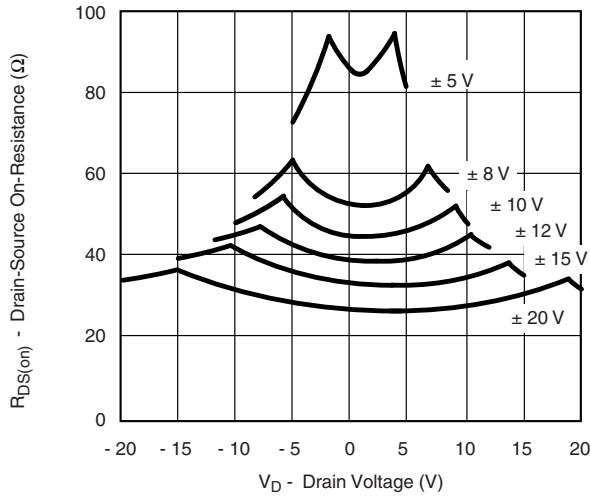
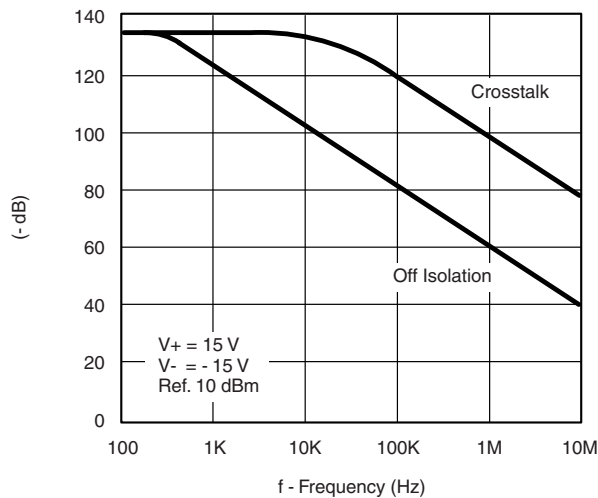**$R_{DS(on)}$ vs. V_D and Power Supply Voltage**
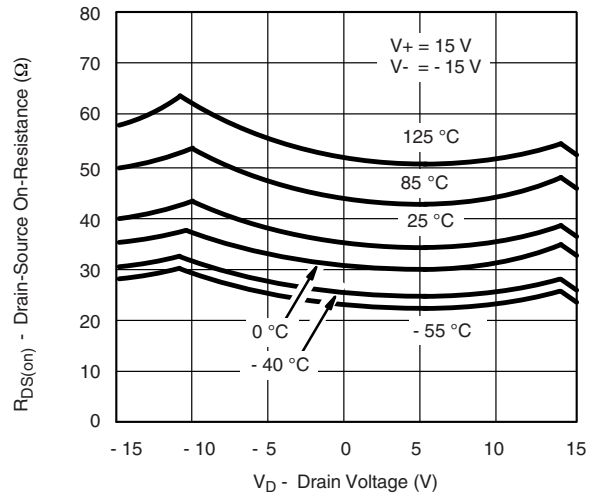
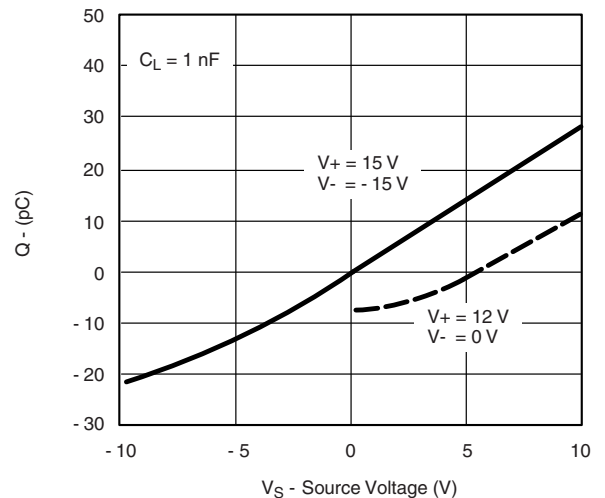**$R_{DS(on)}$ vs. V_D and Temperature**

$R_{DS(on)}$ vs. V_D and Unipolar Power Supply Voltage

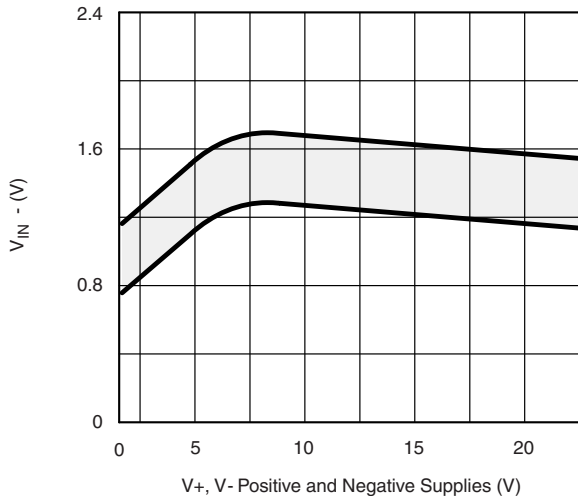**$R_{DS(on)}$ vs. V_D and Temperature (Single 12-V Supply)**
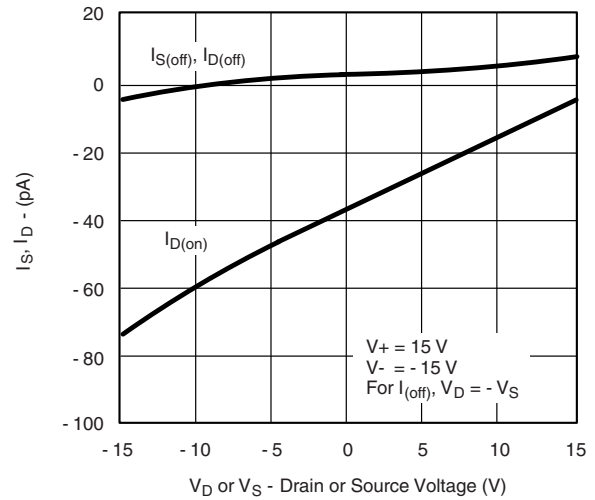

Crosstalk and Off Isolation vs. Frequency
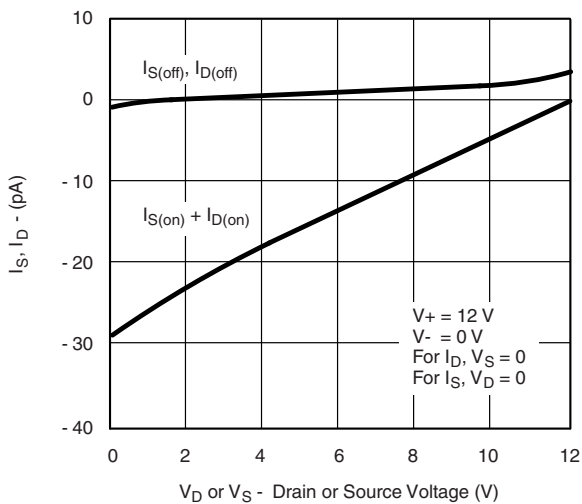

Charge Injection vs. Source Voltage

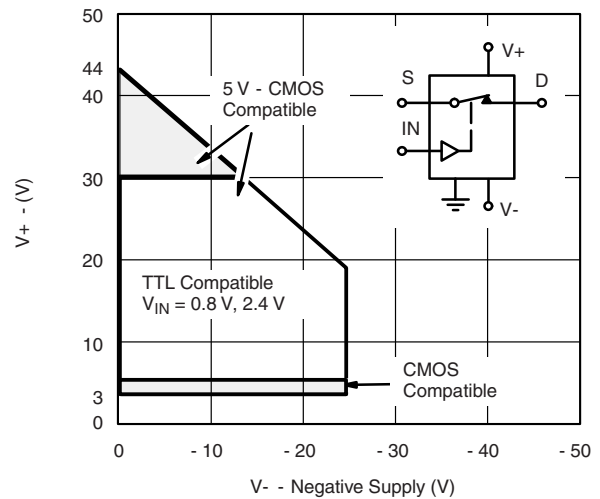## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Switching Threshold vs. Supply Voltage
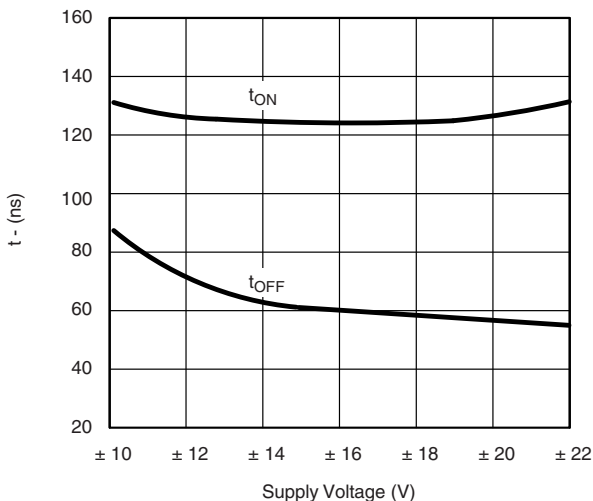

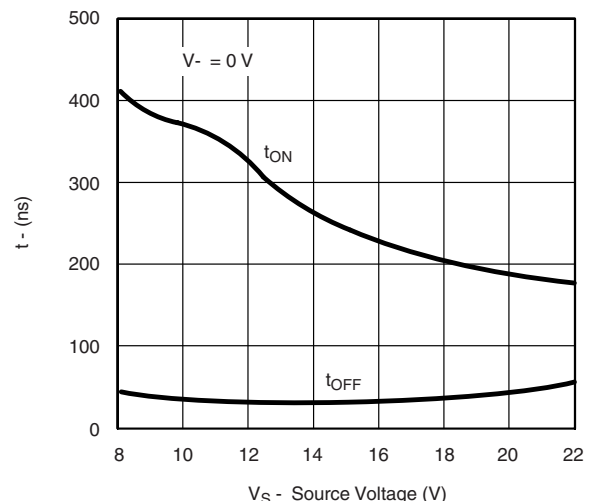**Source/Drain Leakage Currents**

Source/Drain Leakage Currents (Single 12 V Supply)
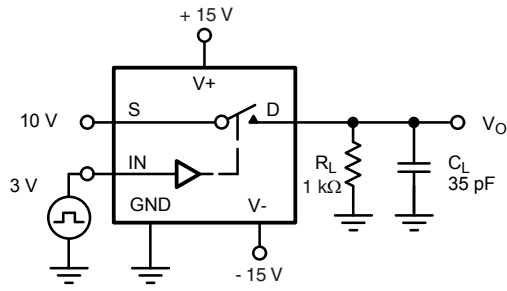

Operating Voltage

Switching Time vs. Power Supply Voltage
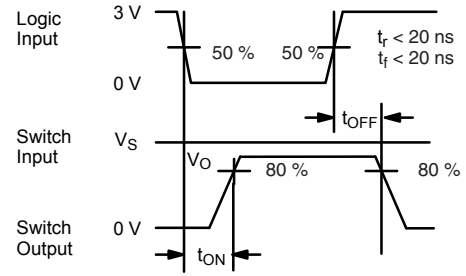

Switching Time vs. Power Supply Voltage

TEST CIRCUITS

C_L (includes fixture and stray capacitance)

Note: Logic input waveform is inverted for DG442.

Figure 2. Switching Time

Figure 3. Charge Injection
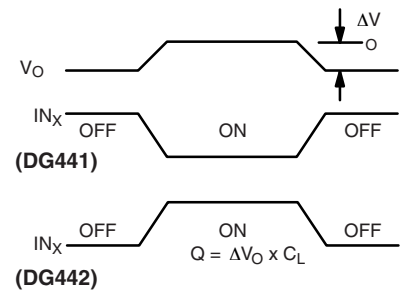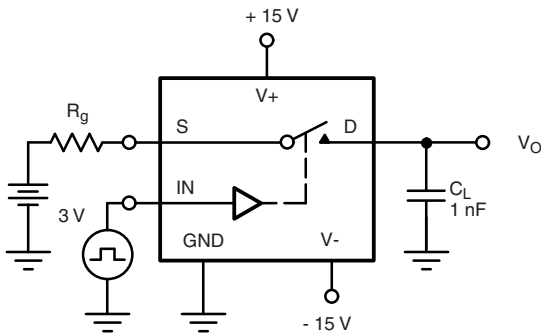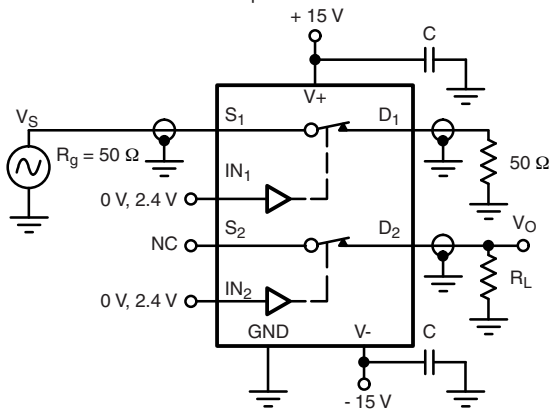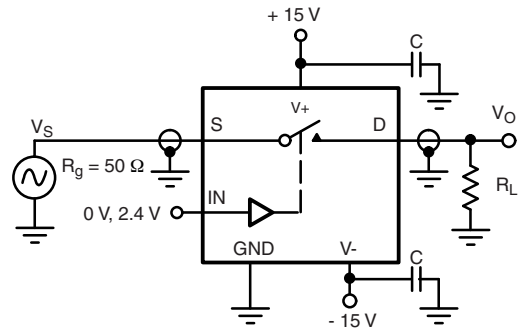

X_{TALK} Isolation $= 20 \log \left| \dfrac{V_S}{V_O} \right|$
C = RF bypass

Figure 4. Crosstalk

Off Isolation $= 20 \log \left| \dfrac{V_S}{V_O} \right|$

Figure 5. Off Isolation
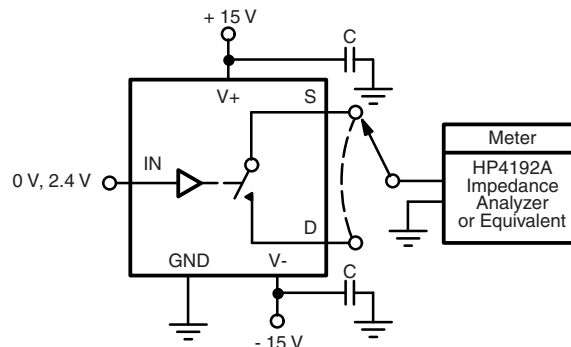
Figure 6. Source/Drain Capacitances

APPLICATIONS
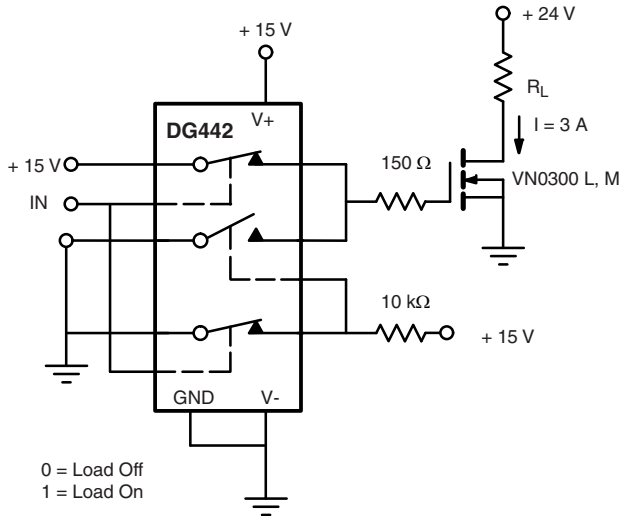
Figure 7. Power MOSFET Driver

0 = Load Off
1 = Load On
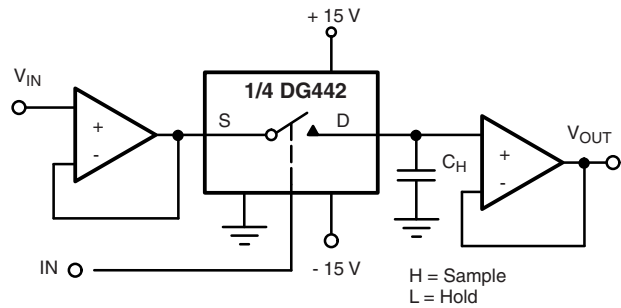
Figure 8. Open Loop Sample-and-Hold

H = Sample
L = Hold

Gain error is determined only by the resistor tolerance. Op amp offset and CMRR will limit accuracy of circuit.

With SW$_4$ Closed

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_1 + R_2 + R_3 + R_4}{R_4} = 100$$

GAIN$_1$ A$_V$ = 1
GAIN$_2$ A$_V$ = 10
GAIN$_3$ A$_V$ = 20
GAIN$_4$ A$_V$ = 100

R$_1$ 90 kΩ
R$_2$ 5 kΩ
R$_3$ 4 kΩ
R$_4$ 1 kΩ

DG441 or DG442
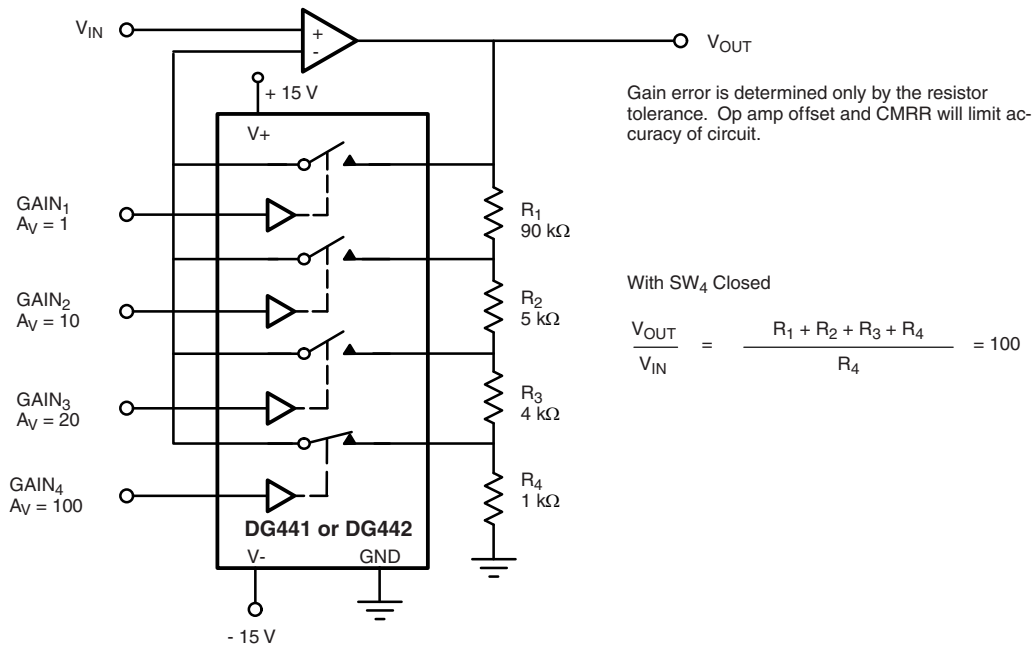
Figure 9. Precision-Weighted Resistor Programmable-Gain Amplifier

Document Number: 70053
S11-1066-Rev. J, 30-May-11

SOIC (NARROW): 16-LEAD

JEDEC Part Number: MS-012

Dim	MILLIMETERS		INCHES	
	Min	**Max**	**Min**	**Max**
A	1.35	1.75	0.053	0.069
A$_1$	0.10	0.20	0.004	0.008
B	0.38	0.51	0.015	0.020
C	0.18	0.23	0.007	0.009
D	9.80	10.00	0.385	0.393
E	3.80	4.00	0.149	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
L	0.50	0.93	0.020	0.037
$\oslash$	0°	8°	0°	8°

ECN: S-03946—Rev. F, 09-Jul-01
DWG: 5300

All Leads

$\oslash$	0.101 mm
	0.004 IN

PDIP: 16-LEAD
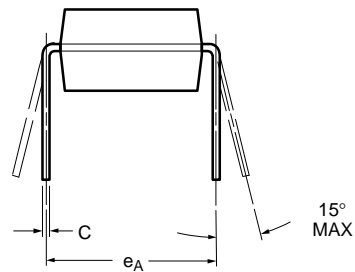
Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	3.81	5.08	0.150	0.200
A_1	0.38	1.27	0.015	0.050
B	0.38	0.51	0.015	0.020
B_1	0.89	1.65	0.035	0.065
C	0.20	0.30	0.008	0.012
D	18.93	21.33	0.745	0.840
E	7.62	8.26	0.300	0.325
E_1	5.59	7.11	0.220	0.280
e_1	2.29	2.79	0.090	0.110
e_A	7.37	7.87	0.290	0.310
L	2.79	3.81	0.110	0.150
Q_1	1.27	2.03	0.050	0.080
S	0.38	1.52	.015	0.060

ECN: S-03946—Rev. D, 09-Jul-01
DWG: 5482

CERDIP: 16-LEAD

	MILLIMETERS		INCHES	
Dim	**Min**	**Max**	**Min**	**Max**
A	4.06	5.08	0.160	0.200
A₁	0.51	1.14	0.020	0.045
B	0.38	0.51	0.015	0.020
B₁	1.14	1.65	0.045	0.065
C	0.20	0.30	0.008	0.012
D	19.05	19.56	0.750	0.770
E	7.62	8.26	0.300	0.325
E₁	6.60	7.62	0.260	0.300
e₁	2.54 BSC		0.100 BSC	
eₐ	7.62 BSC		0.300 BSC	
L	3.18	3.81	0.125	0.150
L₁	3.81	5.08	0.150	0.200
Q₁	1.27	2.16	0.050	0.085
S	0.38	1.14	0.015	0.045
∝	0°	15°	0°	15°
ECN: S-03946—Rev. G, 09-Jul-01				
DWG: 5403				

20-LEAD LCC
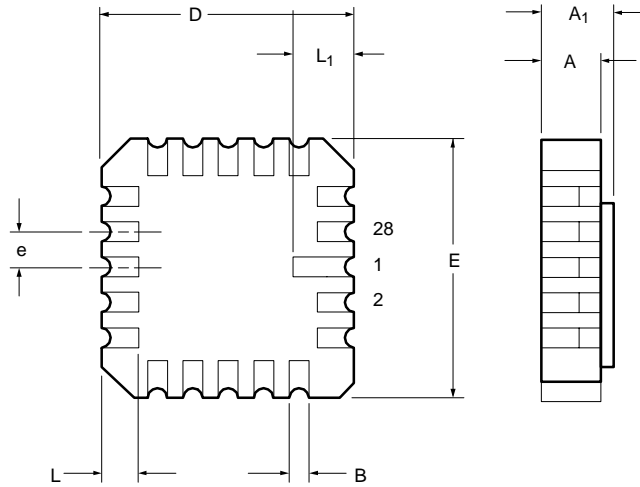
Dim	MILLIMETERS		INCHES	
	Min	**Max**	**Min**	**Max**
A	1.37	2.24	0.054	0.088
A$_1$	1.63	2.54	0.064	0.100
B	0.56	0.71	0.022	0.028
D	8.69	9.09	0.342	0.358
E	8.69	9.09	0.442	0.358
e	1.27 BSC		0.050 BSC	
L	1.14	1.40	0.045	0.055
L$_1$	1.96	2.36	0.077	0.093
ECN: S-03946—Rev. B, 09-Jul-01 DWG: 5321				

RECOMMENDED MINIMUM PADS FOR SO-16
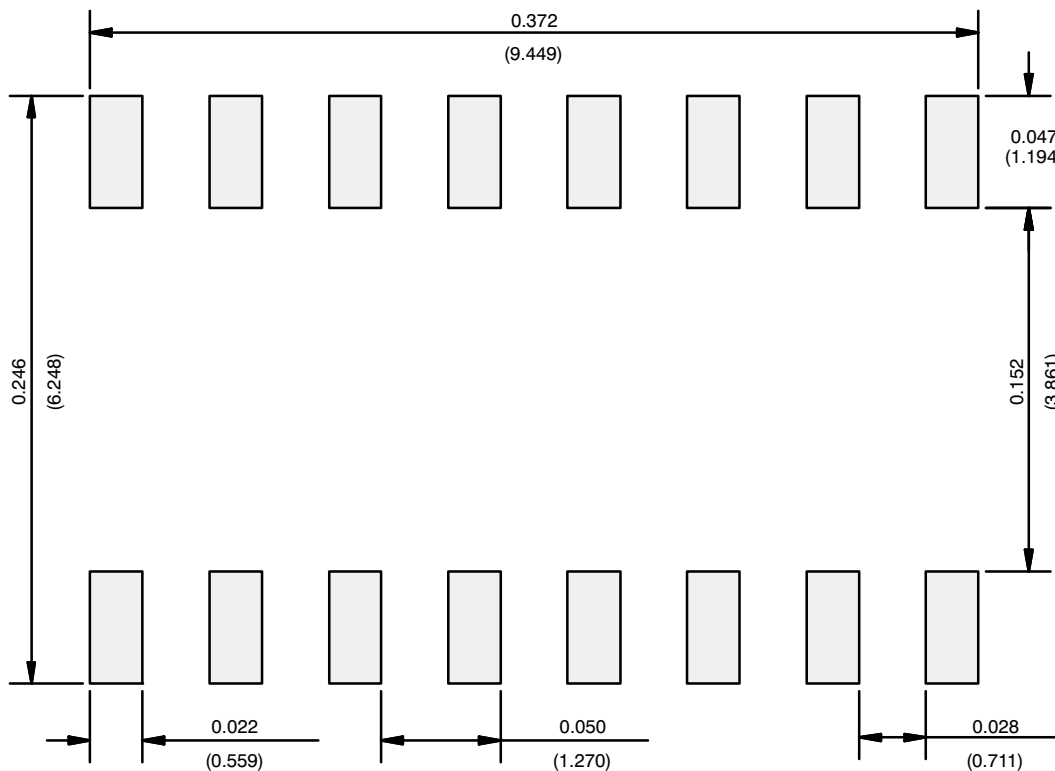
Recommended Minimum Pads
Dimensions in Inches/(mm)

Return to Index

APPLICATION NOTE

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