M74LS197P

PRESETTABLE 4-BIT BINARY COUNTER/LATCH

DESCRIPTION

The M74LS197P is a semiconductor integrated circuit containing an asynchronous hexadecimal (4-bit binary) counter function with direct reset and preset inputs.

FEATURES

- Direct reset input and asychronous preset input provided
- Usable independently as binary and octal counter
- High-speed counting (f_{max}= 80MHz typical)
- Wide operating temperature range (T_a = −20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

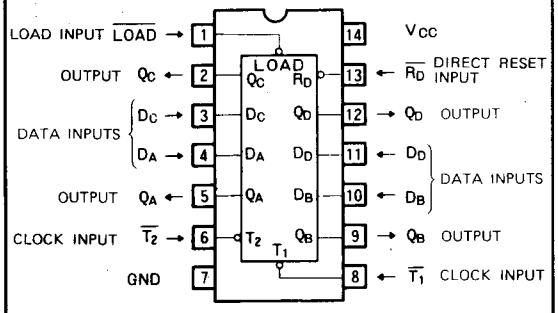
FUNCTIONAL DESCRIPTION

This device is composed of independent binary and octal counters. Clock input $\overline{T_1}$ and output Q_A are employed for use as a binary counter while clock input $\overline{T_2}$ and Q_B, Q_C and Q_D are employed for use as an octal counter. When employed as a hexadecimal counter, Q_A and $\overline{T_2}$ are connected and by making $\overline{T_1}$ the input, the count number as a 4-bit pure binary code appears in outputs Q_A, Q_B, Q_C and Q_D. Counting is performed when $\overline{T_1}$ and $\overline{T_2}$ are changed from high to low.

The counter can be preset by applying data to data inputs D_A, D_B, D_C and D_D and by setting $\overline{LOAD}$ input low, and the D_A, D_B, D_C and D_D signals appear in Q_A, Q_B, Q_C, Q_D outputs irrespective of the $\overline{T_1}$ and $\overline{T_2}$ inputs.

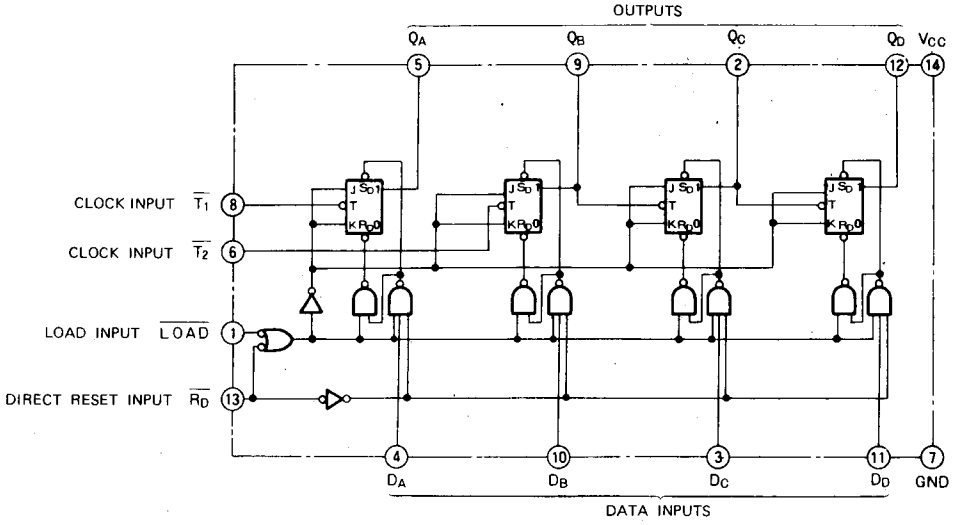
For resetting, it is possible to set Q_A = Q_B = Q_C = Q_D = low by setting direct reset input $\overline{R_D}$ low irrespective of the status of the other inputs.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

PRESETTABLE 4-BIT BINARY COUNTER/LATCH

FUNCTION TABLE (Note 1)

$\overline{T}$	$\overline{R_D}$	$\overline{LOAD}$	Q_A	Q_B	Q_C	Q_D
X	L	X	L	L	L	L
X	H	L	D_A	D_B	D_C	D_D
↓	H	H	Count			

Note 1 ↓ : Transition from high to low (negative trigger)
X : Irrelevant

Count number	Q_A	Q_B	Q_C	Q_D
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

(1) Valid when Q_A and $\overline{T_2}$ are connected and $\overline{T_1}$ is made the input

ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage	Inputs $\overline{T_1}$, $\overline{T_2}$	−0.5 ~ +5.5	V
		Inputs $\overline{LOAD}$, $\overline{R_D}$, D_A ~ D_D	−0.5 ~ +15	
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	℃
Tstg	Storage temperature range		−65 ~ +150	℃

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

PRESETTABLE 4-BIT BINARY COUNTER/LATCH

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits Min	Limits Typ *	Limits Max	Unit
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		$V_{CC}=4.75V$, $I_{IC}=-18mA$				−1.5	V
V_{OH}	High-level output voltage		$V_{CC}=4.75V$, $V_I=0.8V$ $V_I=2V$, $I_{OH}=-400\mu A$		2.7	3.4		V
V_{OL}	Low-level output voltage		$V_{CC}=4.75V$	$I_{OL}=4mA$		0.25	0.4	V
			$V_I=0.8V$, $V_I=2V$	$I_{OL}=8mA$		0.35	0.5	V
I_{IH}	High-level input current	$\overline{LOAD}$, D_A, D_B, D_C, D_D	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
		$\overline{R_D}$, $\overline{T_1}$, $\overline{T_2}$					40	μA
		$\overline{T_1}$, $\overline{T_2}$	$V_{CC}=5.25V$, $V_I=5.5V$				0.2	mA
		$\overline{LOAD}$, D_A, D_B, D_C, D_D	$V_{CC}=5.25V$, $V_I=10V$				0.1	mA
		$\overline{R_D}$					0.2	mA
I_{IL}	Low-level input current	$\overline{LOAD}$, D_A, D_B, D_C, D_D	$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
		$\overline{R_D}$					−0.8	mA
		$\overline{T_1}$					−2.4	mA
		$\overline{T_2}$					−1.3	mA
I_{OS}	Short-circuit output current (note 2)		$V_{CC}=5.25V$, $V_O=0V$		−20		−100	mA
I_{CC}	Supply current		$V_{CC}=5.25V$ (Note 3)			16	27	mA

* : All typical values are at $V_{CC}=5V$, $Ta=25°C$.

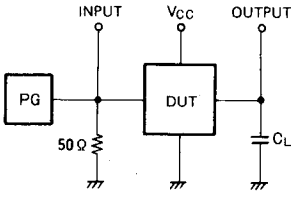
Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all inputs at 0V.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $Ta=25°C$, unless otherwise noted)

Symbol	Parameter	Test conditons	Limits Min	Limits Typ	Limits Max	Unit
fmax	Maximum clock frequency ($\overline{T_1}$)	$C_L=15pF$ (Note 4)	30	80		MHz
fmax	Maximum clock frequency ($\overline{T_2}$)			35		MHz
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{T_1}$ to output Q_A			6	15	ns
t_{PHL}				7	21	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{T_2}$ to output Q_B			8	19	ns
t_{PHL}				8	35	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{T_2}$ to output Q_C			15	51	ns
t_{PHL}				15	63	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{T_2}$ to output Q_D			22	78	ns
t_{PHL}				24	95	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs D_A, D_B, D_C, D_D to outputs Q_A, Q_B, Q_C, Q_D			8	27	ns
t_{PHL}				10	44	ns
t_{PLH}	Low-to-high-level output propagation time, from input $\overline{LOAD}$ to outputs Q_A, Q_B, Q_C, Q_D			13	39	ns
t_{PHL}				10	45	ns
t_{PHL}	High-to-low-level output propagation time, from input $\overline{R_D}$ to outputs Q_A, Q_B, Q_C, Q_D			13	51	ns

Note 4: Measurement circuit



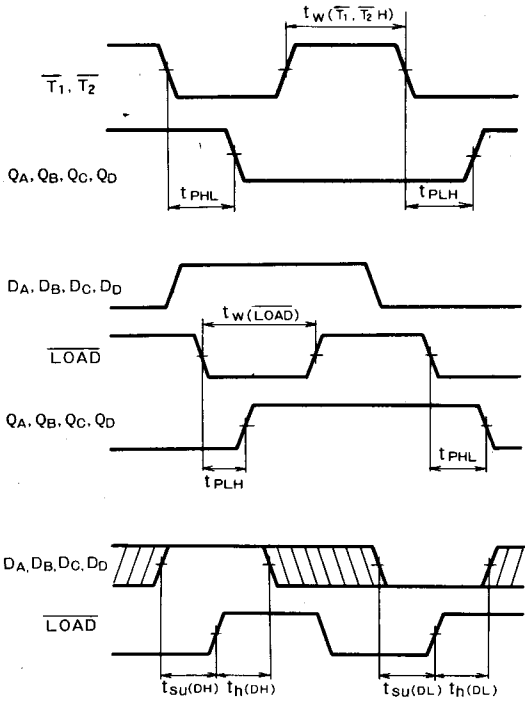
(1) The pusle generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns,
$V_P = 3V_{P\text{-}P}$, Zo = 50Ω.

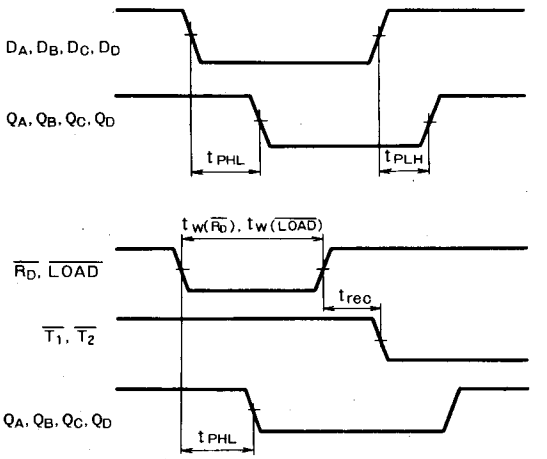
(2) C_L includes probe and jig capacitance

TIMING REQUIREMENTS (V_{CC} = 5 V, Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{w(\overline{T_1}H)}$	Clock input $\overline{T_1}$ high pulse width		20	5		ns
$t_{w(\overline{T_2}H)}$	Clock input $\overline{T_2}$ high pulse width		30	14		ns
$t_{w(\overline{LOAD})}$	Load $\overline{LOAD}$ input pulse width		20	8		ns
$t_{w(\overline{R_D})}$	Direct reset $\overline{R_D}$ pulse width		15	4		ns
$t_{su(DL)}$	Setup time D_A~D_D low to $\overline{LOAD}$		15	3		ns
$t_{su(DH)}$	Setup time D_A~D_D high to $\overline{LOAD}$		10	0		ns
$t_{h(DL)}$	Hold time D_A~D_D low to $\overline{LOAD}$		6	0		ns
$t_{h(DH)}$	Hold time D_A~D_D high to $\overline{LOAD}$		3	−1		ns
$t_{rec(\overline{LOAD})}$	Recovery time $\overline{LOAD}$ to $\overline{T}$		30	7		ns
$t_{rec(\overline{R_D})}$	Recovery time $\overline{R_D}$ to $\overline{T}$		30	7		ns

TIMING DIAGRAM (Reference level = 1.3V)





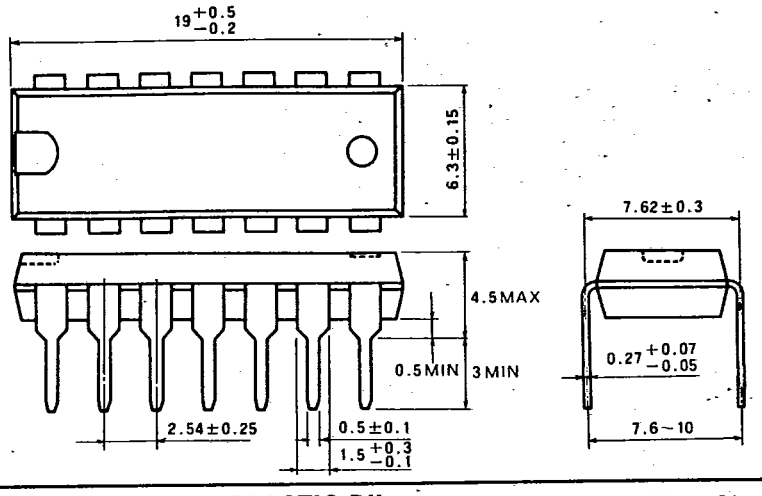
Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.

MITSUBISHI {DGTL LOGIC} 07E D 6249827 0013561 3

T-90-20

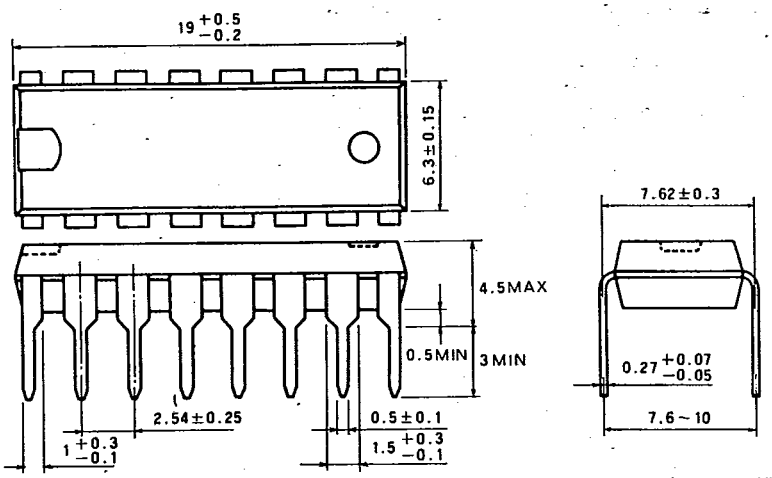
TYPE 14P4 14-PIN MOLDED PLASTIC DIL

Dimension in mm



TYPE 16P4 16-PIN MOLDED PLASTIC DIL

Dimension in mm



TYPE 20P4 20-PIN MOLDED PLASTIC DIL

Dimension in mm