Gb/s (Gigabit) Ethernet: 1.25 GBd 850 nm VCSEL Transceiver in Low Cost 1x9 Package Style

Preliminary Technical Data

HFBR-5305

Features

- **Compliant with Proposed Specifications for IEEE-802.3z/D2 Gigabit Ethernet (1000Base-SX)**
- **850 nm Vertical Cavity Surface Emitting Laser (VCSEL) Source Technology**
- **Industry Standard 1x9 Pin-Out Package Style with Integral Duplex SC Connector**
- **PMC (PCI Mezzanine Card) Compliant Package Style with 9.8 mm Height**
- **Laser AEL Class I (Eye Safe) per US 21 CFR(J)**
- **Laser AEL Class 1 (Eye Safe) per EN 60825-1 (+A11)**
- **Type Tested for EN 60950 and UL 1950 Applications**
- **300 m Links in 62.5/125 μm MMF Cables**
- **550 m Links in 50/125 μm MMF Cables**
- **Single +5 V Power Supply Operation and PECL Logic Interfaces**
- **Wave Solder and Aqueous Wash Process Compatible**
- **Designed and Manufactured in an ISO 9001 Certified Facility**

Applications

- **Switch to Switch Interface**
- **Bus Extension Applications**
- **High Speed Interface for File Servers**

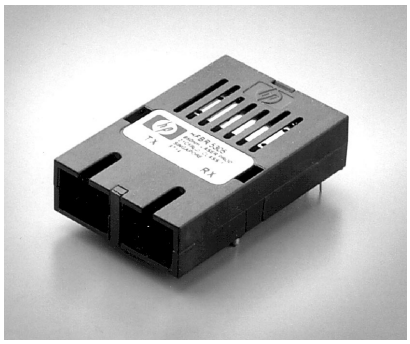
Related Products

- **1300 nm Laser Transceiver for Gigabit Ethernet IEEE 802.3z 1000Base-LX Applications (HFCT-5305) Supports Both Singlemode and Multimode Fiber**
- **Physical Layer ICs Available for Optical or Copper Interface (HDMP-1636/46)**
- **Versions of this Transceiver Module Also Available for Fibre Channel (HFBR-5303) and General Purpose Applications up to 1.5 GBd (HFBR-5315)**

Description

The HFBR-5305 transceiver from Hewlett-Packard allows the system designer to implement a range of solutions for multimode Gigabit Ethernet applications.

The overall HP transceiver product consists of three sections: the transmitter and receiver optical



subassemblies, an electrical subassembly, and the package housing which incorporates a duplex SC connector receptacle.

Transmitter Section

The transmitter section consists of an 850 nm VCSEL in an optical subassembly (OSA), which mates to the fiber cable. The VCSEL OSA is driven by a custom, silicon bipolar IC which converts differential PECL logic signals (ECL referenced to a +5 Volt supply) into an analog Laser Diode drive current.

Receiver Section

The receiver includes a silicon PIN photo-diode mounted together with a custom, silicon-bipolar transimpedance preamplifier IC in an OSA. This

OSA is mated to a custom silicon-bipolar circuit that provides post-amplification and quantization.

The custom silicon-bipolar circuit post-amplifier also includes a Signal Detect circuit which provides a PECL logic-high output upon detection of a usable input optical signal level. This single-ended PECL output is designed to drive a standard PECL input through a 50 Ω PECL load.

Package and Handling Instructions

Flammability

The HFBR-5305 VCSEL transceiver housing is made of high strength, heat resistant, chemically resistant, and UL 94V-0 flame retardant ULTEM® plastic (UL File #E121562).

Recommended Solder and Wash Process

The HFBR-5305 is compatible with industry-standard wave or hand solder processes.

Process plug

This transceiver is supplied with a process plug (HFBR-5200) for protection of the optical ports within the duplex SC connector receptacle. This process plug prevents contamination during wave solder and aqueous rinse as well as during handling, shipping and storage. It is made of a high-temperature, molded sealing material (UL94HB flame retardant) that can withstand 80°C and a rinse pressure of 50 lbs per square inch.

Recommended Solder fluxes

Solder fluxes used with the HFBR-5305 should be water-soluble, organic fluxes. Recommended solder fluxes include Lonco 3355-11 from London Chemical West, Inc. of Burbank, CA, and 100 Flux from Alpha-Metals of Jersey City, NJ.

Recommended Cleaning/ Degreasing Chemicals

Alcohols: methyl, isopropyl, isobutyl.

Aliphatics: hexane, heptane

Other: soap solution, naphtha.

Do not use partially halogenated hydrocarbons such as 1,1.1 trichloroethane, ketones such as MEK, acetone, chloroform, ethyl acetate, methylene dichloride, phenol, methylene chloride, or N-methylpyrolldone. Also, HP does not recommend the use of cleaners that use halogenated hydrocarbons because of their potential environmental harm.

Regulatory Compliance

(See the Regulatory Compliance Table for transceiver performance)

The overall equipment design will determine the certification level. The transceiver performance is offered as a figure of merit to assist the designer in considering their use in equipment designs.

Electrostatic Discharge (ESD)

There are two design cases in which immunity to ESD damage is important.

The first case is during handling of the transceiver prior to mounting it on the circuit board. It is important to use normal ESD handling precautions for ESD sensitive devices. These precautions include using grounded wrist straps, work benches, and floor mats in ESD controlled areas. The transceiver performance has been shown to provide adequate performance in typical industry production environments.

The second case to consider is static discharges to the exterior of the equipment chassis containing the transceiver parts. To the extent that the duplex SC connector receptacle is exposed to the outside of the equipment chassis it may be subject to whatever system-level ESD test criteria that the equipment is intended to meet. The transceiver performance is more robust than typical industry equipment requirements of today.

Electromagnetic Interference (EMI)

Most equipment designs utilizing these high-speed transceivers from Hewlett-Packard will be required to meet the requirements of FCC in the United States, CENELEC EN55022 (CISPR 22) in Europe and VCCI in Japan.

These transceivers, with their shielded design, perform to the limits listed in the table below to assist the designer in the management of the overall equipment EMI performance.

Immunity

Equipment utilizing these transceivers will be subject to radio-frequency electromagnetic fields in some environments. These transceivers have good immunity to such fields due to their shielded design.

Eye Safety

These 850 nm VCSEL-based transceivers are classified as AEL Class I (U.S. 21 CFR(J) and AEL Class 1 per EN 60825-1(+A11). They are eye safe when used within the data sheet limits under

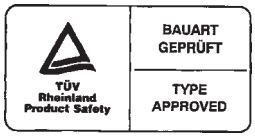
all reasonably foreseeable single fault conditions. Hewlett-Packard has tested the transceiver design for compliance with the requirements listed below under normal operating conditions and under single fault conditions. TUV Rheinland has also granted certification to these transceivers for laser eye safety and use in EN 60950, EN 60825-2, and UL 1950 applications. This performance will enable the transceivers to be used without concern for eye safety up to 7 volts transmitter V_{CC}.

CAUTION:

There are no user serviceable parts nor any maintenance required for the HFBR-5305. All adjustments are made at the factory before shipment to our customers. Tampering with or modifying the performance of the HFBR-5305 will result in voided product warranty. It may also result in improper operation of the HFBR-5305 circuitry, and possible overstress of the laser source. Device degradation or product failure may result.

Connection of the HFBR-5305 to a nonapproved optical source, operating above the recommended absolute maximum conditions or operating the HFBR-5305 in a manner inconsistent with its design and function may result in hazardous radiation exposure and may be considered an act of modifying or manufacturing a laser product. The person(s) performing such an act is required by law to recertify and reidentify the laser product under the provisions of U.S. 21 CFR(Subchapter J).

Regulatory Compliance

Feature	Test Method	Performance
Electrostatic Discharge (ESD) to the Electrical Pins	MIL-STD-883C Method 3015.4	Class 1 (>2000 V).
Electrostatic Discharge (ESD) to the Duplex SC Receptacle	Variation of IEC 801-2	Typically withstand at least 25 kV without damage when the duplex SC connector receptacle is contacted by a Human Body Model probe.
Electromagnetic Interference (EMI)	FCC Class B CENELEC EN55022 Class B (CISPR 22A) VCCI Class I	Typically provide a 4 dB margin to the FCC Class B and a 1 dB margin to the other noted standard limits when tested at a certified test range with the transceiver mounted to a circuit card without a chassis enclosure at frequencies up to 1 GHz. Margins above 1 GHz are dependent on customer board and chassis designs.
Immunity	Variation of IEC 801-3	Typically show no measurable effect from a 3 V/m field swept from 10 to 450 MHz applied to the transceiver without a chassis enclosure.
Laser Eye Safety and Equipment Type Testing 	US 21 CFR, Subchapter J per Paragraphs 1002.10 and 1002.12 EN 60825-1: 1994 +A11 EN 60825-2: 1994 EN 60950: 1992+A1+A2+A3 UL 1950/07.95	AEL Class I, FDA/CDRH Accession #9720151-00 AEL Class 1, TUV Rheinland of North America Certificate #R9771018/File #E9771047.01 Protection Class III NRTL TUV Rheinland of North America Certificate #US9771019/File #G9671066.01 Protection Class III

Application Support

Optical Power Budget and Link Penalties

The worst-case Optical Power Budget (OPB) in dB for a fiber-optic link is determined by the difference between the minimum transmitter output optical power (dBm avg) and the lowest receiver sensitivity (dBm avg). This OPB provides the necessary optical signal range to establish a working fiber-optic link. The OPB is allocated for the fiber-optic cable length and the corresponding link penalties. For proper link performance, all penalties that affect the link performance must be accounted for within the link optical power budget. The Gigabit/sec Ethernet (GbE) IEEE 802.3z standard identifies, and has modeled, the contributions of these OPB penalties to establish the link length requirements for 62.5/125 μm and 50/125 μm multimode fiber usage. In addition, single-mode fiber with standard 1300 nm Fabry-Perot lasers have been modeled and specified. Refer to the IEEE 802.3z standard and its supplemental documents that develop the model, empirical results and final specifications.

A brief description of each penalty term is given for the convenience of the designers who are not familar with these parameters. It should be noted that some of these penalties are fiber dependent while other penalties are not. Unlike incoherent Light Emitting Diodes (LED) sources, lasers emit coherent wavelengths of light. This results in optical power penalties to the optical power budget when multimode fiber is used that do not appear when LED sources are used. Explanation of optical power penalties begin with fiber-independent penalties, and end with fiber-dependent penalties. Some penalties are incorporated directly into the receiver sensitivity specification instead of the link budget specification.

Fiber-Independent Penalties:

Extinction Ratio (ER) Penalty:

GbE committee has chosen to incorporate the worst-case laser transmitter ER penalty as part of the receiver sensitivity specification. The ER penalty accounts for the receiver noise contribution due to a low-light input condition to the receiver from the laser "off" state. This noise contribution degrades the receiver sensitivity for a required Bit-Error-Ratio of 10^{-12}.

Receiver Eye-Opening Penalty:

Receiver eye-opening penalty is the optical dB penalty required to open the receiver output data eye-pattern to 30% of the baud interval (0.3 Unit Interval) at a BER = 10^{-12} to account for clock recovery circuit jitter.

Total Connector Loss Penalty:

The maximum total loss allowed for connectors is 1.5 dB. This is a fiber-length independent penalty. This connector penalty, along with all the other penalties, allow the worst-case IEEE 802.3z standard to achieve link lengths of 300 metres with 62.5/125 μm fiber and 550 metres with 50/125 μm fiber while using four, typical in-line connectors.

Fiber-Dependent Penalties:

Relative Intensity Noise (RIN) Penalty:

For the laser transmitter, the RIN penalty is due to optical noise caused by reflected optical power back into the laser device. This laser noise is seen as additional amplitude noise at the receiver and degrades the link budget accordingly. The fiber dependency results from the bandwidth of the fiber filtering the noise spectrum experienced by the receiver.

Laser Diode Modal Noise (MN) Penalty:

Laser diode MN penalty for the link is caused by the laser's coherent, spatially varying optical modes which experience Mode Selective Loss (MSL) at fiber connector discontinuities. Fundamentally, MSL results when there is a mismatch between connecting fibers that couples a subset of the original modes. This coupled subset of modes is a time-varying optical power level. The resulting MSL creates an amplitude noise detected by the receiver that degrades the available link budget.

Mode Partition Noise (MPN) Penalty:

The total optical power of a laser is the sum of many optical modes. This total optical power is constant, but the laser wavelength partitions (or "hops") between these modes. Since the optical modes are at different wavelengths, they experience different chromatic dispersion through the fiber. These various wavelengths arrive at different times and at

different optical power amplitudes. The wavelength optical energy variation creates an optical amplitude noise that the receiver experiences resulting in an MPN penalty.

Intersymbol Interference (ISI) Penalty:

The ISI penalty degrades link budget due to dispersion of the optical signal as it propagates in the fiber. The total dispersion increases with fiber length. To account for this dispersion, more optical power is required at the receiver input to maintain a particular signal-to-noise ratio in order to achieve the desired BER condition (10^{-12}).

Fiber Attentuation Penalty:

The fiber attentuation reduces optical signal power with increasing fiber length and causes a penalty to the link budget.

Figure x graphically shows the worst-case, individual optical power penalties discussed below as a function of standardized 62.5/125 µm multimode fiber length for the Gigabit/sec Ethernet HFBR-5305 850 nm VCSEL fiber-optic transceiver. From this graph, worst-case link length is shown to achieve 300 metres. The listed conditions for the Optical Power Budget and Optical Power Penalties are given to represent the fiber, laser source and receiver characteristics. For details of this analysis, refer to the IEEE 802.3z Gigabit/sec Ethernet standard for link analysis model, spreadsheet and supporting documents.

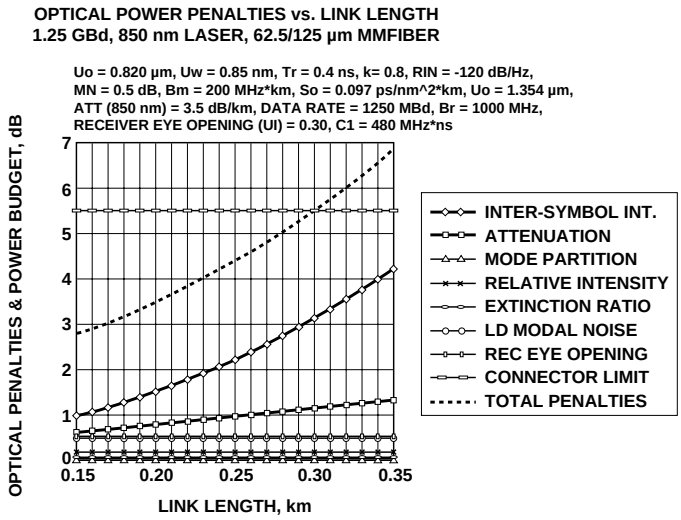


Figure 1. Individual and Total Optical Power Penalties versus Link Length at 1.25 GBd with 850 nm Laser and 62.5/125 µm Multimode Fiber.

Data Line Interconnections

Hewlett-Packard's HFBR-5305 fiber-optic transceiver is designed to directly couple to +5 V PECL signals. The transmitter inputs are internally dc-coupled to the VCSEL driver circuit from the transmitter input pins (pins 7, 8). There is no internal, capacitively-coupled 50 Ohm termination resistance within the transmitter input section. The transmitter driver circuit for the VCSEL light source is a dc-coupled circuit. This circuit regulates the output optical power. The regulated light output will maintain a constant output optical power provided the data pattern is reasonably balanced in duty factor. If the data duty factor has long, continuous state times (low or high data duty factor), then the output optical power will gradually change its average output optical power level to its nominal value of -7 dBm average.

As for the receiver section, it is internally ac-coupled between the pre-amplifier and the post-amplifier stages. The actual Data and Data-bar outputs of the post-amplifier are dc-coupled to their respective output pins (pins 2, 3). Signal Detect is a single-ended, +5 V PECL output signal that is dc-coupled to pin 4 of the module. Signal Detect should not be ac-coupled externally to the follow-on circuits because of its infrequent state changes.

Caution should be taken to account for the proper interconnection between the supporting Physical Layer integrated circuits and this HFBR-5305 transceiver. Figures 5,6,and 7 illustrate recommended interface circuits for interconnecting to a +5 Vdc PECL fiber-optic transceiver. Figure 6 illustrates a recommended test interface circuit for interconnecting to test equipment or to logic devices that are not +5 V PECL logic components.

Some fiber-optic transceiver suppliers' modules include internal capacitors, with or without 50 Ohm termination, to couple their Data and Data-bar lines to the I/O pins of their module. When designing to use these type of transceivers along with Hewlett-Packard transceivers, it is

important that the interface circuit can accommodate either internal or external capacitive coupling with 50 Ohm termination components for proper operation of both transceiver designs. The internal dc-coupled design of the HFBR-5305 I/O connections was done to provide the designer with the most flexibility for interfacing to various types of circuits.

Eye Safety Circuit
For an optical transmitter device to be eye-safe in the event of a single fault failure, the transmitter must either maintain normal, eye-safe operation or be disabled

There are three key elements to the VCSEL driver safety circuitry: a monitor diode, a window detector circuit, and direct control of the laser bias. The window detection circuit monitors the average optical power using the monitor diode. If a fault occurs such that the transmitter DC regulation circuit cannot maintain the preset bias conditions for the VCSEL emitter within ± 20%, the transmitter will automatically be disabled. Once this has occurred, only a electrical power reset will allow an attempted turn-on of the transmitter.

A data pattern with a duty factor greater than 95% may be perceived by the eye-safety circuit as a fault condition. To ensure proper operation of the link, we recommend the data pattern duty factor not exceed 95% at any time, including link start-up and system power-up.

Signal Detect
The Signal Detect circuit provides a receiver output signal that indicates the loss of an input optical signal to the receiver, functioning as an optical fault indicator for the link. The signal detect thresholds are set to decide when a modulated optical signal has fallen below a predetermined level indicating that a definite optical fault has occurred. (e.g., unplugged connector from receiver or transmitter, broken fiber, or failed far-end transmitter or data source). The Signal Detect (SD) is to indicate that an optical fault has occurred, not to detect receiver data error or error-rate. Data errors are determined by follow-on circuitry.

Evaluation Kit
To help you in your preliminary transceiver evaluation, HP offers a 1250 MBd Gigabit Ethernet evaluation board (Part # HFBR-0535). This board allows testing of the fiber-optic VCSEL transceiver. It includes the HFBR-5305 transceiver, test board, and application instructions. In addition, a complementary evaluation board is available for the HDMP-1636 1250 MBd Gigabit Ethernet serializer/deserializer (SERDES) IC. (Part # HDMP-163k) Please contact your local Field Sales representative for ordering details.

Other application materials
A reference design for the HFBR-5305 fiber-optic transceiver and the HDMP-1636/46 physical layer IC is in progress. Upon completion, all artwork will be available at the HP electronic bulletin board Please contact your local Field Sales Engineer for more information regarding application tools.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Storage Temperature	T_S	–40		100	°C	
Supply Voltage	V_{CC}	–0.5		7.0	V	1
Data Input Voltage	V_I	–0.5		V_{CC}	V	
Transmitter Differential Input Voltage	V_D			1.6	V	2
Output Current	I_D			50	mA	
Relative Humidity	RH	5		95	%	

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Ambient Operating Temperature	T_A	0		70	°C	
Case Temperature	T_C			90	°C	3
Supply Voltage	V_{CC}	4.75		5.25	V	
Power Supply Rejection	PSR		50		mV_{P-P}	4
Transmitter Data Input Voltage - Low	V_{IL}-V_{CC}	–1.810		–1.475	V	5
Transmitter Data Input Voltage - High	V_{IH}-V_{CC}	–1.165		–0.880	V	5
Transmitter Differential Input Voltage	V_D	0.3		1.6	V	
Data Output Load	R_{DL}	50			Ω	6
Signal Detect Output Load	R_{SDL}	50			Ω	6

Process Compatibility

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Hand Lead Soldering Temperature/Time	T_{SOLD}/t_{SOLD}			260/10	°C/sec.	
Wave Soldering and Aqueous Wash	T_{SOLD}/t_{SOLD}			260/10	°C/sec.	

Notes:
1. The transceiver is class 1 eye-safe up to V_{CC} = 7 V.
2. This is the maximum voltage that can be applied across the Differential Transmitter Data Inputs without damaging the input circuit.
3. Case temperature measurement referenced to the center-top of the metal transmitter shield.
4. Tested with a 50 mV_{p-p} sinusoidal signal in the frequency range from 500 Hz to 1500 MHz on the V_{CC} supply with the recommended power supply filter in place. Typically less than a 0.25 dB change in sensitivity is experienced.
5. Compatible with 10 K, 10 KH, and 100 K ECL and PECL input signals.
6. The outputs are terminated to V_{CC} - 2 V.

Transmitter Electrical Characteristics

(T_A = 0°C to +70°C, V_{CC} = 4.75 V to 5.25 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Supply Current	I_{CCT}		85	120	mA	
Power Dissipation	P_{DIST}		0.45	0.63	W	
Data Input Current – Low	I_{IL}	–350	0		µA	
Data Input Current – High	I_{IH}		16	350	µA	
Laser Reset Voltage	$V_{CCT\text{-}reset}$		2.7	2.5	V	1

Receiver Electrical Characteristics

(T_A = 0°C to +70°C, V_{CC} = 4.75 V to 5.25 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Supply Current	I_{CCR}		105	130	mA	
Power Dissipation	P_{DISR}		0.53	0.63	W	2
Data Output Voltage – Low	$V_{OL} – V_{CC}$	–1.950		–1.620	V	3
Data Output Voltage – High	$V_{OH} – V_{CC}$	–1.045		–1.740	V	3
Data Output Rise Time	t_r			0.40	ns	4, Fig. 1
Data Output Fall Time	t_f			0.40	ns	4, Fig. 1
Signal Detect Output Voltage – Low	$V_{OL} – V_{CC}$	–1.950		–1.620	V	3
Signal Detect Output Voltage – High	$V_{OH} – V_{CC}$	–1.045		–0.740	V	3
Signal Detect Assert Time (Off to On)	t_{SDA}		30	100	µs	5
Signal Detect Deassert Time (On to Off)	t_{SDD}		100	350	µs	6

Notes:

1. The Laser Reset Voltage is the voltage level below which the V_{CCT} voltage must be lowered to cause the laser driver circuit to reset from an electrical/optical shutdown condition to a proper electrical/optical operating condition. The maximum value corresponds to the worst-case highest V_{CC} voltage necessary to cause a reset condition to occur. The laser safety shutdown circuit will operate properly with transmitter V_{CC} levels of 3.5 Vdc ≤ V_{CC} ≤ 7.0 Vdc.
2. Power dissipation value is the power dissipated in the receiver itself. It is calculated as the sum of the products of V_{CC} and I_{CC} minus the sum of the products of the output voltages and currents.
3. These outputs are compatible with 10 K, 10 KH, and 100 K ECL and PECL inputs.
4. These are 20-80% values.
5. The Signal Detect output will change from logic “0” (Low) to “1” (High) within 100 µs of a step transition in optical input power from no light to -18 dBm.
6. The Signal Detect output will change from logic “1” (High) to “0” (Low) within 350 µs of a step transition in optical input power from -16 dBm to no light condition.

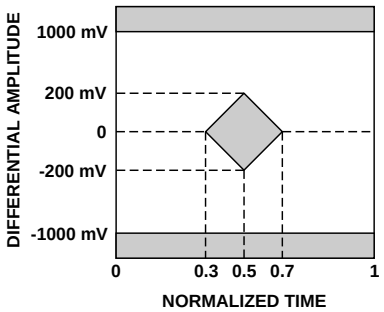


Figure 2. Receiver Electrical Eye Diagram Mask per IEEE 802.3z/D2 Figure 39-4.

Transmitter Optical Characteristics

(T_A = 0°C to +70°C, V_{CC} = 4.75 V to 5.25 V)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Reference
Output Optical Power 50/125 µm, NA = 0.20 Fiber		P_{OUT}	–10		–4	dBm avg.	1
Output Optical Power 62.5/125 µm, NA = 0.275 Fiber		P_{OUT}	–10		–4	dBm avg.	1
Optical Extinction Ratio			9			dB	2
Center Wavelength		λ_C	830	850	860	nm	
Spectral Width – rms		σ			0.85	nm rms	
Optical Rise/Fall Time		t_r/t_f			0.26	ns	3, 4, Fig. 2
RIN_{12}					–120	dB/Hz	
Transmitter Jitter Contribution	Systematic	SJ			96	ps_{p-p}	4, 7, Fig. 2
	Random	RJ			160	ps_{p-p}	4, 8, Fig. 2

Receiver Optical Characteristics

(T_A = 0°C to +70°C, V_{CC} = 4.75 V to 5.25 V)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Reference
Input Optical Power Minimum		P_{IN}			–17	dBm avg.	5
Input Optical Power Maximum		P_{IN}	0			dBm avg.	
Operating Center Wavelength		λ_C	770		860	nm	
Return Loss			12			dB	6
Signal Detect – Asserted		P_A	P_D + 1.5 dB		–18	dBm avg.	
Signal Detect – Deasserted		P_D	–45		P_A – 1.5 dB	dBm avg.	
Signal Detect – Hysteresis		$P_A – P_D$	1.5			dB	
Receiver Jitter Contribution	Systematic	SJ			64	ps_{p-p}	7
	Random	RJ			248	ps_{p-p}	8

Notes:

1. The maximum Optical Output Power complies with the IEEE 802.3z/D2 specification, and is class 1 laser eye safe.
2. Optical Extinction Ratio is defined as the ratio of the average output optical power of the transmitter in the high ("1") state to the low ("0") state. The transmitter is driven with a Gigabit Ethernet 1250 MBd 8B/10B encoded serial data pattern. This Optical Extinction Ratio is expressed in decibels (dB) by the relationship $10\log(P_{high\ avg}/P_{low\ avg})$.
3. These are unfiltered 20-80% values.
4. Laser transmitter pulse response characteristics are specified by an eye diagram (Figure 2). The characteristics include rise time, fall time, pulse overshoot, pulse undershoot, and ringing, all of which are controlled to prevent excessive degradation of the receiver sensitivity. These parameters are specified by the referenced Gigabit Ethernet eye diagram using the required filter. The output optical waveform complies with the requirements of the eye mask discussed in section 38.6.5 and Fig. 38-1 of IEEE 802.3z/D2.
5. The sensitivity conforms to the measurement definition used in 802.3z/D2 and is provided at a BER of 1×10^{-12}. The input is a Gigabit Ethernet 8B/10B encoded signal at 1250 MBd from a fast rise/fall time source with a RIN of -125dB/Hz or better. The transmitter is operating at the 1250 MBd rate during the test to simulate any cross-talk effects between the transmitter and receiver sections of the transceiver with worst case extinction ratio at the center of the eye opening over a short cable.
6. Return loss is defined as the minimum attenuation (dB) of received optical power for energy reflected back into the optical fiber.
7. Systematic Jitter is defined as the combination of Duty Cycle Distortion (Pulse-Width Distortion) and Data Dependent Jitter. Systematic Jitter is measured at the 50% signal threshold level using a Gigabit Ethernet 1250 MBd 8B/10B serial encoded data pattern signal.
8. Random Jitter is specified with a 1250 MBd (625 MHz squarewave) input signal measured at the 50% threshold level.

Table 1. Pinout Table

Pin	Symbol	Functional Description
Mounting Pins		The mounting pins are provided for transceiver mechanical attachment to the circuit board. They are embedded in the nonconductive plastic housing and are not connected to the transceiver internal circuit. They should be soldered into plated-through holes on the printed circuit board.
1	V_{EER}	Receiver Signal Ground Directly connect this pin to receiver signal ground plane.
2	RD+	Receiver Data Out RD+ is an open-emitter output circuit. Terminate this high-speed differential PECL output with standard PECL techniques at the follow-on device input pin.
3	RD–	Receiver Data Out Bar RD– is an open-emitter output circuit. Terminate this high-speed differential PECL output with standard PECL techniques at the follow-on device input pin.
4	SD	Signal Detect Normal optical input levels to the receiver result in a logic “1” output, V_{OH}, asserted. Low input optical levels to the receiver result in a fault condition indicated by a logic “0” output V_{OL}, deasserted. Signal Detect is a single-ended PECL output. SD can be terminated with standard PECL techniques via 50 Ω to V_{CCR} - 2 V. Alternatively, SD can be loaded with a 270 Ω reisistor to V_{EER} to conserve electrical power with small compromise to signal quality. If Signal Detect output is not used, leave it open-circuited. This Signal Detect output can be used to drive a PECL input on an upstream circuit, such as, Signal Detect input or Loss of Signal-bar.
5	V_{CCR}	Receiver Power Supply Provide +5 Vdc via the recommended receiver power supply filter circuit. Locate the power supply filter circuit as close as possible to the V_{CCR} pin.
6	V_{CCT}	Transmitter Power Supply Provide +5 Vdc via the recommended transmitter power supply filter circuit. Locate the power supply filter circuit as close as possible to the V_{CCT} pin.
7	TD–	Transmitter Data In-Bar Terminate this high-speed differential PECL input with standard PECL techniques at the transmitter input pin.
8	TD+	Transmitter Data In Terminate this high-speed differential PECL input with standard PECL techniques at the transmitter input pin.
9	V_{EET}	Transmitter Signal Ground Directly connect this pin to the transmitter signal ground plane.

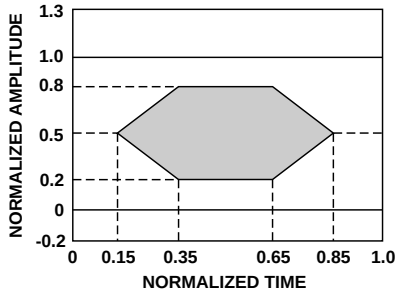


Figure 2. Transmitter Optical Eye Diagram Mask.

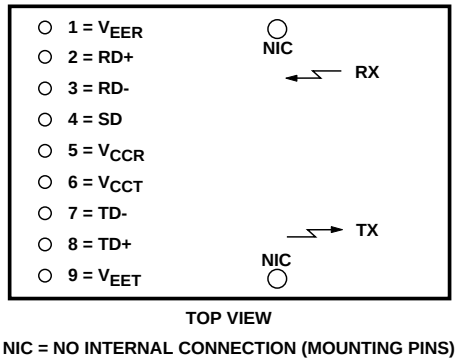


Figure 3. Pin-out.

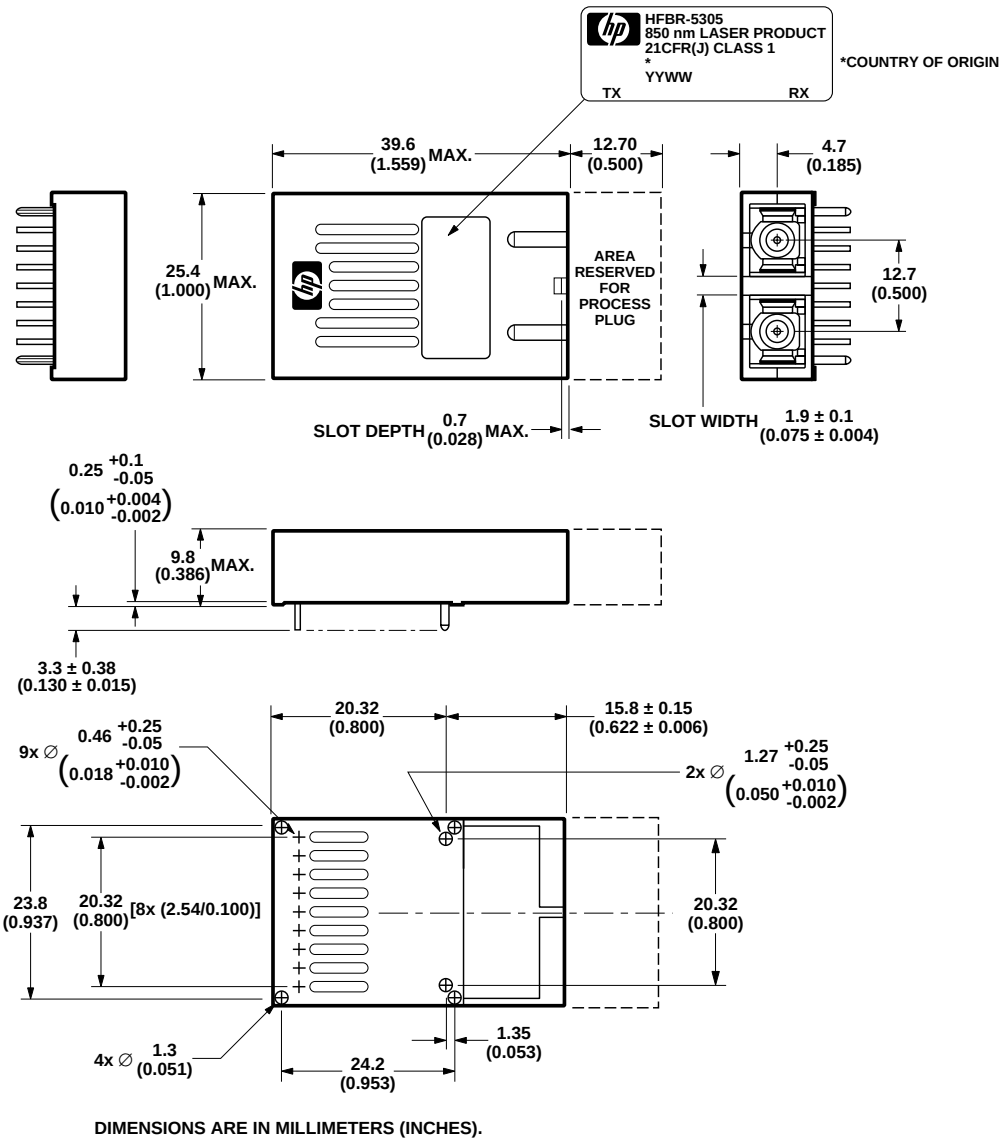
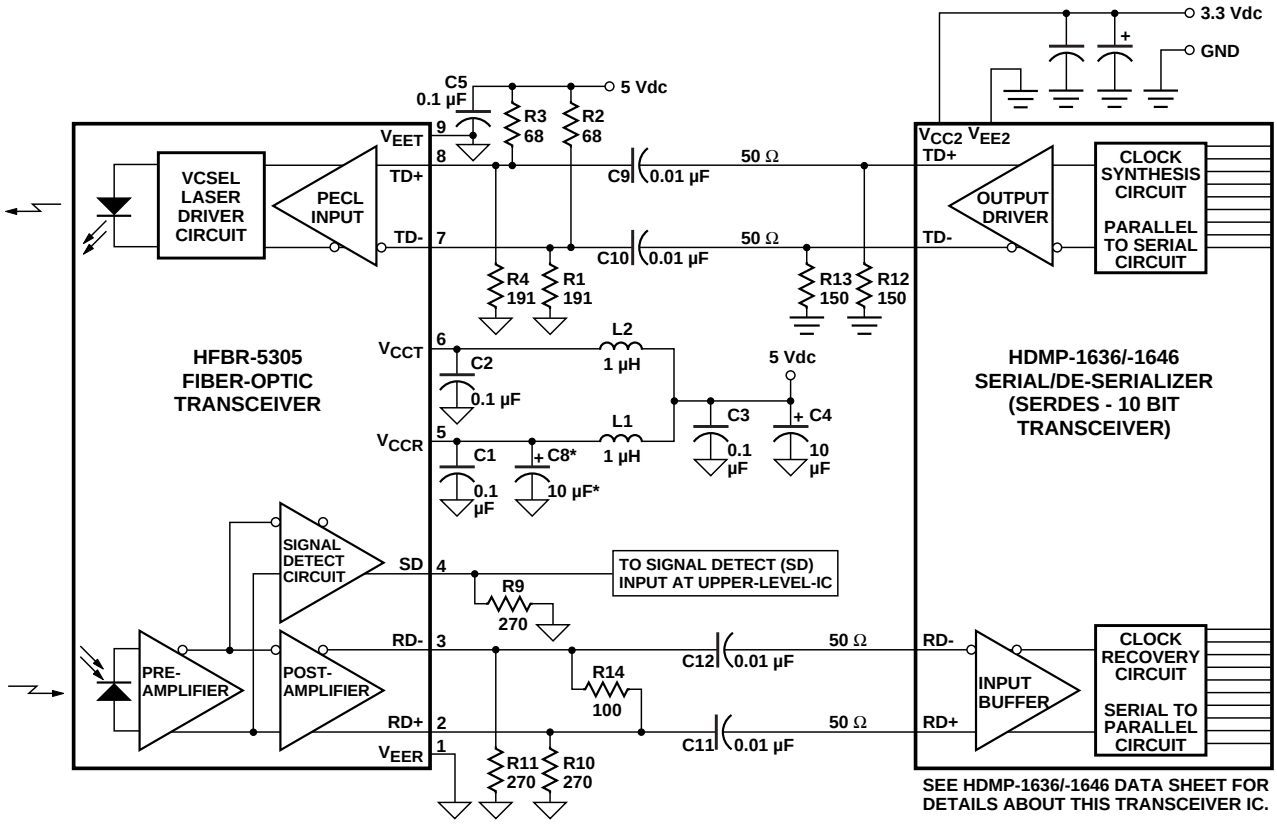
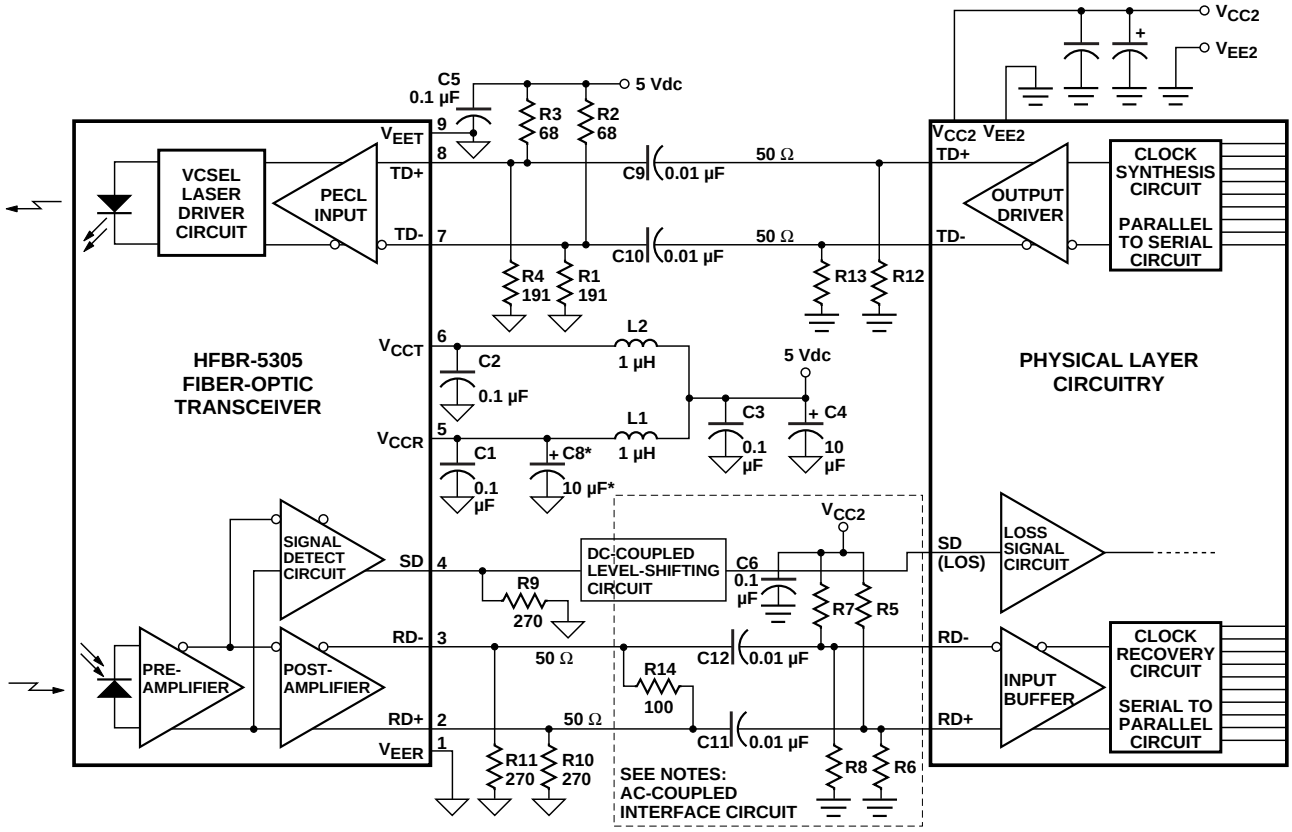


Figure 5. Package Outline Drawing and Pinout.



NOTES:
*C8 IS AN OPTIONAL BYPASS CAPACITOR FOR ADDITIONAL LOW-FREQUENCY NOISE FILTERING.
USE SURFACE-MOUNT COMPONENTS FOR OPTIMUM HIGH-FREQUENCY PERFORMANCE.
USE 50 Ω MICROSTRIP OR STRIPLINE FOR SIGNAL PATHS.
LOCATE 50 Ω TERMINATIONS AT THE INPUTS OF RECEIVING UNITS.

Figure 6. Recommended Gigabit/sec Ethernet HFBR-5305 Fiber-Optic Transceiver and HDMP-1636/-1646 SERDES Integrated Circuit Transceiver Interface and Power Supply Filter Circuits.



NOTES:
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USE SURFACE-MOUNT COMPONENTS FOR OPTIMUM HIGH-FREQUENCY PERFORMANCE.
USE 50 Ω MICROSTRIP OR STRIPLINE FOR SIGNAL PATHS.
LOCATE 50 Ω TERMINATIONS AT THE INPUTS OF RECEIVING UNITS.

AC-COUPLE INTERFACE CIRCUITS:

WITH THIS AC-COUPLED INTERFACE CIRCUIT, TERMINATION RESISTORS R5 & R6, AS WELL AS R7 & R8, MUST PROVIDE THEVENIN EQUIVALENT IMPEDANCE OF 50 Ω AND AN APPROPRIATE MID-SIGNAL BIAS VOLTAGE. FOUR APPLICATION EXAMPLES ARE GIVEN BELOW.

1. FOR 5 Vdc TO 3.3 Vdc PECL INTERFACE APPLICATIONS WHERE NO MID-SIGNAL BIAS VOLTAGE (V_{CC} - 1.3 V = 2 V) IS PROVIDED BY THE PHYSICAL LAYER IC INTERNAL INPUT CIRCUIT, THEN

R5 = R7 = 82 Ω
R6 = R8 = 130 Ω
R12 = R13 = 150 Ω
R14 IS NOT USED.

2. FOR 5 Vdc TO 3.3 Vdc PECL INTERFACE APPLICATIONS WHERE THE MID-SIGNAL BIAS VOLTAGE IS SUPPLIED BY THE PHYSICAL LAYER IC INTERNAL INPUT CIRCUIT, THEN R14 CAN BE USED FOR THE DIFFERENTIAL SIGNAL LOAD TERMINATION IN PLACE OF USING THE TWO RESISTOR SETS OF R5 & R6 AND R7 & R8 THAT ARE NO LONGER NECESSARY. THIS IS THE CASE WITH THE HDMP-1636/1646 FIBRE CHANNEL PHYSICAL LAYER INTEGRATED CIRCUITS. NOTE THAT THE HDMP-1636/1646 DO NOT HAVE A SIGNAL DETECT/RECEIVED LOSS OF SIGNAL INPUT. INSTEAD, SIGNAL DETECT CAN CONNECT TO AN UPSTREAM PROTOCOL CIRCUIT.

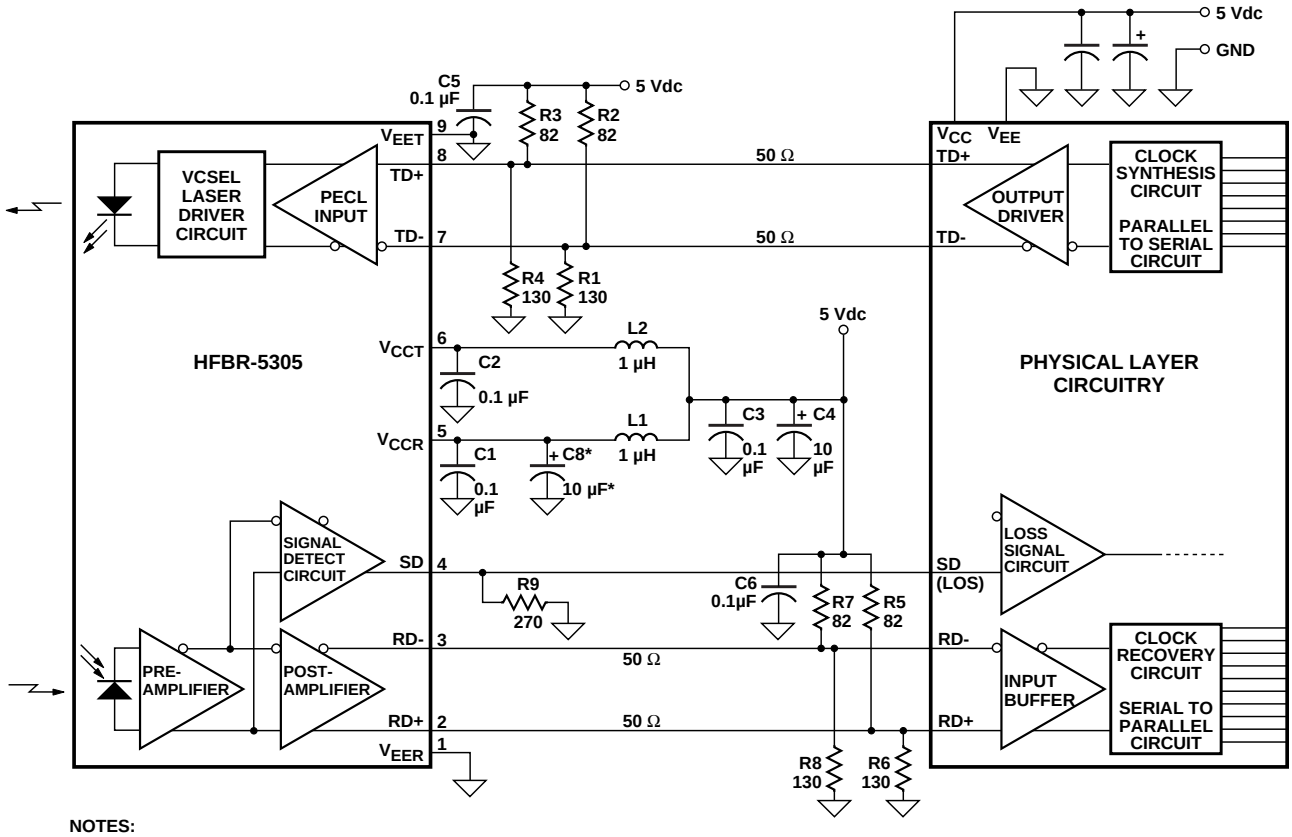
R5 = R6 = R7 = R8 = OPEN (NOT USED)
R12 = R13 = 150 Ω
R14 = 100 Ω.

3. FOR 5 Vdc TO -5.2 Vdc ECL INTERFACE APPLICATIONS (V_{CC2} = 0 Vdc, V_{EE2} = -5.2 Vdc) WHERE THE MID-SIGNAL BIAS VOLTAGE IS -1.3 Vdc (V_{CC} -1.3 V), THEN,

R5 = R7 = 68 Ω
R6 = R8 = 191 Ω
R12 = R13 = 270 Ω
R14 IS NOT USED.

4. FOR BIT-ERROR-RATIO TESTER (BERT) OR HIGH-SPEED SAMPLING OSCILLOSCOPE EQUIPMENT INTERFACE APPLICATIONS, HFBR-5305 OUTPUT SIGNALS VIA C11 AND C12 CAN BE CONNECTED DIRECTLY TO THE EQUIPMENT 50 Ω INPUTS THAT ARE REFERENCED TO GROUND. OMIT RESISTORS R5, R6, R7, R8, AND R14. BERT SOURCING SIGNALS TO THE HFBR-5305 WILL NEED THE AC-COUPLED NETWORK SETS OF C10, R1 & R2 AND C9, R3 & R4.

Figure 7. Gigabit/sec Ethernet HFBR-5305 AC-Coupled Interface Circuit for 3.3 V PECL, -5.2 V ECL or Ground-Referenced Test Instrumentation.



NOTES:
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USE SURFACE-MOUNT COMPONENTS FOR OPTIMUM HIGH-FREQUENCY PERFORMANCE.
USE 50 Ω MICROSTRIP OR STRIPLINE FOR SIGNAL PATHS.
LOCATE 50 Ω TERMINATIONS AT THE INPUTS OF RECEIVING UNITS.

TERMINATION RESISTORS R5 & R6, AS WELL AS R7 & R8, MUST PROVIDE THEVENIN EQUIVALENT IMPEDANCE OF 50 Ω AND THE APPROPRIATE PULL-DOWN BIAS VOLTAGE OF 3 Vdc (V_{CC} - 2 V) .

Figure 8. Gigabit/sec Ethernet Fiber-Optic Transceiver HFBR-5305 +5 Vdc PECL to +5 Vdc PECL Physical Layer Interface Circuit.

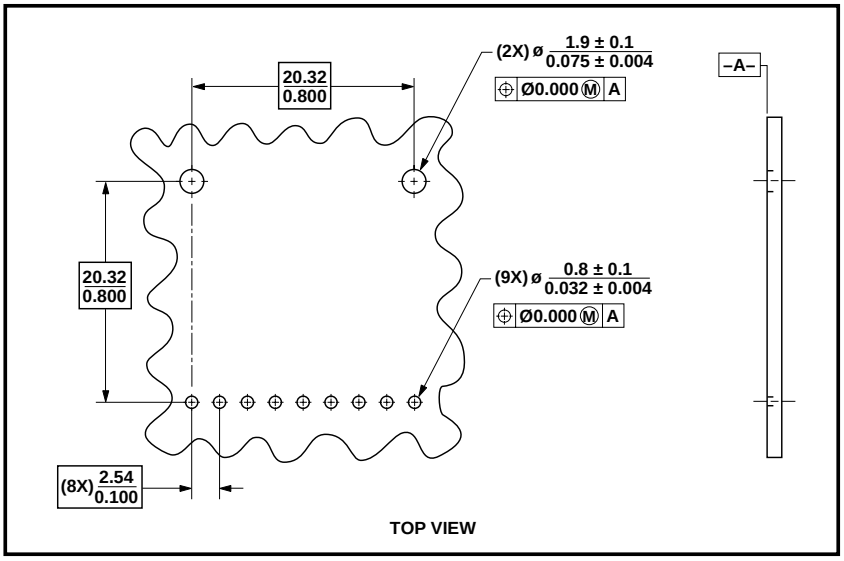

Figure 9. Recommended Board Layout Hole Pattern.