PRELIMINARY

HYUNDAI SEMICONDUCTOR

HY62C64

8192×8-Bit CMOS Static RAM

NOVEMBER 1986

DESCRIPTION

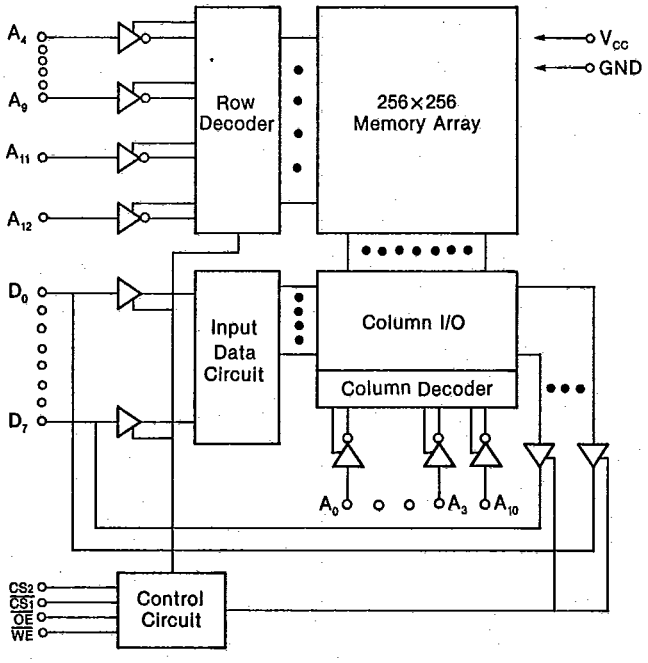
The HYUNDAI HY62C64 is a 65, 536-bit static random access memory organized as 8192 words by 8 bits and operates from a single 5 volt supply. It is built with HYUNDAI's high performance HYCMOS process. Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures. The HY62C64 is moulded in a standard 28-pin, 600 mil-DIP.

	HY62C64/L-45	HY62C64/L-55	HY62C64/L-70
Maximum Access Time (ns)	45	55	70
Maximum Average Operating Current (mA)	90	90	90
Maximum Standby Current (mA)	2/0.1	2/0.1	2/0.1

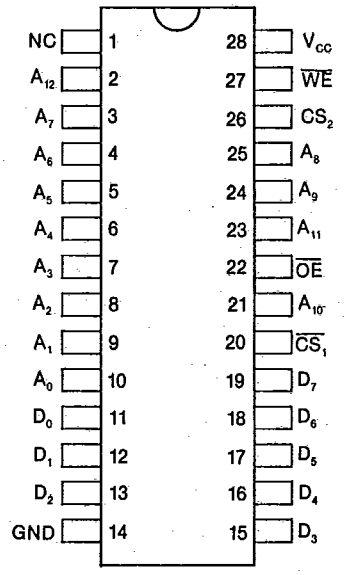
FEATURES

- ▲High-speed—45/55/70ns (Max.)
- ▲Low Power dissipation
  - –300mW (Typ.) Operating
  - –10μW (Typ.) Standby—HY62C64L
- ▲Single 5V power supply
- ▲Fully static operation
- ▲All inputs and outputs directly TTL compatible
- ▲Three State Outputs
- ▲Data retention supply voltage: 2.0-5.5V

BLOCK DIAGRAM



PIN CONNECTIONS



PIN NAMES

A_0-A_{12}	ADDRESS	$\overline{WE}$	WRITE ENABLE
D_0-D_7	DATA INPUT/OUTPUT	$\overline{OE}$	OUTPUT ENABLE
$\overline{CS_1}$	CHIP SELECT ONE	CS_2	CHIP SELECT TWO
V_{CC}	POWER	GND	GROUND

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ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_{BIAS}	Temperature Under Bias	-10 to +125	°C
T_{STG}	Storage Temperature	-40 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	20	mA

RECOMMENDED DC OPERATING CONDITIONS

(T_A=0°C to +70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	3.5	6.0	V
V_{IL}	Input Low Voltage	-0.5	0	0.8	V

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TRUTH TABLE

MODE	$\overline{WE}$	$\overline{CS_1}$	CS_2	$\overline{OE}$	I/O OPERATION	V_{CC} CURRENT	NOTE
Not Selected (Power Down)	X	H	X	X	High-Z	I_{SB}, I_{SB1}	
	X	X	L	X	High-Z	I_{SB}, I_{SB2}	
Output Disabled	H	L	H	H	High-Z	I_{CC}, I_{CC1}	
Read	H	L	H	L	D_{OUT}	I_{CC}, I_{CC1}	
Write	L	L	H	H	D_{IN}	I_{CC}, I_{CC1}	Write Cycle (1)
	L	L	H	L	D_{IN}	I_{CC}, I_{CC1}	Write Cycle (2)

CAPACITANCE[1]

(T_A=25°C, f=1.0MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	6	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$=0V	8	pF

1. This parameter is sampled and not 100% tested.

AC TEST CONDITIONS

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5ns
Input and Output	1.5V
Timing Reference Level Output Load	1 TTL Gate and C_L=30pF (including scope and jig)

DC ELECTRICAL CHARACTERISTICS

(V_{CC}=5V±10%, T_A=0°C to +70°C)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.[1]	MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{IN}=GND to V_{CC}		—	—	2	μA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS_1}$=V_{IH} or CS_2=V_{IL} or $\overline{OE}$=V_{IH}, $V_{I/O}$=GND to V_{CC}		—	—	2	μA
I_{CC}	Operating Power Supply Current	$\overline{CS_1}$=V_{IL}, CS_2=V_{IH}, $I_{I/O}$=0mA		—	50	90	mA
I_{CC1}	Average Operating Current	Min. Duty Cycle=100%, $\overline{CS_1}$=V_{IL}, CS_2=V_{IH}		—	60	90	mA
I_{SB}	Standby Power Supply Current	$\overline{CS_1}$=V_{IH} or CS_2=V_{IL}, $I_{I/O}$=0mA		—	5	15	mA
I_{SB1}[2]		$\overline{CS_1}$≥V_{CC}-0.2V, V_{IN}≥V_{CC}-0.2V or V_{IN}≤0.2V	HY62C64	—	0.02	2	mA
			HY62C64 L	—	2	100	μA
I_{SB2}[2]		CS_2≤0.2V, V_{IN}≥V_{CC}-0.2V or V_{IN}≤0.2V	HY62C64	—	0.02	2	mA
			HY62C64 L	—	2	100	μA
V_{OL}	Output Voltage	I_{OL}=2.1mA		—	—	0.4	V
V_{OH}		I_{OH}=-1.0mA		2.4	—	—	V

1. Typical limits are at V_{CC}=5.0V, T_A=25°C and specified loading 2. V_{IL} min=-0.3V

AC ELECTRICAL CHARACTERISTICS

(V_{CC}=5V±10%, T_A=0°C to+70°C)

READ CYCLE

SYMBOL	PARAMETER		HY62C64/L-45		HY62C64/L-55		HY62C64/L-70		UNIT
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time		45	—	55	—	70	—	ns
t_{AA}	Address Access Time		—	45	—	55	—	70	ns
t_{ACS1}	Chip Select Access Time	$\overline{CS_1}$	—	45	—	55	—	70	ns
t_{ACS2}		CS_2	—	45	—	55	—	70	ns
t_{OE}	Output Enable to Output Valid		—	30	—	35	—	50	ns
t_{CLZ1}	Chip Selection to Output in Low-Z	$\overline{CS_1}$	5	—	5	—	5	—	ns
t_{CLZ2}		CS_2	5	—	5	—	5	—	ns
t_{OLZ}	Output Enable to Output in Low-Z		5	—	5	—	5	—	ns
t_{CHZ1}	Chip Deselection to Output in High-Z	$\overline{CS_1}$	0	25	0	30	0	35	ns
t_{CHZ2}		CS_2	0	25	0	30	0	35	ns
t_{OHZ}	Output Disable to Output in High-Z		0	25	0	30	0	35	ns
t_{OH}	Output Hold from Address Change		5	—	5	—	5	—	ns

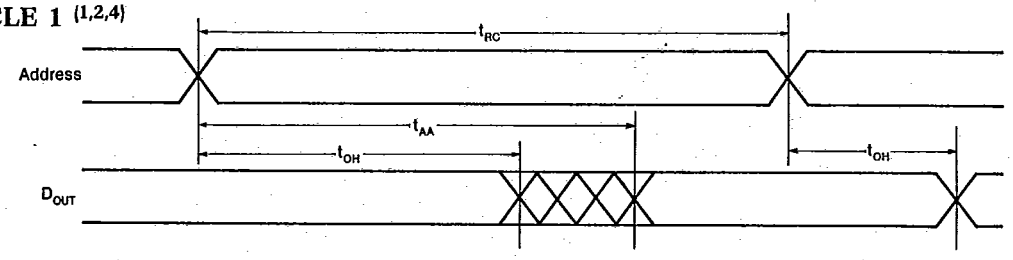
WRITE CYCLE

SYMBOL	PARAMETER		HY62C64/L-45		HY62C64/L-55		HY62C64/L-70		UNIT
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time		45	—	55	—	70	—	ns
t_{CW}	Chip Selection to End of Write		35	—	40	—	45	—	ns
t_{AS}	Address Setup Time		5	—	5	—	5	—	ns
t_{AW}	Address Valid to End of Write		40	—	50	—	65	—	ns
t_{WP}	Write Pulse Width		35	—	40	—	45	—	ns
t_{WR1}	Write Recovery Time	$\overline{CS_1}$, $\overline{WE}$	5	—	5	—	5	—	ns
t_{WR2}		CS_2	5	—	10	—	10	—	ns
t_{WHZ}	Write to Output in High-Z		0	20	0	25	0	30	ns
t_{DW}	Data to Write Time Overlap		20	—	25	—	30	—	ns
t_{DH}	Data Hold from Write Time		5	—	5	—	5	—	ns
t_{OHZ}	Output Enable to Output in High-Z		0	25	0	25	0	25	ns
t_{OW}	Output Active from End of Write		5	—	5	—	5	—	ns

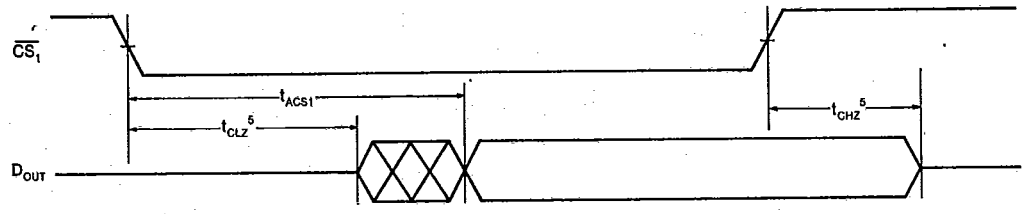
NOTES: t_{CHZ}, t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

TIMING DIAGRAM

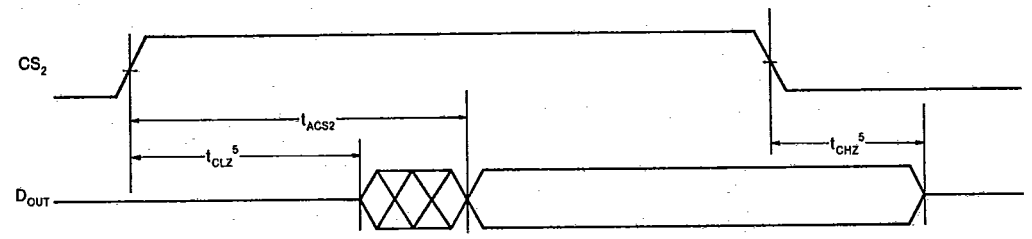
READ CYCLE 1 (1,2,4)



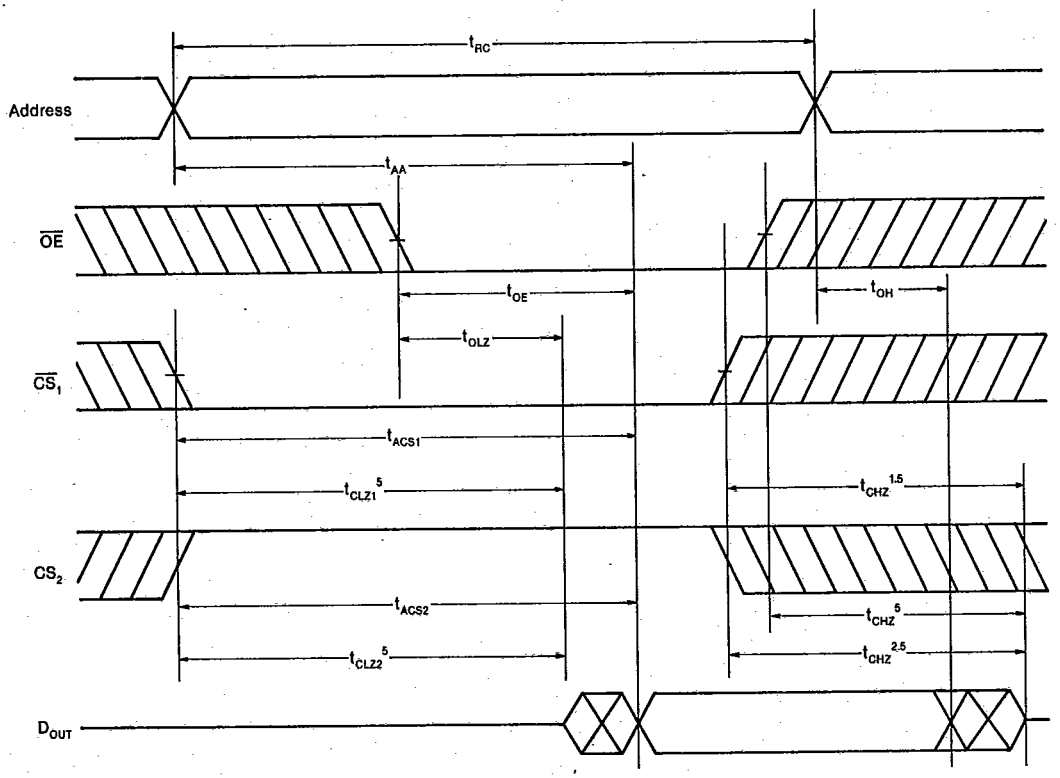
READ CYCLE 2[1,3,4,6]



READ CYCLE 3[1,4,7]



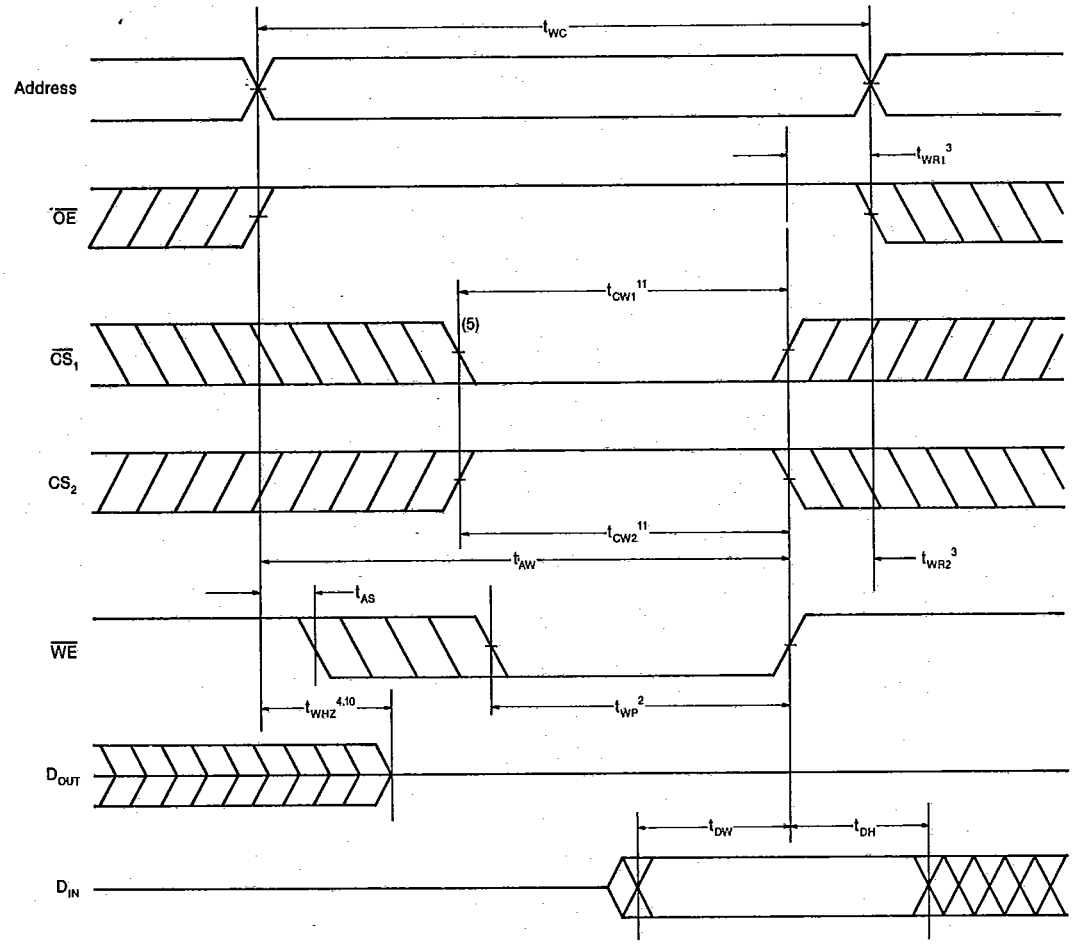
READ CYCLE 4[1]



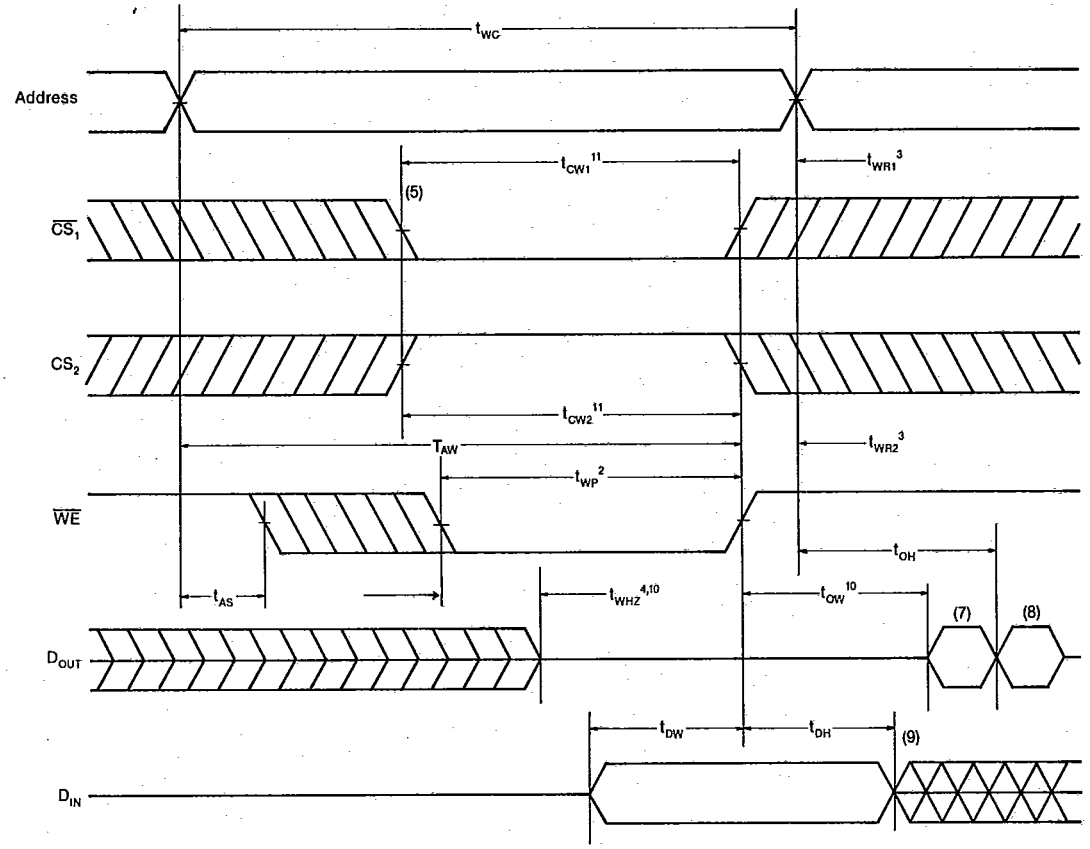
NOTES:
1. $\overline{WE}$ is high for READ cycle.
2. Device is continuously selected $\overline{CS_1}$=V_{IL} and CS_2=V_{IH}.
3. Address valid prior to or coincident with $\overline{CS_1}$ transition low.
4. $\overline{OE}$=V_{IL}.
5. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.
6. CS_2 is high.
7. $\overline{CS_1}$ is low.

TIMING DIAGRAM (CONT'D)

WRITE CYCLE 1[1]



WRITE CYCLE 2[1,6]



NOTES:

1. $\overline{WE}$ must be high during address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS_1}$, a high CS_2 and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS_1}$ or $\overline{WE}$ going high or CS_2 going low to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS_1}$ low transition or the CS_2 high transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE}$=V_{IL}).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{CS_1}$ is low and CS_2 is high during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.
11. t_{CW} is measured from the later of $\overline{CS_1}$ going low or CS_2 going high to the end of write.

DATA RETENTION CHARACTERISTICS

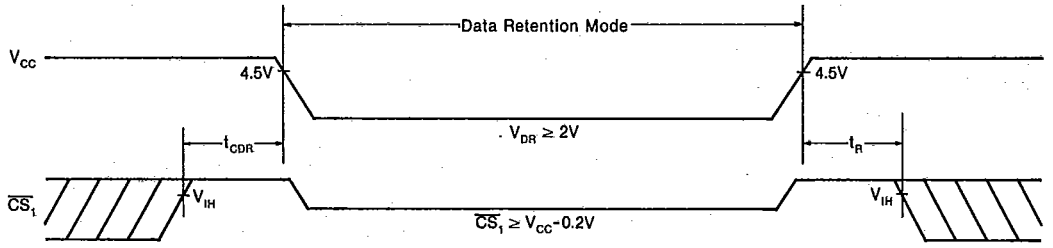
(T_A = 0°C to +70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.[1]	MAX.	UNIT
V_{DR1}	V_{CC} for Data Retention	$\overline{CS_1} \geq V_{CC}-0.2V$, $V_{IN} \geq V_{CC}-0.2V$ or $V_{IN} \leq 0.2V$	2.0	—	—	V
V_{DR2}		$CS_2 \leq 0.2V$, $V_{IN} \geq V_{CC}-0.2V$ or $V_{IN} \leq 0.2V$	2.0	—	—	V
I_{CCDR1}	Data Retention Current	$\overline{CS_1} \geq V_{CC}-0.2V$, $V_{IN} \geq V_{CC}-0.2V$ or $V_{IN} \leq 0.2$	—	2	50	μA
I_{CCDR2}		$CS_2 \leq 0.2V$, $V_{IN} \geq V_{CC}-0.2V$ or $V_{IN} \leq 0.2V$	—	2	50	μA
t_{CDR}	Chip Deselect to Data Retention Time	See Retention Diagram	0	—	—	ns
t_R	Operation Recovery Time		t_{RC}[2]	—	—	ns

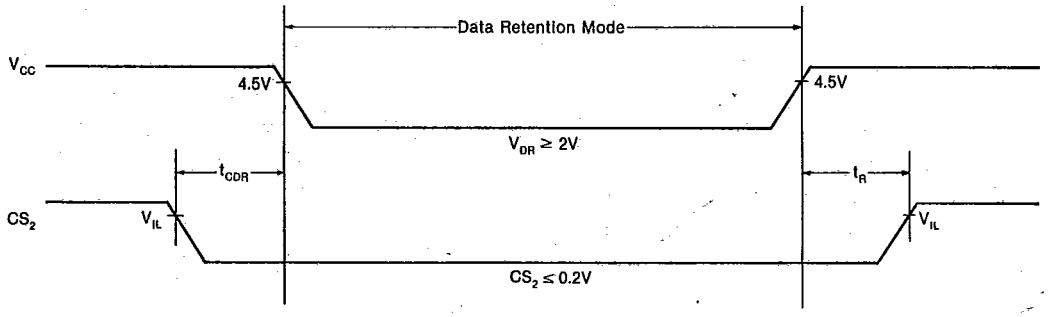
NOTES:

1. V_{CC} = 2V, T_A = +25°C
2. t_{RC} = Read Cycle Time

LOW V_{CC} DATA RETENTION DIAGRAM 1 ($\overline{CS_1}$ Controlled)



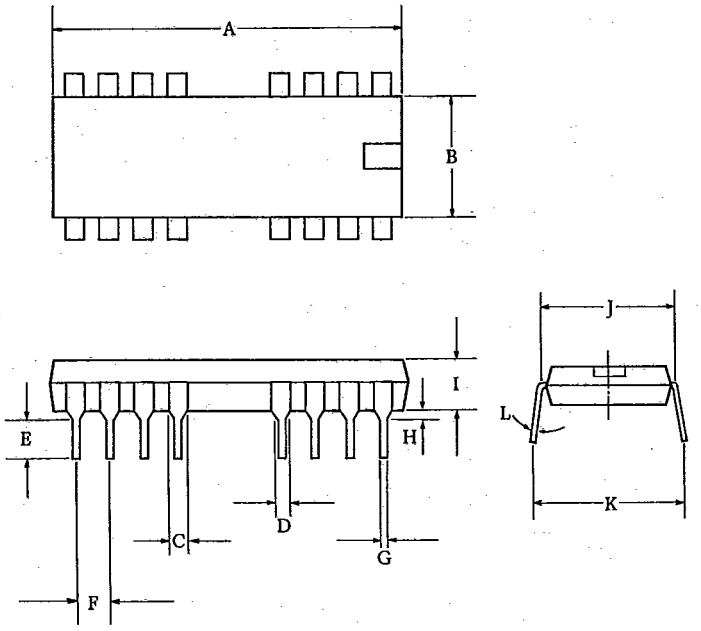
Low V_{CC} DATA RETENTION DIAGRAM 2 (CS_2 Controlled)



PACKAGE OUTLINE

28 PIN PLASTIC

DIM	Inches			Millimeters		
	Min	Typ	Max	Min	Typ	Max
A	1.445		1.455	36.703		36.957
B	0.535		0.545	13.685		13.843
C		0.060			1.524	
D		0.032			0.813	
E	0.125			3.175		
F	0.090		0.110	2.286		2.794
G	0.016		0.020	0.406		0.508
H	0.020			0.508		
I	0.150			3.810		
J			0.625			15.875
K			0.700			17.780
L		0.010			0.254	



ORDERING INFORMATION

Part Number: HY62C64/L XXX

Speed
45=45ns
55=55ns
70=70ns

Package
P: Plastic DIP

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