KM28C64A/KM28C65A CMOS EEPROM

8K×8 Bit CMOS Electrically Erasable PROM

FEATURES

- **Operating Temperature Range**
  - **KM28C64A/65A: Commercial**
  - **KM28C64AI/65AI: Industrial**
- **Simple Byte Write & Page Write**
  - **Single TTL Level Write Signal**
  - **Internal Address and Data Latch**
  - **Automatic Internal Erase-Before-Write**
  - **Ready/$\overline{\text{Busy}}$ Output Pin (KM28C65A)**
- **Fast Write Cycle Time**
  - **64-Byte Page Write Operation**
  - **5ms Byte and Page Write Cycle Time**
  - **Complete Memory Rewrite: 0.7 seconds**
- **$\overline{\text{Data}}$-Polling and Toggle bit for End of Write Detection**
- **Single 5 volt Supply**
- **Fast Access Time: 120ns**
- **Power: 100μA—Standby (max.)**
  40mA—Operating (max.)
- **Hardware and Software Data Protection**
- **Reliable CMOS Floating-Gate Technology**
  - **Endurance: 100,000 Cycle**
  - **Data Retention: 10 years**
- **JEDEC Byte-wide Memory Pinout**

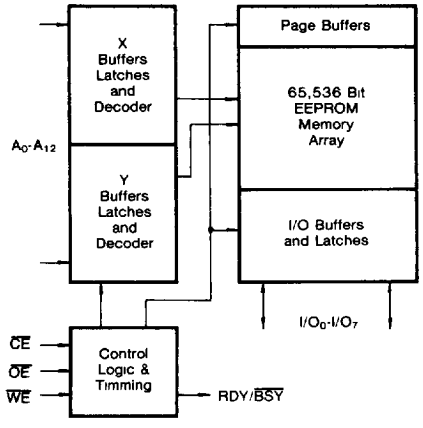
GENERAL DESCRIPTION

The KM28C64A/65A is a 8,192×8 bit Electrically Erasable Programmable Read Only Memory. It is fabricated with the floating-gate CMOS technology using Fowler-Nordheim tunneling for erasing and programming.

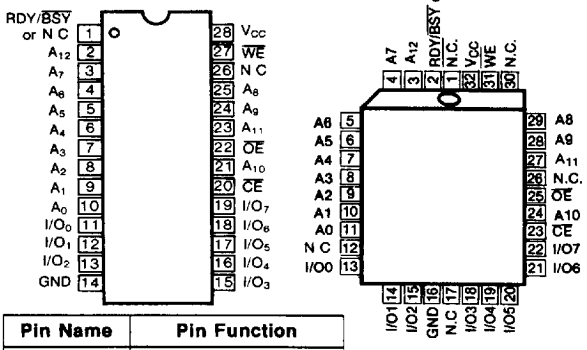
Writing data into the KM28C64A/65A is very simple. The internally self-timed writing cycle latches both address and data to provide a free system bus during the 5ms write period A 64-byte page write enables an entire chip written in 0.7 seconds.

The KM28C64A/65A also features $\overline{\text{Data}}$-polling and a Toggle bit schemes that signal the processor the early completion of a write cycle without requiring any external hardware. The KM28C65A features Read/$\overline{\text{Busy}}$ which is a hardware scheme to signal the status of the write operation and is especially useful in interrupt driven systems.
The KM28C64A/65A is designed for applications up to 100,000 write cycles per byte. It's on-chip Error Checking and Correction scheme improves the endurance to over 100,000 write cycles.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{12}	Address Inputs
I/O_0-I/O_7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
RDY/$\overline{BSY}$	Ready/$\overline{\text{Busy}}$ Output
N.C.	No Connection
V_{CC}	+5V
GND	Ground

SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS*

Parameter		Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}		V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	Com.	T_{bias}	−10 to +125	°C
	Ind.		−65 to +150	°C
Storage Temperature		T_{stg}	−65 to +150	°C
Short Circuit Output Current		I_{OS}	5	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

KM28C64A/65A : Voltage reference to V_{SS}, T_A=0°C to +70°C
KM28C64AI/65AI : Voltage reference to V_{SS}, T_A=−40°C to +85°C

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{CE}=\overline{OE}=V_{IL}$, $\overline{WE}=V_{IH}$, all I/O's open (Note 1)	—	40	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE}=V_{IH}$, all I/O's = open	—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE}=V_{CC}-0.2$, all I/O's = open	—	100	μA
Input Leakage Current	I_{LI}	V_{IN} = 0 to 5.5V	—	10	μA
Output Leakage Current	I_{LO}	V_{OUT} = 0 to 5.5V	—	10	μA
Input High Voltage, all Inputs	V_{IH}		2.0	$V_{CC}+0.3$	V
Input Low Voltage, all Inputs	V_{IL}		−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH}=-400\mu A$	2.4	—	V
Output Low Voltage Level	V_{OL}	I_{OL} = 2.1mA	—	0.4	V
Write Inhibit V_{CC} Level	V_{WI}		3.0	—	V

Note 1: All address toggling from V_{IL} to V_{IH} at 8.4MHz.

CAPACITANCE (T_A=25°C, f=1.0 MHz))

Item	Symbol	Conditions	Min	Max	Unit
Input/Output Capacitance	$C_{I/O}$	V_{IL}=0V	—	10	pF
Input Capacitance	C_{IN}	V_{IN}=0V	—	6	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
L	L	H	$\overline{Data}$ Polling	$I/O_7=\overline{D_7}$	Active
			Toggle Bit	I/O_6	Active
H	X	X	Standby and Write Inhibit	High-Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

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AC CHARACTERISTICS

KM28C64A/65A : T_A=0°C to +70°C V_{CC}=5V±10%, unless otherwise noted
KM28C64AI/65AI: T_A=−40°C to +85°C V_{CC}=5V±10%, unless otherwise noted

TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0.45V to 2.4V
Input Rise and Fall Times	20ns
Input and Output Timing measurement Levels	0 8V and 2.0V
Output Load	1 TTL Gate and C_L=100pF

READ CYCLE

Parameter	Symbol	KM28C64A-12 KM28C65A-12		KM28C64A-15 KM28C64AI-15 KM28C65A-15 KM28C65AI-15		KM28C64A-20 KM28C64AI-20 KM28C65A-20 KM28C65AI-20		KM28C64A-25 KM28C64AI-25 KM28C65A-25 KM28C65AI-25		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	120		150		200		250		ns
Chip Enable Access Time	t_{CE}		120		150		200		250	ns
Address Access Time	t_{AA}		120		150		200		250	ns
Output Enable Access Time	t_{OE}		60		80		100		120	ns
Output or Chip Disable to Output High-Z	t_{DF}	0	50	0	50	0	50	0	50	ns
Output Hold from Address Change	t_{OH}	0		0		0		0		ns

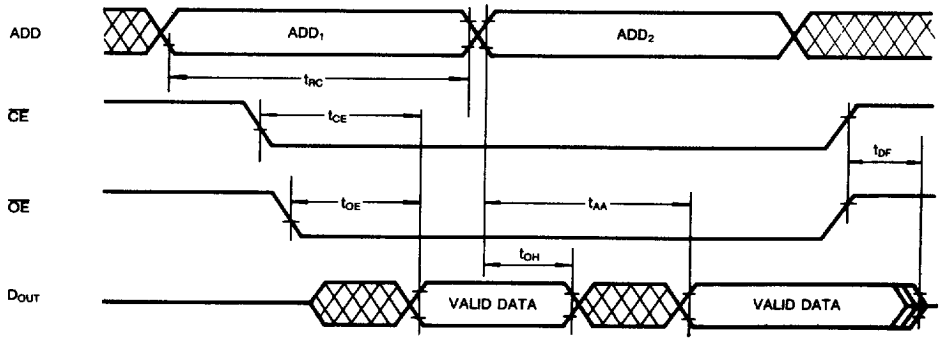
WRITE CYCLE

Parameter	Symbol	Min	Max	Unit
Write Cycle Time	t_{WC}		5	ms
Address Set-Up Time	t_{AS}	0		ns
Address Hold Time	t_{AH}	80		ns
Write Set-Up Time	t_{CS}	0		ns
Write Hold Time	t_{CH}	0		ns
$\overline{CE}$ Pulse Width	t_{CW}	100		ns
Output Enable Set-Up Time	t_{OES}	10		ns
Output Enable Hold Time	t_{OEH}	10		ns
$\overline{WE}$ Pulse Width	t_{WP}	100		ns
Data Set-Up Time	t_{DS}	50		ns
Data Hold Time	t_{DH}	0		ns
Time to Device Busy	t_{DB}		100	ns
Busy to Write Recovery Time	t_{BWR}	50		ns
Byte Load Cycle Time	t_{BLC}	0.2	150	μs
Last Byte Loaded to $\overline{Data}$ Polling	t_{LP}		200	ns

Note: The timer for t_{BLC} is reset at a falling edge of $\overline{WE}$ and restarts at rising edge of $\overline{WE}$.

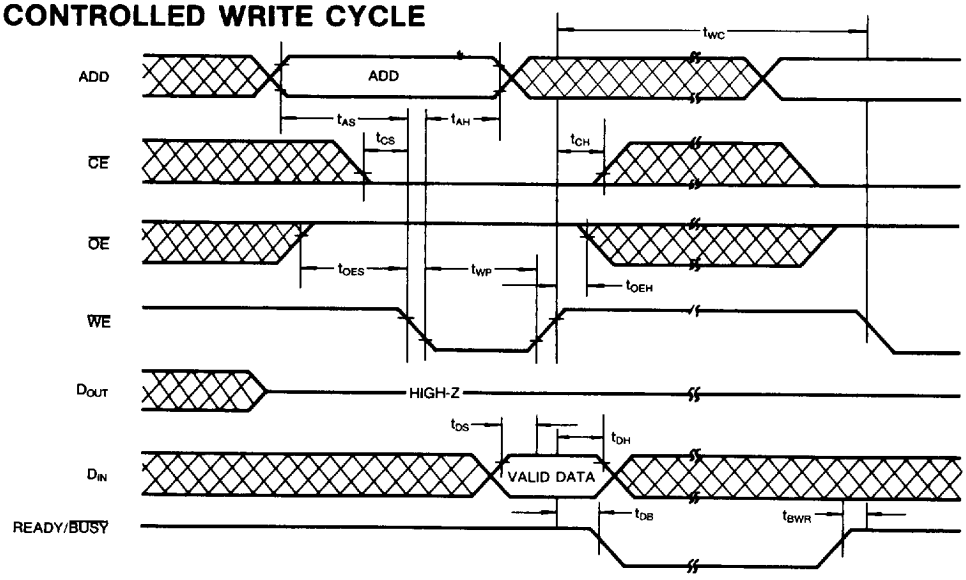
TIMING DIAGRAM

READ CYCLE ($\overline{WE}$=V_{IH})

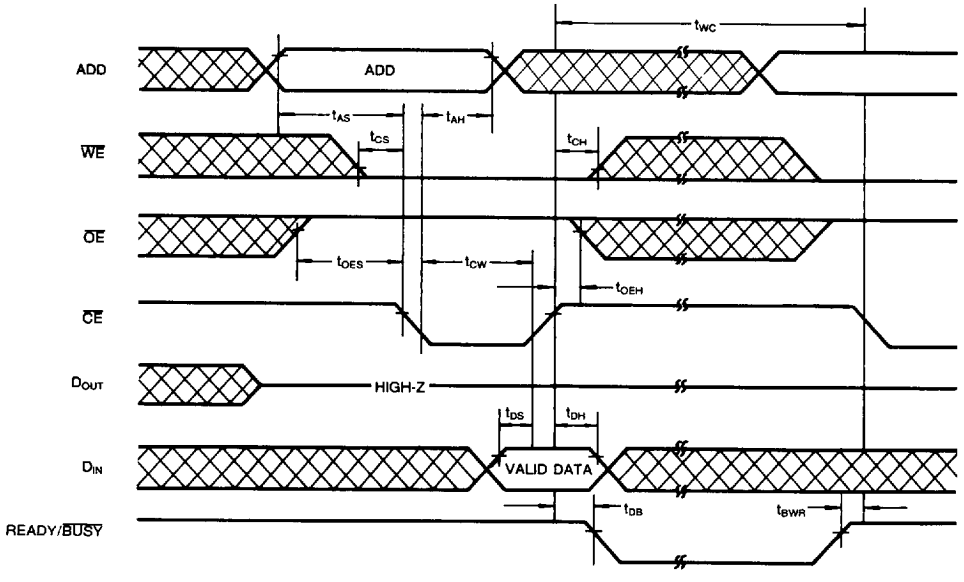


TIMING DIAGRAM (Continued)

$\overline{WE}$ CONTROLLED WRITE CYCLE

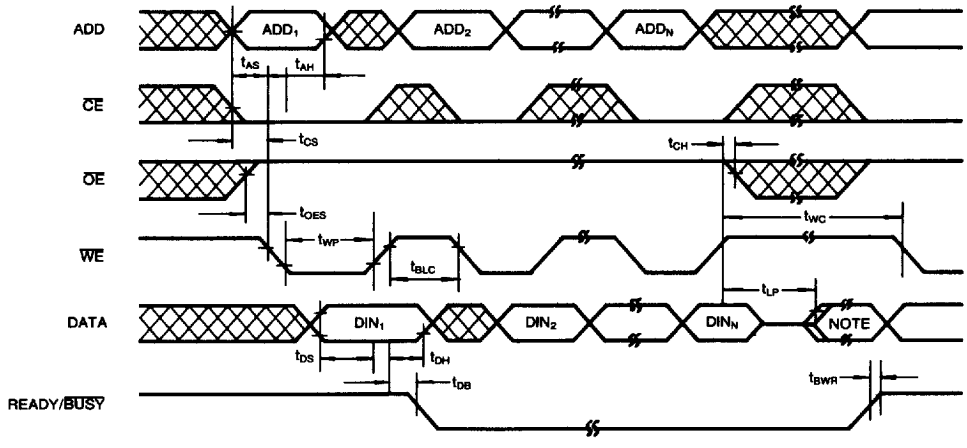


$\overline{CE}$ CONTROLLED WRITE CYCLE

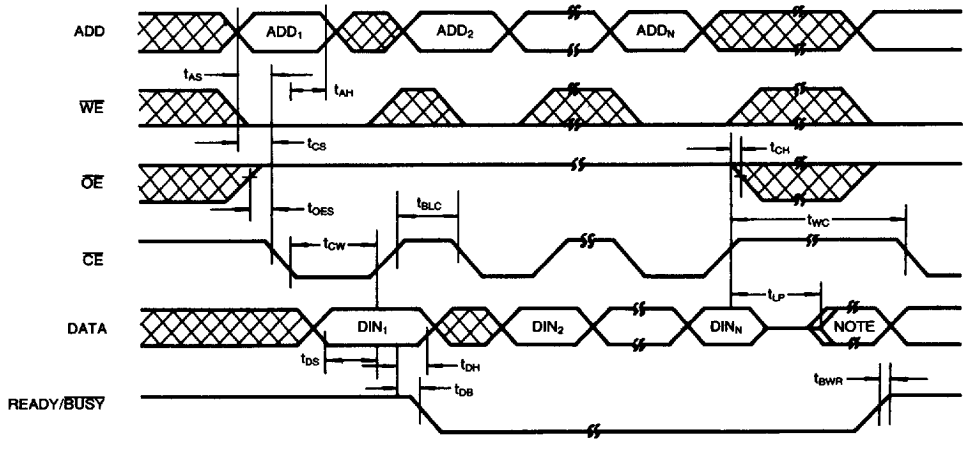


TIMING DIAGRAMS (Continued)

PAGE MODE WRITE ($\overline{WE}$ CONTROLLED WRITE CYCLE)



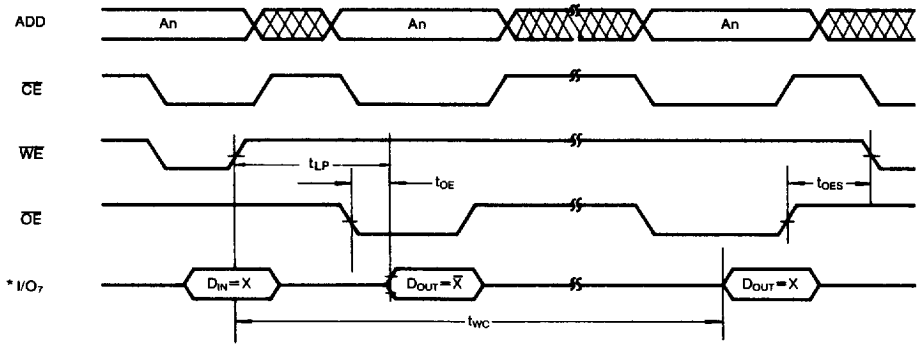
PAGE MODE WRITE ($\overline{CE}$ CONTROLLED WRITE CYCLE)



* NOTE: I/O_7 output $\overline{DIN_N}$ when the chip is read.
I/O_6 is toggling between "1" and "0" when the chip is successively read.

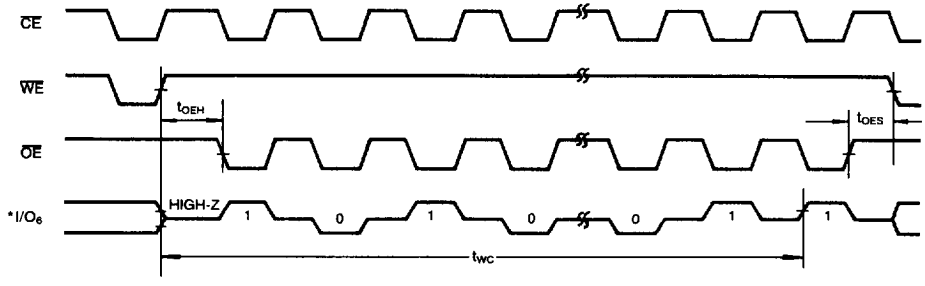
TIMING DIAGRAMS (Continued)

DATA POLLING CYCLE



* During the write cycle, I/O_7 will produce an inverted data of the last I/O_7 data, loaded into the EEPROM

TOGGLE BIT CYCLE



* During the write cycle, I/O_6 will toggle between "1" and "0".

DEVICE OPERATION

READ

Reading data from the KM28C64A/65A is similar to reading data from a SRAM. A read cycle occurs when $\overline{WE}$ is high and $\overline{CE}$ and $\overline{OE}$ are low. If either $\overline{CE}$ or $\overline{OE}$ goes high the read cycle is terminated. This two line control eliminates bus contention in a system environment. The DATA I/O pins are in the high impedance state whenever $\overline{OE}$ or $\overline{CE}$ is high.

WRITE

Writing data into the KM28C64A/65A is easy. Only a single 5V supply and TTL level signals are required. The on-chip data latches, address latches, high voltage generator, and fully self-timed control logic make writing as easy as writing to a SRAM.

**** BYTE WRITE MODE ****

The byte write mode of the KM28C64A/65A is only a part of the page write mode. A single byte data loading followed by a t_{BLC} time-out and by a nonvolitile write cycle will complete a byte mode write.

**** PAGE WRITE MODE ****

The KM28C64A/65A allows up to 64 bytes to be written in a single page write cycle. A page write cycle consists of a data loading period, in which from 1 to 64 bytes of data are loaded into the KM28C64A/65A internal registers and a nonvolatile write period, in which the loaded data in the registers are written to the EEPROM cells of the selected page.

Data is loaded into the KM28C64A/65A by sequentially pulsing $\overline{WE}$ with $\overline{CE}$ low and $\overline{OE}$ high. For each addressed location in the page, address is latched on the falling edge of the $\overline{WE}$ and data is latched on the rising edge of the $\overline{WE}$. The data can be loaded in any "Y" address (A_0-A_5) order (i.e. data need not be loaded into consecutive locations in memory in anypage) and can be renewed in a data loading period.

Since the timer for the data loading (t_{BLC}) is reset at the falling edge of $\overline{WE}$ and starts at every rising edge of $\overline{WE}$, the only requirement on $\overline{WE}$ to continue loding the data is that the interval between $\overline{WE}$ pulses dose not exceed the maximum t_{BLC} (150μs). If $\overline{OE}$ goes low during the data loading period, further attempt to load the data will be ignored because the external $\overline{WE}$ signal is blocked by $\overline{OE}$ signal internally. Consequently, the t_{BLC} timer is not reset by the external $\overline{WE}$ pulse if $\overline{OE}$ is low. The nonvolatile write starts if $\overline{WE}$ stays high for at least t_{BLC} maximum (150μs) after the last $\overline{WE}$ low to high transition. The page address for the nonvolatile write is the "X" address (A6-A12) latched on the last $\overline{WE}$. The nonvolatile write period consists of an erase cycle and a program cycle. During the erase cycle, the existing data of the locations being addressed are erased. the new data latched at the register are written into the location during the program cycle. Note that only the addressed location in a page are rewritten during a page write cycle.

The KM28C64A/65A also supports $\overline{CE}$ controlled write cycle. That means $\overline{CE}$ can be used to latch address and data as well as $\overline{WE}$.

STANDBY

Power comsumption is reduced to less than 100μA by deselecting the device with a high input on $\overline{CE}$. Whenever $\overline{CE}$ is high, the device is in the standby mode and I/O_0-I/O_7 are in the high impedance state, regardless of the state of $\overline{OE}$ or $\overline{WE}$.

DATA PROTECTION

Features have been designed into the KM28C64A/65A to prevent unwanted write cycles during power supply transitions and system noise periods.

The KM28C64A/65A has a protection feature against $\overline{WE}$ noises; a $\overline{WE}$ noise the width shorter than 20ns (typ.) will not start any unwanted write cycle. Write cycles are also inhibited when V_{CC} is less than V_{WI}=3.0 volts, the write inhibits V_{CC} level. During power-up, the KM28C64A/65A automatically prevents any write operation for a period of 5ms (typ.) after V_{CC} reaches the V_{WI} level. This will provide the system with sufficient time to bring $\overline{WE}$ and $\overline{CE}$ to a high level before a write can occur. Read cycles can be executed during this initialization period. Holding either $\overline{OE}$ low or $\overline{WE}$ high or $\overline{CE}$ high during power-on and power-off will inhibit inadvertent writes.

**** SOFTWARE DATA PROTECTION ****

The KM28C64A/65A has the JEDEC standard software data protection scheme for enhanced protection of stored data. The scheme does not affect normal write operation if it is not enabled through a SDP enable software algorithm, followed by a write or page write operation. Once the protection mode is enabled, the KM28C64A/65A will not write any data if the SDP enable software algorithm is not proceded. The data protection function can be disabled by exection a SDP disable software algorithm. Power transitions will not reset the SDP feature. All the data and address timings for the SDP enable and disable are identical to those of a page write cycle.

DEVICE OPERATION (Continued)

WRITE COMPLETION INDICATORS

*** $\overline{\text{DATA}}$ POLLING ***

The KM28C64A/65A features $\overline{\text{DATA}}$-Polling at I/O_7 to detect the completion of a write cycle using a simple read and compare operation. Such a scheme dose not require any external hardware. During the write period, any attempt to read of the last byte the EEPROM will produce, at I/O_7. an inverted inverted value of the last I/O_7 data loaded to the EEPROM. True data will be produced at all I/O's once the write cycle has been completed

*** TOGGLE BIT ***

The KM28C64A/65A also provides toggle bit at I/O_6 to determine the end of a write cycle. During the write cycle, subsequent attempts to read the EEPROM will toggle I/O_6 between "1" and "0". Once the write cycle is complete, the toggling will stop and valid data will be read.

*** READY/$\overline{\text{BUSY}}$ ***

The KM28C65A has a Ready/$\overline{\text{Busy}}$ output on pin 1 that indicates when the write cycle is complete. The pin is normally high except when a write cycle is in progress, in which case the pin is low. The Ready/$\overline{\text{Busy}}$ output is configured as an open-drain driver there-by allowing two or more Ready/$\overline{\text{Busy}}$ output to be OR-tied. This pin requires an appropriate pull-up resistor for proper operation. The pull-up resistor value maybe calculated as follows.

$$RP = \frac{V_{CC}(max) - V_{OL}(max)}{I_{OL} + \Sigma I_L} = \frac{5.1V}{2.1mA + \Sigma I_L}$$

where ΣI_L is the sum of the input currents of all devices tied to the Ready/$\overline{\text{Busy}}$ pin.

ENDURANCE AND DATA RETENTION

KM28C64A/65A is designed for applications requiring up to 100,000 write cycles per EEPROM byte and ten years of data retention. This means that each byte may be reliably written 100,000 times without degrading device operation. The device also featires an on-chip Error Checking and Correction scheme that can detect and correct any single bit failure in a byte, and hence, significant improvements in the endurance and data retention characteristics are achieved.

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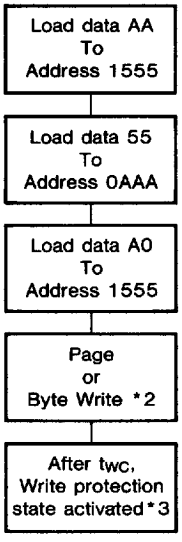
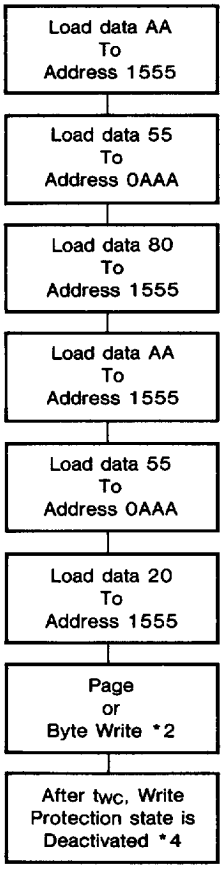
SOFTWARE DATA PROTECTION ALGORITHIM*1

SDP Enable Sequence



* Write mode enabled

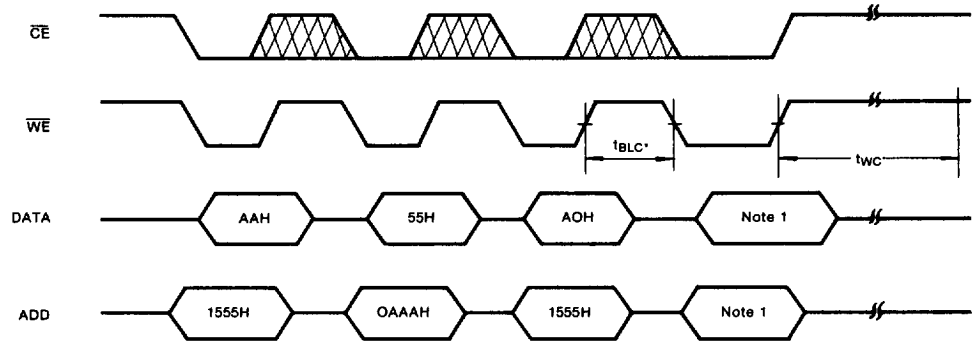
SDP Disable Sequance



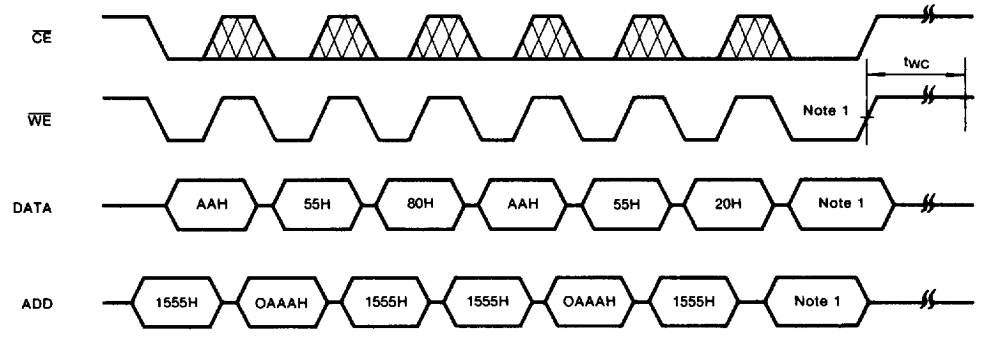
Note: 1. Data Format: I/O_7-I/O_0 (HEX)
Address Format: A_{12}-A_0 (HEX)
2. 1 to 64 byte of data may be loaded in random order.
3. Write protection state will be activated after t_{WC} even if no data is writtern.
4. Write protection state will be deactived after.

TIMING DIAGRAM OF SOFTWARE DATA PROTECTION

SDP ENABLE TIMING SEQUENCE



SDP DISABLE TIMING SEQUENCE



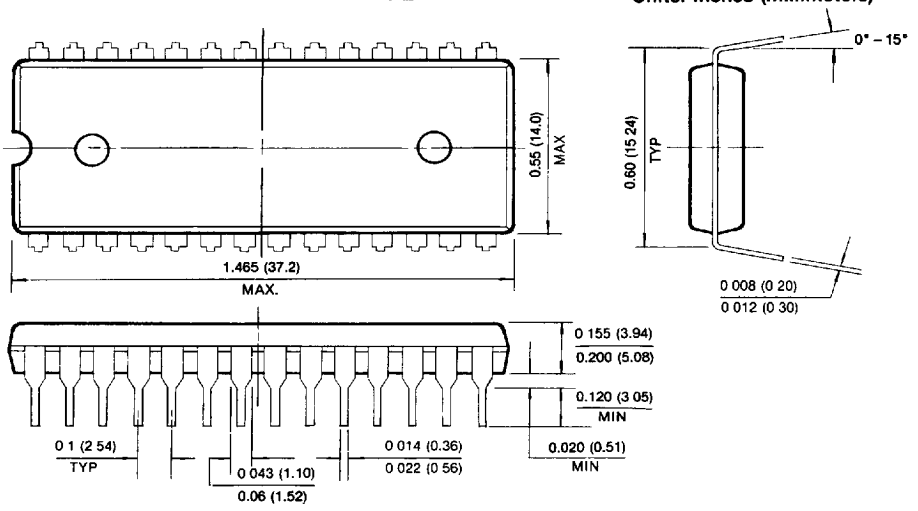
* $\leq t_{BLC}$ max.

Note 1: 1 to 64 byte of data maybe loaded in random order.

PACKAGE DIMENSIONS (Continued)

28 LEAD PLASTIC DUAL IN LINE PACKAGE

Units: Inches (millimeters)



32 PIN PLASTIC LEADED CHIP CARRIER