# **KPS Series, X7R Dielectric, 10VDC-250VDC** (Automotive Grade)



#### **Overview**

KEMET Power Solutions (KPS) Automotive Series stacked capacitors utilize a proprietary lead-frame technology to vertically stack one or two multilayer ceramic chip capacitors into a single compact surface mount package. The attached lead-frame mechanically isolates the capacitor/s from the printed circuit board, therefore offering advanced mechanical and thermal stress performance. Isolation also addresses concerns for audible, microphonic noise that may occur when a bias voltage is applied. A two chip stack offers up to double the capacitance in the same or smaller design footprint when compared to traditional surface mount MLCC devices. Providing up to 10mm of board flex capability, KPS Series capacitors are environmentally friendly and in compliance with RoHS legislation. Available in X7R dielectric, these devices are capable of Pb-Free reflow profiles and provide

lower ESR, ESL and higher ripple current capability when compared to other dielectric solutions.

Combined with the stability of an X7R dielectric, KEMET's KPS Series devices exhibit a predictable change in capacitance with respect to time and voltage and boast a minimal change in capacitance with reference to ambient temperature. Capacitance change is limited to ±15% from -55°C to +125°C.

KPS Series automotive grade capacitors meet the demanding Automotive Electronics Council's AEC-Q200 qualification requirements and are manufactured in state of the art ISO/TS 16949:2002 certified facilities.

#### **Benefits**

- · AEC-Q200 automotive qualified
- -55°C to +125°C operating temperature range
- · Reliable and robust termination system
- EIA 1210, 1812 and 2220 Case sizes
- DC voltage ratings of 10V, 16V, 25V, 50V, 100V and 250V
- Capacitance offerings ranging from 0.1µF up to 47µF
- Available capacitance tolerances of ±10% & ±20%
- · Higher capacitance in the same footprint
- · Potential board space savings
- · Advanced protection against thermal and mechanical stress
- · Provides up to 10mm of board flex capability
- · Reduces audible, microphonic noise

- Extremely low ESR and ESL
- Pb-Free and RoHS compliant
- Capable of Pb-Free reflow profiles
- Non-polar device, minimizing installation concerns
- · Tantalum and electrolytic alternative





# **Ordering Information**

C	2220	C	106	M	5	R	2	С	AUTO
Ceramic	Case Size (L" x W")	Specification/ Series	Capacitance Code (pF)	Capacitance Tolerance <sup>1</sup>	Voltage	Dielectric	Failure Rate/Design	Leadframe Finish <sup>2</sup>	Packaging/Grade (C-Spec) <sup>3</sup>
	1210 1812 2220	C = Standard	2 Sig. Digits + Number of Zeros	K = ±10% M = ±20%	8 = 10V 4 = 16V 3 = 25V 5 = 50V 1 = 100V A = 250V	R = X7R	1 = KPS Single Chip Stack 2 = KPS Double Chip Stack	C = 100% Matte Sn	AUTO = Automotive Grade 7" Reel Unmarked

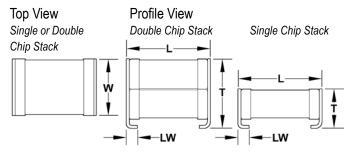
<sup>&</sup>lt;sup>1</sup> Double chip stacks ("2" in the 13th character position of the ordering code) are only available in M ( $\pm$ 20%) capacitance tolerance. Single chip stacks ("1" in the 13th character position of the ordering code) are available in K ( $\pm$ 10%) or M ( $\pm$ 20%) tolerances.

<sup>&</sup>lt;sup>2</sup> Additional leadframe finish options may be available. Contact KEMET for details.

<sup>&</sup>lt;sup>3</sup> Additional reeling or packaging options may be available. Contact KEMET for details.



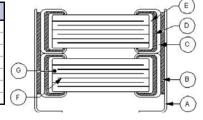
# **Dimensions – Millimeters (Inches)**



Chip Stack	EIA Size Code	Metric Size Code	L Length	W Width	T Thickness	LW Lead Width	Mounting Technique
	1210	3225	3.50 (.138) ± 0.30 (.012)	2.60 (.102) ± 0.30 (.012)	3.35 (.132) ± 0.10 (.004)	0.80 (.032) ± 0.15 (.006)	
Single	1812	4532	5.00 (.197) ± 0.50 (.020)	3.50 (.138) ± 0.50 (.020)	2.65 (.104) ± 0.35 (.014)	1.10 (.043) ± 0.30 (.012)	
	2220	5650	6.00 (.236) ± 0.50 (.020)	5.00 (.197) ± 0.50 (.020)	$3.50 (.138) \pm 0.30 (.012)$	1.60 (.063) ± 0.30 (.012)	Solder Reflow
	1210	3225	3.50 (.138) ± 0.30 (.012)	2.60 (.102) ± 0.30 (.012)	6.15 (.242) ± 0.15 (.006)	0.80 (.031) ± 0.15 (.006)	Only
Double	1812	4532	5.00 (.197) ± 0.50 (.020)	3.50 (.138) ± 0.50 (.020)	5.00 (.197) ± 0.50 (.020)	1.10 (.043) ± 0.30 (.012)	
	2220	5650	6.00 (.236) ± 0.50 (.020)	5.00 (.197) ± 0.50 (.020)	5.00 (.197) ± 0.50 (.020)	1.60 (.063) ± 0.30 (.012)	

# **Outline Drawing**

Ref	Name	Material			
A	Leadframe	Phosphor Bronze - Alloy 510			
В	Leadframe Attach	High Temp Solder			
С		Cu			
D	Termination	Ni			
E		Sn			
F	Electrode	Ni			
G	Dielectric	BaTiO₃			



# **Applications**

Typical applications include smoothing circuits, DC/DC converters, power supplies (input/output filters), noise reduction (piezoelectric/mechanical), circuits with a direct battery or power source connection, critical and safety relevant circuits without (integrated) current limitation and any application that is subject to high levels of board flexure or temperature cycling.

#### **Qualification/Certification**

Automotive grade products meet or exceed the requirements outlined by the Automotive Electronics Council. Details regarding test methods and conditions are referenced in document AEC-Q200, Stress Test Qualification for Passive Components. For additional information regarding the Automotive Electronics Council and AEC-Q200, please visit their website @www.aecouncil.com.

# **Environmental Compliance**

Pb-Free and RoHS compliant



#### **Electrical Parameters/Characteristics**

Item	Parameters/Characteristics
Operating Temperature Range	-55°C to +125°C
Capacitance Change with Reference to +25°C and 0 VDC Applied (TCC)	±15%
Aging Rate (Max % Cap Loss/Decade Hour)	3.0%
Dielectric Withstanding Voltage	250% of rated voltage (5 ± 1 seconds and charge/discharge not exceeding 50mA)
Dissipation Factor (DF) Maximum Limits @ 25°C	5%(10V), 3.5%(16V & 25V) and 2.5%(50V to 250V)
Insulation Resistance (IR) Limit @ 25°C	See Insulation Resistance Limit Table (Rated voltage applied for 120 ± 5 secs @ 25°C)

Regarding Aging Rate: Capacitance measurements (including tolerance) are indexed to a referee time of 1000 hours.

To obtain IR limit, divide  $M\Omega$ - $\mu$ F value by the capacitance and compare to  $G\Omega$  limit. Select the lower of the two limits.

Capacitance and Dissipation Factor (DF) measured under the following conditions:

1kHz ± 50Hz and 1.0 ± 0.2 Vrms if capacitance ≤10µF

120Hz  $\pm$  10Hz and 0.5  $\pm$  0.1 Vrms if capacitance >10 $\mu$ F

Note: When measuring capacitance it is important to ensure the set voltage level is held constant. The HP4284 & Agilent E4980 have a feature known as Automatic Level Control (ALC). The ALC feature should be switched to "ON".

#### **Post Environmental Limits**

High Temperature Life, Biased Humidity, Moisture Resistance										
Dielectric	Rated DC Voltage	Capacitance Value	DF (%)	Cap Shift	IR					
	>25		3.0							
X7R	16 / 25 All		5.0	± 20%	10% of Initial Limit					
	< 16		7.5							

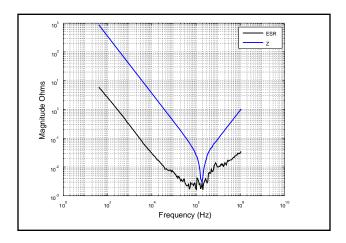
#### **Insulation Resistance Limit Table**

EIA Case Size	1000 megohm microfarads or $100G\Omega$	500 megohm microfarads or 10GΩ
1210	< 0.39µF	≥ 0.39µF
1812	< 2.2µF	≥ 2.2µF
2220	< 10µF	≥ 10µF

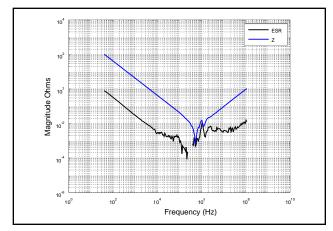


#### **Electrical Characteristics**

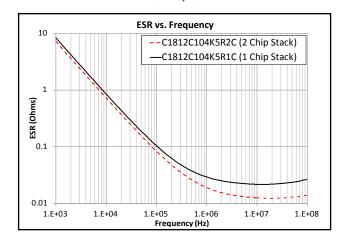
#### Z and ESR C1210C475M5R1C



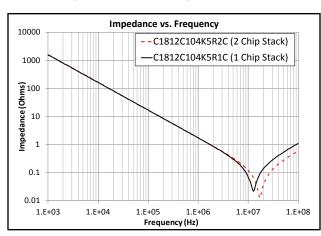
# Z and ESR C2220C476M3R2C



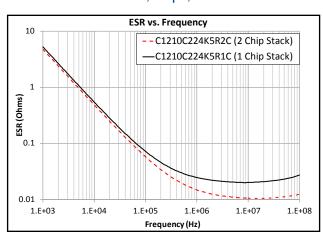
# ESR - 1812, .10µF, 50V X7R



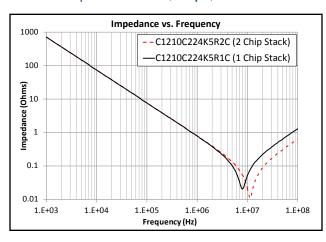
Impedance - 1812, .10µF, 50V X7R



#### ESR - 1210, .22µF, 50V X7R



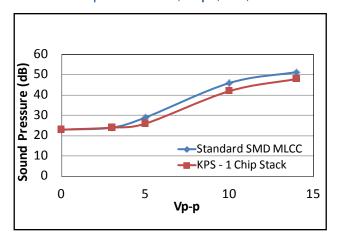
#### Impedance - 1210, .22µF, 50V X7R



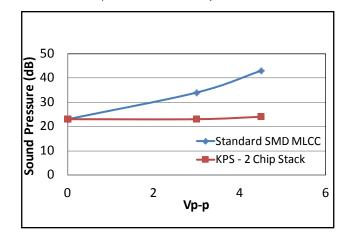


#### **Electrical Characteristics con't**

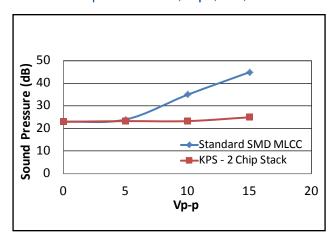
Microphonics - 1210, 4.7µF, 50V, X7R



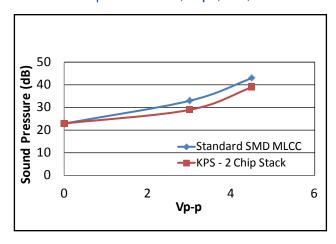
Microphonics - 2220, 22µF, 50V, X7R



Microphonics - 2220, 47µF, 25V, X7R

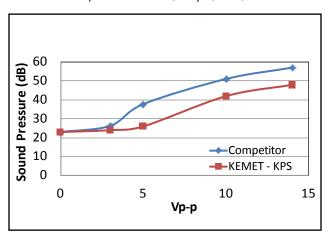


Microphonics - 1210, 22µF, 25V, X7R

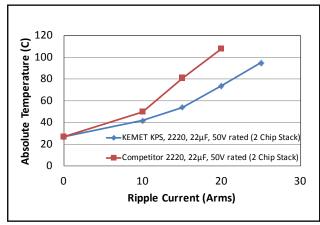


# **Competitive Comparision**

Microphonics - 1210, 4.7µF, 50V, X7R



Ripple Current (Arms) 2220, 22µF, 50V

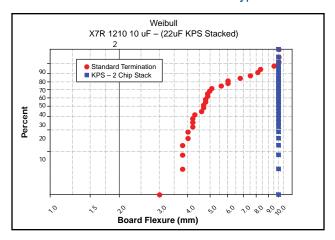


Note: Refer to Table 4 for test method.

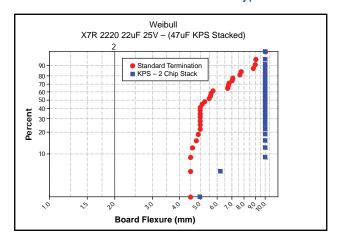


# **Electrical Characteristics**

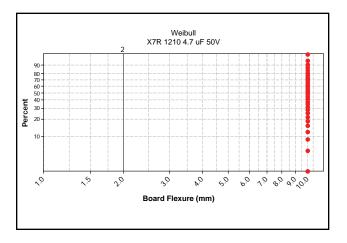
# Board Flex vs. Termination Type



# Board Flex vs. Termination Type



#### Board Flexure to 10mm



#### Board Flexure to 10mm

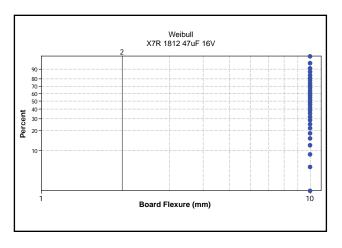




Table 1 – (1210 - 2220 Case Sizes)

		Ser	ies			C,	1210					C181	2			(	2220	)	
Сар	Сар	Voltage	e Code	8	4	3	5	1	Α	4	3	5	1	Α	4	3	5	1	Α
Cap	Code	Volta	ge DC	9	16	25	50	100	250	16	25	20	100	250	16	25	50	100	250
		Cap Tolerance P		Prod	uct A	vailab	ility a	nd Chi	p Thick	ness	Code	s - Se	e Tab	le 2 for	Chip T	hickr	ess [	Dimen	sions
				•		Si	nale	Chip S	Stack										
0.10 µF	104	K	М	FV	FV	FV	FV	FV	FV	GP	GP	GP	UD	UD	JP	JP	JP	UD	UD
0.22 µF	224	K	M	FV	FV	FV	FV	FV		GP	GP	GP	UD	UD	JP	JP	JP	UD	UD
0.47 µF	474	K	M	FV	FV	FV	FV	FV		GP	GP	GP	UD	UD	JP	JP	JP	UD	UD
1.0 µF	105	K	M	FV	FV	FV	FV	FV		GP	GP	GP	UD		JP	JP	JP	UD	UD
2.2 µF	225	K	M	FV	FV	FV	FV			GP	GP	GP			JP	JP	JP	UD	
3.3 µF	335	K	M	F۷	FV	FV	FV			GP	GP	GP			JP	JP	JP	UD	
4.7 µF	475	K	M	FV	FV	FV	FV			GP	GP	GP			JP	JP	JP		
10 µF	106	K	M	FV	FV	FV				GP	GP				JP	JP	JP		
15 µF	156	K	M												JP	JP			
22 µF	226	K	M												JP	JP			
33 µF	336	K	M																
47 μF	476	K	M																
100 μF	107	K	M																
						Do	uble	Chip S	Stack										
0.10 µF	104		M	FW	FW	FW	FW	FW	FW	GR	GR	GR	UD	UD	JR	JR	JR	UD	UD
0.22 µF	224		M	FW	FW	FW	FW	FW	FW	GR	GR	GR	UD	UD	JR	JR	JR	UD	UD
0.47 μF	474		M	FW	FW	FW	FW	FW		GR	GR	GR	UD	UD	JR	JR	JR	UD	UD
1.0 µF	105		M	FW	FW	FW	FW	FW		GR	GR	GR	UD	UD	JR	JR	JR		
2.2 µF	225		M	FW	FW	FW	FW	FW		GR	GR	GR	UD		JR	JR	JR		
3.3 µF	335		M	FW	FW	FW	FW			GR	GR	GR	UD		JR	JR	JR	UD	
4.7 µF	475		М	FW	FW	FW	FW			GR	GR	GR			JR	JR	JR	UD	
10 µF	106		М	FW	FW	FW	FW			GR	GR	GR			JR	JR	JR		
22 µF	226		M	FW	FW	FW				GR	GR				JR	JR	JR		
33 µF	336		М												JR	JR			
47 μF	476		М												JR	JR			
100 µF	107		M																
220 μF	227		M	<del>  _</del>			_	0	0			_	0	0	-	ļ	_	-	0
	Сар	Volta		9	16	25	20	100	250	16	25	20	5	250	16	25	20	100	250
Cap		Voltag	e Code	8	4	3	5	1	Α	4	3	5	1	Α	4	3	5	1	Α
	Code	Ser	ries			C,	1210					C181	2			(	2220	)	

UD = Under Development

**Table 2 – Chip Thickness / Packaging Quantities** 

Thickness Code	Chip Size	Thickness ± Range (mm)	Qty per Reel 7" Plastic	Qty per Reel 13" Plastic
FV	1210	3.35 ± 0.10	600	2000
FW	1210	6.15 ± 0.15	300	1000
GP	1812	2.65 ± 0.35	500	2000
GR	1812	5.00 ± 0.50	400	1700
JP	2220	$3.50 \pm 0.30$	300	1300
JR	2220	5.00 ± 0.50	200	800

Package Quantity Based on Finished Chip Thickness Specifications



# **Soldering Process**

Recommended Soldering Technique:

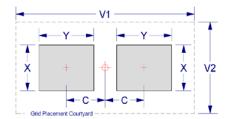
Solder reflow only

Recommended Soldering Profile:

• KEMET recommends following the guidelines outlined in IPC/JEDEC J-STD-020

# **Table 3 – KPS Land Pattern Design Recommendations**

EIA Size Code	Metric Size Code	Median (Nominal) Land Protrusion (mm)					
		Х	Υ	2xC			
1210	3225	1.75	1.14	3.00			
1812	4532	2.87	1.35	4.39			
2220	5650	4.78	2.08	5.38			



# Table 4 – Performance & Reliability: Test Methods and Conditions

Stress	Reference	Test or Inspection Method
Terminal Strength	JIS-C-6429	Appendix 1, Note: Force of 1.8kg for 60 seconds.
Board Flex	JIS-C-6429	Appendix 2, Note: 2mm (min) for all except 3mm for C0G.
		Magnification 50X. Conditions:
Caldarahilitu	J-STD-002	a) Method B, 4 hrs @ 155°C, dry heat @ 235°C
Solderability	J-51D-002	b) Method B @ 215°C category 3
		c) Method D, category 3 @ 260°C
Temperature Cycling	JESD22 Method JA-104	1000 cycles (-55°C to +125°C), Measurement at 24 hrs. +/- 2 hrs after test conclusion.
Biased Humidity	MIL-STD-202 Method 103	Load Humidity: 1000 hours 85°C/85%RH and Rated Voltage. Add 100K ohm resistor. Measurement at 24 hrs. +/- 2 hrs after test conclusion.  Low Volt Humidity: 1000 hours 85°CO/85%RH and 1.5V. Add 100K ohm resistor.  Measurement at 24 hrs. +/- 2 hrs after test conclusion.
Moisture Resistance	MIL-STD-202 Method 106	t = 24 hours/cycle. Steps 7a & 7b not required. Unpowered.  Measurement at 24 hrs. +/- 2 hrs after test conclusion.
Thermal Shock	MIL-STD-202 Method 107	-55°C/+125°C. Note: Number of cycles required-300, maximum transfer time-20 seconds, dwell time-15 minutes. Air-Air.
High Temperature Life	MIL-STD-202 Method 108/ EIA-198	1000 hours at 125°C (85°C for X5R, Z5U and Y5V) with 2X rated voltage applied.
Storage Life	MIL-STD-202 Method 108	150°C, 0VDC, for 1000 hours.
Mechanical Shock	MIL-STD-202 Method 213	Figure 1 of Method 213, Condition F.
Resistance to Solvents	MIL-STD-202 Method 215	Add aqueous wash chemical - OKEM Clean or equivalent.



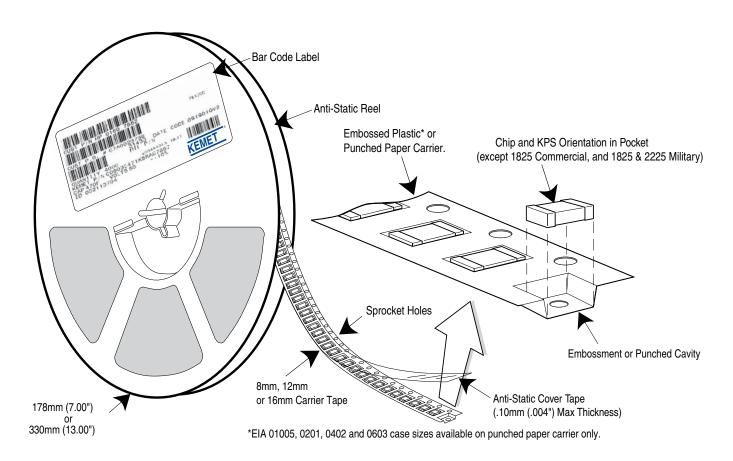
### **Storage and Handling**

Ceramic chip capacitors should be stored in normal working environments. While the chips themselves are quite robust in other environments, solderability will be degraded by exposure to high temperatures, high humidity, corrosive atmospheres, and long term storage. In addition, packaging materials will be degraded by high temperature – reels may soften or warp, and tape peel force may increase. KEMET recommends that maximum storage temperature not exceed 40°C, and maximum storage humidity not exceed 70% relative humidity. In addition, temperature fluctuations should be minimized to avoid condensation on the parts, and atmospheres should be free of chlorine and sulfur bearing compounds. For optimized solderability, chip stock should be used promptly, preferably within 1.5 years of receipt.



# **Tape & Reel Packaging Information**

KEMET offers Multilayer Ceramic Chip Capacitors packaged in 8mm, 12mm and 16mm tape on 7" and 13" reels in accordance with EIA standard 481. This packaging system is compatible with all tape fed automatic pick and place systems. See Table 2 for details on reeling quantities for commercial chips.



**Table 5 – Carrier Tape Configuration (mm)** 

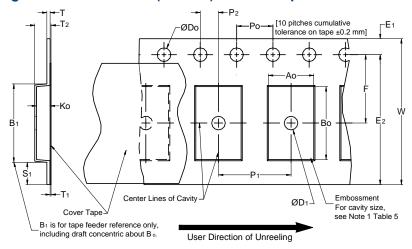
EIA Case Size	Tape Size (W)*	Lead Space (P <sub>1</sub> )*
01005 - 0402	8	2
0603 - 1210	8	4
1805 - 1808	12	4
≥ 1812	12	8
KPS 1210	12	8
KPS 1812 & 2220	16	12
Array 0508 & 0612	8	4

<sup>\*</sup>Refer to Figure 1 for W and P, carrier tape reference locations.

<sup>\*</sup>Refer to Table 6 for tolerance specifications.



# Figure 1 – Embossed (Plastic) Carrier Tape Dimensions



# Table 6 - Embossed (Plastic) Carrier Tape Dimensions

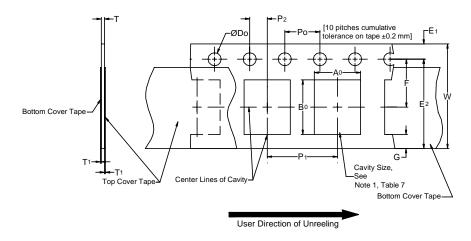
Metric will govern

	Constant Dimensions — Millimeters (Inches)											
Tape Size	D <sub>0</sub>	D₁ Min. Note 1	E <sub>1</sub>	P <sub>0</sub>	P <sub>2</sub>	R Ref. Note 2	S₁ Min. Note 3	T Max.	T <sub>1</sub> Max.			
8mm		1.0 (0.039)				25.0 (0.984)						
12mm	1.5 +0.10/-0.0 (0.059 +0.004/-0.0)	1.5	$1.75 \pm 0.10$ (0.069 ± 0.004)	4.0 ± 0.10 (0.157 ± 0.004)	2.0 ± 0.05 (0.079 ± 0.002)	2) 30 (1.181)	0.600 (0.024)	0.600 (0.024)	0.100 (0.004)			
16mm		(0.059)										
			Variable Dime	ensions — Milli	meters (Inche	s)						
Tape Size	Pitch	B₁ Max. Note 4	E <sub>2</sub> Min.	F	P <sub>1</sub>	T <sub>2</sub> Max	W Max	A <sub>0</sub> ,B	<sub>0</sub> & K <sub>0</sub>			
8mm	Single (4mm)	4.35 (0.171)	6.25 (0.246)	$3.5 \pm 0.05$ (0.138 $\pm$ 0.002)	4.0 ± 0.10 (0.157 ± 0.004)	2.5 (0.098)	8.3 (0.327)					
12mm	Single (4mm) & Double (8mm)	8.2 (0.323)	10.25 (0.404)	5.5 ± 0.05 (0.217 ± 0.002)	$8.0 \pm 0.10$ (0.315 ± 0.004)	4.6 (0.181)	12.3 (0.484)	No	te 5			
16mm	Triple (12mm)	12.1 (0.476)	14.25 (0.561)	5.5 ± 0.05 (0.217 ± 0.002)	8.0 ± 0.10 (0.315 ± 0.004)	4.6 (0.181)	16.3 (0.642)					

- 1. The embossment hole location shall be measured from the sprocket hole controlling the location of the embossment. Dimensions of embossment location and hole location shall be applied independent of each other.
- 2. The tape with or without components shall pass around R without damage (see Figure 5).
- 3. If S,<1.0 mm, there may not be enough area for cover tape to be properly applied (see EIA Document 481 paragraph 4.3 (b)).
- 4. B1 dimension is a reference dimension for tape feeder clearance only.
- 5. The cavity defined by  $A_{\alpha}$ ,  $B_{\alpha}$  and  $K_{\alpha}$  shall surround the component with sufficient clearance that:
  - (a) the component does not protrude above the top surface of the carrier tape.
  - (b) the component can be removed from the cavity in a vertical direction without mechanical restriction, after the top cover tape has been removed.
  - (c) rotation of the component is limited to 20° maximum for 8 and 12mm tapes and 10° maximum for 16mm tapes (see Figure 3).
  - (d) lateral movement of the component is restricted to 0.5 mm maximum for 8mm and 12mm wide tape and to 1.0mm maximum for 16mm tape (see Figure 4).
  - (e) for KPS Series product  $A_0$  and  $B_0$  are measured on a plane 0.3mm above the bottom of the pocket.
  - (f) see Addendum in EIA Document 481 for standards relating to more precise taping requirements.



# Figure 2 – Punched (Paper) Carrier Tape Dimensions



# **Table 7 – Punched (Paper) Carrier Tape Dimensions**

Metric will govern

	Constant Dimensions — Millimeters (Inches)						
Tape Size	D <sub>0</sub>	E <sub>1</sub>	P <sub>0</sub>	P <sub>2</sub>	T₁Max	G Min	R Ref. Note 2
8mm	1.5 +0.10-0.0 (0.059 +0.004, -0.0)	1.75 ±0.10 (0.069 ±0.004)	4.0 ±0.10 (0.157 ±0.004)	2.0 ±0.05 (0.079 ±0.002)	0.10 (.004) Max.	0.75 (.030)	25 (.984)
	Variable Dimensions — Millimeters (Inches)						
Tape Size	Pitch	E2 Min	F	P <sub>1</sub>	T Max	W Max	$A_0B_0$
8mm	Half (2mm)	6.25	3.5 ± 0.05	$2.0 \pm 0.05$ (0.079 ± 0.002)	1.1	8.3 (0.327)	Note 5
8mm	Single (4mm)	(0.246)	$(0.138 \pm 0.002)$	$4.0 \pm 0.10$ (0.157 ± 0.004)	(0.098)	8.3 (0.327)	NOTE 5

<sup>1.</sup> The cavity defined by  $A_{o}$ ,  $B_{o}$  and T shall surround the component with sufficient clearance that:

a) the component does not protrude beyond either surface of the carrier tape.

b) the component can be removed from the cavity in a vertical direction without mechanical restriction, after the top cover tape has been removed.

d) lateral movement of the component is restricted to 0.5 mm maximum (see Figure 4).

e) see Addendum in EIA Document 481 for standards relating to more precise taping requirements.

<sup>2.</sup> The tape with or without components shall pass around R without damage (see Figure 5).



### **Packaging Information Performance Notes**

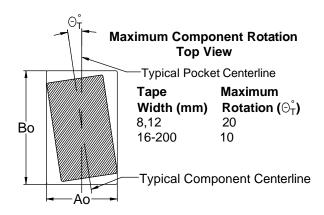
- 1. Cover Tape Break Force: 1.0 Kg Minimum.
- 2. Cover Tape Peel Strength: The total peel strength of the cover tape from the carrier tape shall be:

Tape Width	Peel Strength	
8mm	0.1 Newton to 1.0 Newton (10gf to 100gf)	
12mm & 16mm	0.1 Newton to 1.3 Newton (10gf to 130gf)	

The direction of the pull shall be opposite the direction of the carrier tape travel. The pull angle of the carrier tape shall be 165° to 180° from the plane of the carrier tape. During peeling, the carrier and/or cover tape shall be pulled at a velocity of 300±10 mm/minute.

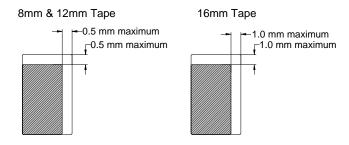
3. Labeling: Bar code labeling (standard or custom) shall be on the side of the reel opposite the sprocket holes. Refer to EIA-556 and EIA-624.

# Figure 3 – Maximum Component Rotation



# Maximum Component Rotation Side View Tape Maximum Width (mm) Rotation (⊖s) 8,12 20 16-56 10 72-200 5

# Figure 4 – Maximum Lateral Movement



# Figure 5 – Bending Radius

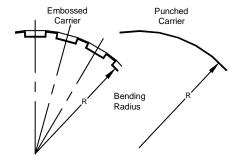
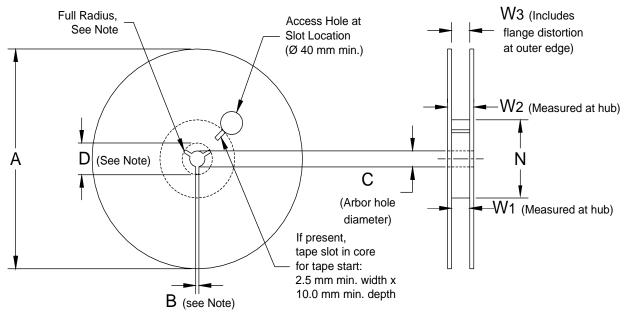




Figure 6 - Reel Dimensions



Note: Drive spokes optional; if used, dimensions B and D shall apply.

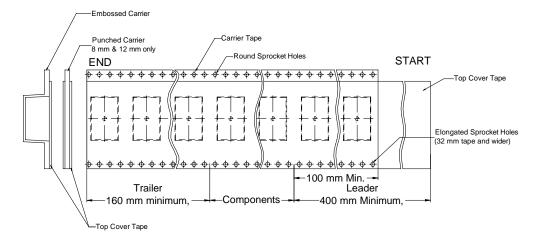
# Table 8 - Reel Dimensions

Metric will govern

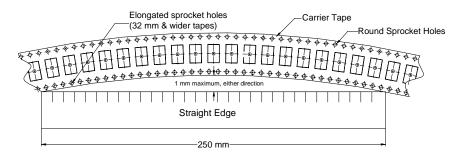
Constant Dimensions — Millimeters (Inches)					
Tape Size	A	B Min	С	D Min	
8mm	178 ± 0.20				
12mm	(7.008 ± 0.008) or	1.5 (0.059)	13.0 +0.5/-0.2 (0.521 +0.02/-0.008)	20.2 (0.795)	
16mm	$330 \pm 0.20$ $(13.000 \pm 0.008)$	(****)	(,	(,	
Variable Dimensions — Millimeters (Inches)					
Tape Size	N Min	W <sub>1</sub>	W <sub>2</sub> Max	$W_3$	
8mm		8.4 +1.5/-0.0 (0.331 +0.059/-0.0)	14.4 (0.567)		
12mm	50 (1.969)	12.4 +2.0/-0.0 (0.488 +0.078/-0.0)	18.4 (0.724)	Shall accommodate tape width without interference	
16mm		16.4 +2.0/-0.0 (0.646 +0.078/-0.0)	22.4 (0.882)		



# Figure 7 – Tape Leader & Trailer Dimensions



# Figure 8 - Maximum Camber





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