November 8, 2010

National Semiconductor

LMC555

CMOS Timer

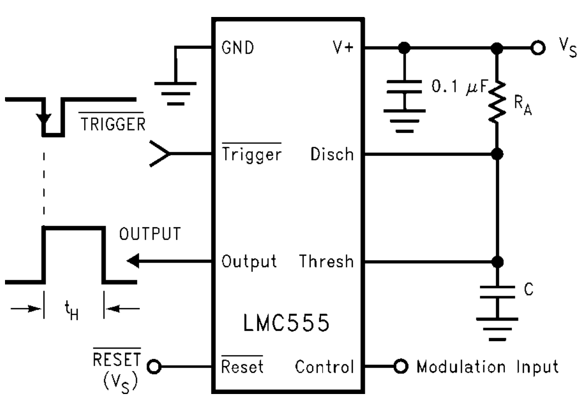
General Description

The LMC555 is a CMOS version of the industry standard 555 series general purpose timers. In addition to the standard package (SOIC, MSOP, and MDIP) the LMC555 is also available in a chip sized package (8 Bump micro SMD) using National's micro SMD package technology. The LMC555 offers the same capability of generating accurate time delays and frequencies as the LM555 but with much lower power dissipation and supply current spikes. When operated as a one-shot, the time delay is precisely controlled by a single external resistor and capacitor. In the stable mode the oscillation frequency and duty cycle are accurately set by two external resistors and one capacitor. The use of National Semiconductor's LMCMOS™ process extends both the frequency range and low supply capability.

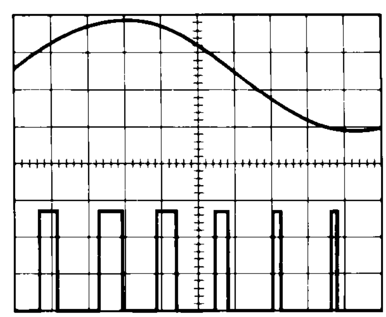
Features

- Less than 1 mW typical power dissipation at 5V supply
- 3 MHz astable frequency capability
- 1.5V supply operating voltage guaranteed
- Output fully compatible with TTL and CMOS logic at 5V supply
- Tested to −10 mA, +50 mA output current levels
- Reduced supply current spikes during output transitions
- Extremely low reset, trigger, and threshold currents
- Excellent temperature stability
- Pin-for-pin compatible with 555 series of timers
- Available in 8-pin MSOP Package and 8-Bump micro SMD package

Pulse Width Modulator



866920



866915

Ordering Information

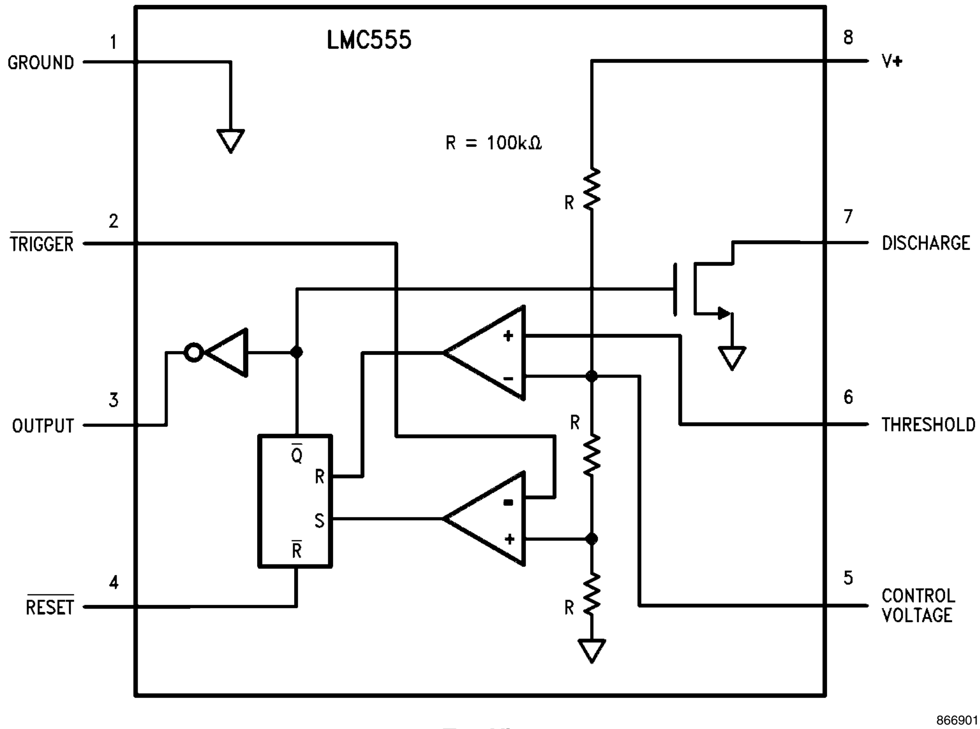
Package	Temperature Range	Package Marking	Transport Media	NSC Drawing
	Industrial −40°C to +85°C			
8-Pin Small Outline (SO)	LMC555CM	LMC555CM	Rails	M08A
	LMC555CMX		2.5k Units Tape and Reel	
8-Pin Mini Small Outline (MSOP)	LMC555CMM	ZC5	1k Units Tape and Reel	MUA08A
	LMC555CMMX		3.5k Units Tape and Reel	
8-Pin Molded Dip (MDIP)	LMC555CN	LMC555CN	Rails	N08E
8-Bump micro SMD NOPB	LMC555CTP	F02	250 Units Tape and Reel	TPA08FGA
	LMC555CTPX		3k Units Tape and Reel	

Note: See Mil-datasheet MNLMC555-X for specifications on the military device LMC555J/883.

LMCMOS™ is a trademark of National Semiconductor Corp.

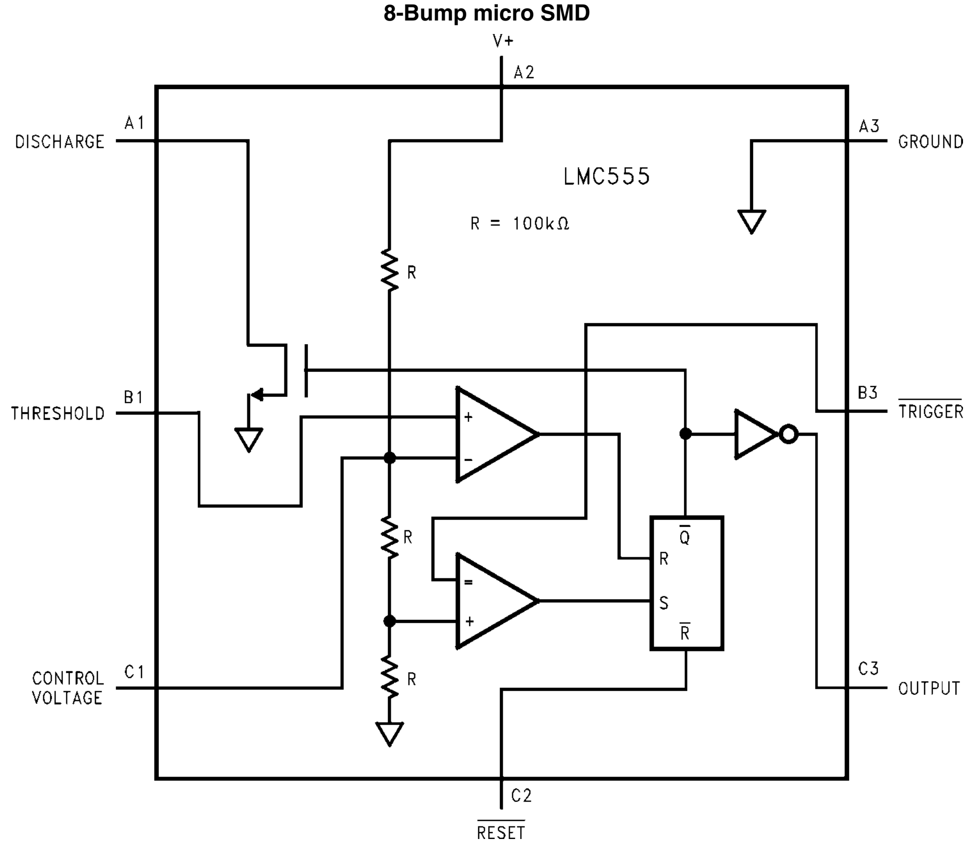
Connection Diagrams

8-Pin SOIC, MSOP, MDIP



Top View

8-Bump micro SMD



Top View
(Bump Side Down)

Absolute Maximum Ratings (Note 2, Note 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, V^+	15V
Input Voltages, V_{TRIG}, V_{RES}, V_{CTRL}, V_{THRESH}	−0.3V to V_S + 0.3V
Output Voltages, V_O, V_{DIS}	15V
Output Current I_O, I_{DIS}	100 mA
Storage Temperature Range	−65°C to +150°C
Soldering specification for MDIP package:	
Soldering (10 seconds)	260°C
Soldering specification for all other packages: see product folder at www.national.com and www.national.com/ms/MS/MS-SOLDERING.pdf	

Operating Ratings (Note 2, Note 3)

Termperature Range	−40°C to +85°C
Thermal Resistance (θ_{JA}) (Note 2)	
SO, 8-Pin Small Outline	169°C/W
MSOP, 8-Pin Mini Small Outline	225°C/W
MDIP, 8-Pin Molded Dip	111°C/W
8-Bump micro SMD	220°C/W
Maximum Allowable Power Dissipation @25°C	
MDIP-8	1126 mW
SO-8	740 mW
MSOP-8	555 mW
8 Bump micro SMD	568 mW

Electrical Characteristics (Note 1, Note 2)

Test Circuit, T = 25°C, all switches open, $\overline{RESET}$ to V_S unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units (Limits)
I_S	Supply Current	V_S = 1.5V V_S = 5V V_S = 12V		50 100 150	150 250 400	μA
V_{CTRL}	Control Voltage	V_S = 1.5V V_S = 5V V_S = 12V	0.8 2.9 7.4	1.0 3.3 8.0	1.2 3.8 8.6	V
V_{DIS}	Discharge Saturation Voltage	V_S = 1.5V, I_{DIS} = 1 mA V_S = 5V, I_{DIS} = 10 mA		75 150	150 300	mV
V_{OL}	Output Voltage (Low)	V_S = 1.5V, I_O = 1 mA V_S = 5V, I_O = 8 mA V_S = 12V, I_O = 50 mA		0.2 0.3 1.0	0.4 0.6 2.0	V
V_{OH}	Output Voltage (High)	V_S = 1.5V, I_O = −0.25 mA V_S = 5V, I_O = −2 mA V_S = 12V, I_O = −10 mA	1.0 4.4 10.5	1.25 4.7 11.3		V
V_{TRIG}	Trigger Voltage	V_S = 1.5V V_S = 12V	0.4 3.7	0.5 4.0	0.6 4.3	V
I_{TRIG}	Trigger Current	V_S = 5V		10		pA
V_{RES}	Reset Voltage	V_S = 1.5V (Note 4) V_S = 12V	0.4 0.4	0.7 0.75	1.0 1.1	V
I_{RES}	Reset Current	V_S = 5V		10		pA
I_{THRESH}	Threshold Current	V_S = 5V		10		pA
I_{DIS}	Discharge Leakage	V_S = 12V		1.0	100	nA
t	Timing Accuracy	SW 2, 4 Closed V_S = 1.5V V_S = 5V V_S = 12V	 0.9 1.0 1.0	 1.1 1.1 1.1	 1.25 1.20 1.25	ms
$\Delta t/\Delta V_S$	Timing Shift with Supply	V_S = 5V ± 1V		0.3		%/V
$\Delta t/\Delta T$	Timing Shift with Temperature	V_S = 5V −40°C ≤ T ≤ +85°C		75		ppm/°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units (Limits)
f_A	Astable Frequency	SW 1, 3 Closed, V_S = 12V	4.0	4.8	5.6	kHz
f_{MAX}	Maximum Frequency	Max. Freq. Test Circuit, V_S = 5V		3.0		MHz
t_R, t_F	Output Rise and Fall Times	Max. Freq. Test Circuit V_S = 5V, C_L = 10 pF		15		ns
t_{PD}	Trigger Propagation Delay	V_S = 5V, Measure Delay from Trigger to Output		100		ns

Note 1: All voltages are measured with respect to the ground pin, unless otherwise specified.

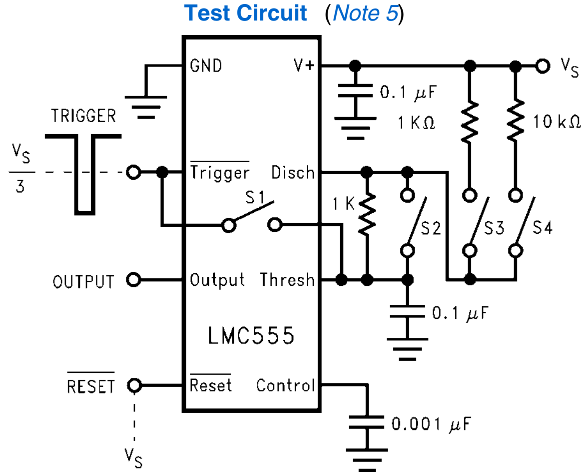
Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: See AN-1112 for micro SMD considerations.

Note 4: If the $\overline{\text{RESET}}$ pin is to be used at temperatures of −20°C and below V_S is required to be 2.0V or greater.

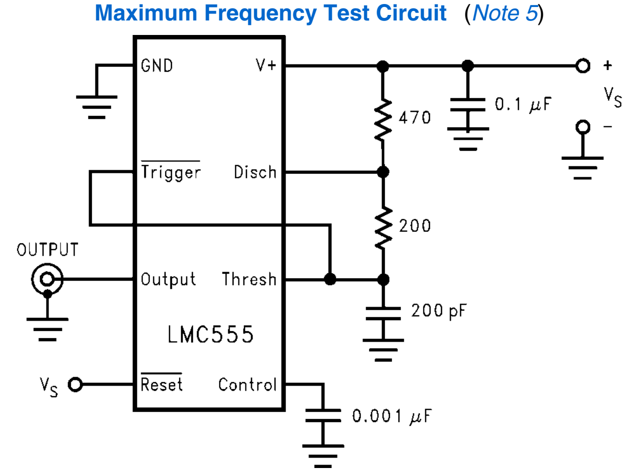
Note 5: For device pinout please refer to table 1

Test Circuit (*Note 5*)



866902

Maximum Frequency Test Circuit (*Note 5*)



866903

TABLE 1. Package Pinout Names vs. Pin Function

Pin Function	Package Pin numbers	
8-Pin SO, MSOP, and MDIP	8-Bump micro SMD	
GND	1	A3
$\overline{\text{Trigger}}$	2	B3
Output	3	C3
$\overline{\text{Reset}}$	4	C2
Control Voltage	5	C1
Threshold	6	B1
Discharge	7	A1
V+	8	A2

Application Information

MONOSTABLE OPERATION

In this mode of operation, the timer functions as a one-shot (*Figure 1*). The external capacitor is initially held discharged by internal circuitry. Upon application of a negative trigger pulse of less than 1/3 V_S to the $\overline{\text{Trigger}}$ terminal, the flip-flop is set which both releases the short circuit across the capacitor and drives the output high.

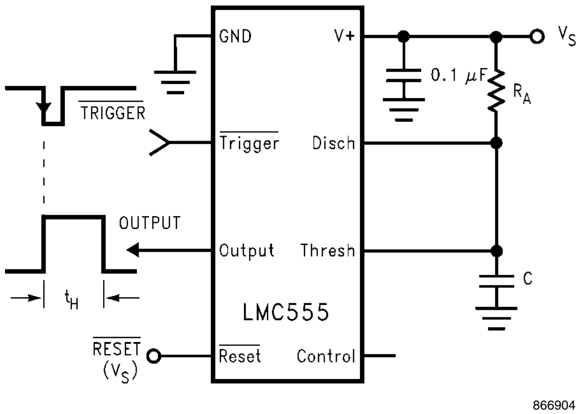
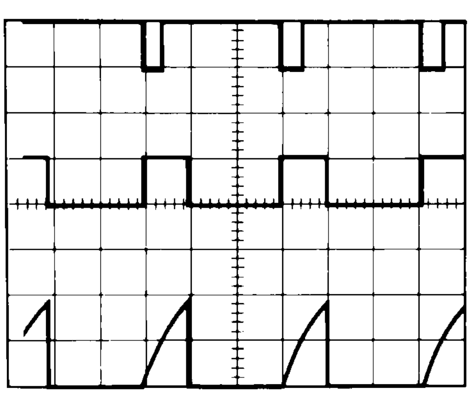


FIGURE 1. Monostable (One-Shot)

The voltage across the capacitor then increases exponentially for a period of $t_H = 1.1\ R_AC$, which is also the time that the output stays high, at the end of which time the voltage equals 2/3 V_S. The comparator then resets the flip-flop which in turn discharges the capacitor and drives the output to its low state. *Figure 2* shows the waveforms generated in this mode of operation. Since the charge and the threshold level of the comparator are both directly proportional to supply voltage, the timing internal is independent of supply.



V_{CC} = 5V — Top Trace: Input 5 V/Div.
TIME = 0.1 ms/Div. — Middle Trace: Output 5 V/Div.
R_A = 9.1 kΩ — Bottom Trace: Capacitor Voltage 2 V/Div.
C = 0.01 µF

FIGURE 2. Monostable Waveforms

Reset overrides Trigger, which can override threshold. Therefore the trigger pulse must be shorter than the desired t_H. The minimum pulse width for the Trigger is 20ns, and it is 400ns for the Reset. During the timing cycle when the output is high, the further application of a trigger pulse will not effect the circuit so long as the trigger input is returned high at least 10µs before the end of the timing interval. However the circuit can be reset during this time by the application of a negative pulse to the reset terminal. The output will then remain in the low state until a trigger pulse is again applied.

When the reset function is not use, it is recommended that it be connected to V_+ to avoid any possibility of false triggering. *Figure 3* is a nomograph for easy determination of RC values for various time delays.

Note: In monstable operation, the trigger should be driven high before the end of timing cycle.

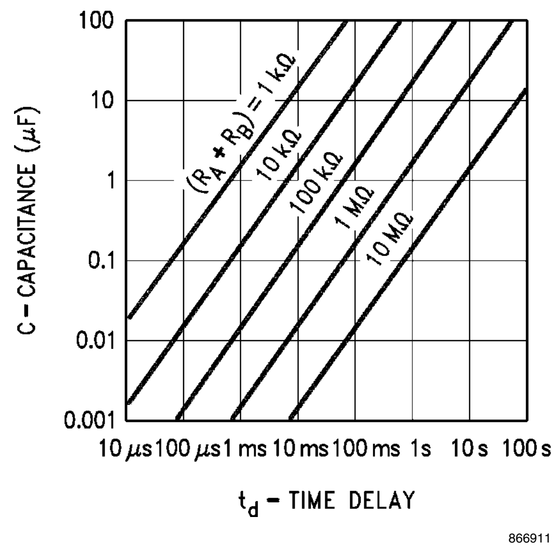


FIGURE 3. Time Delay

ASTABLE OPERATION

If the circuit is connected as shown in *Figure 4* ($\overline{\text{Trigger}}$ and Threshold terminals connected together) it will trigger itself and free run as a multivibrator. The external capacitor charges through $R_A + R_B$ and discharges through R_B. Thus the duty cycle may be precisely set by the ratio of these two resistors.

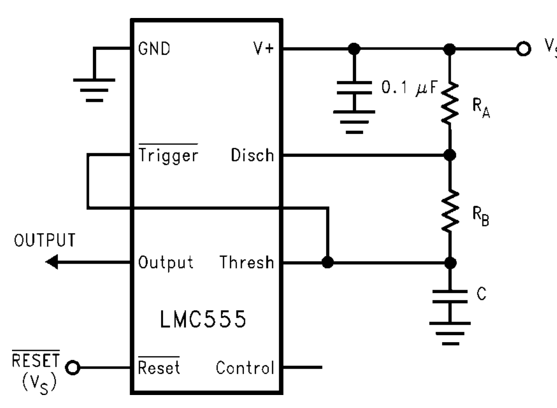
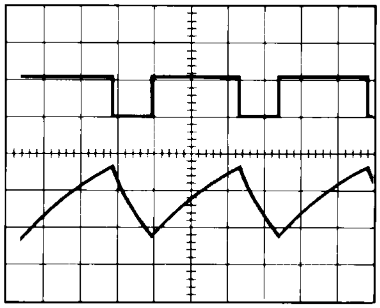


FIGURE 4. Astable (Variable Duty Cycle Oscillator)

In this mode of operation, the capacitor charges and discharges between 1/3 V_S and 2/3 V_S. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

Figure 5 shows the waveform generated in this mode of operation.



866912

V_{CC} = 5V
TIME = 20 µs/Div.
R_A = 3.9 kΩ
R_B = 9 kΩ
C = 0.01 µF

Top Trace: Output 5 V/Div.
Bottom Trace: Capacitor Voltage 1 V/Div.

FIGURE 5. Astable Waveforms

The charge time (output high) is given by

$$t_1 = 0.693\ (R_A + R_B)C$$

And the discharge time (output low) by:

$$t_2 = 0.693\ (R_B)C$$

Thus the total period is:

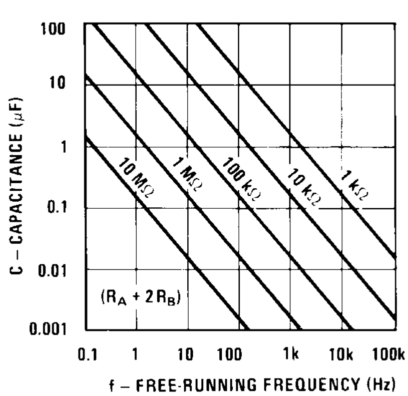
$$T = t_1 + t_2 = 0.693\ (R_A + 2R_B)C$$

The frequency of oscillation is:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2\,R_B)\,C}$$

Figure 6 may be used for quick determination of these RC Values. The duty cycle, as a fraction of total period that the output is low, is:

$$D = \frac{R_B}{R_A + 2R_B}$$

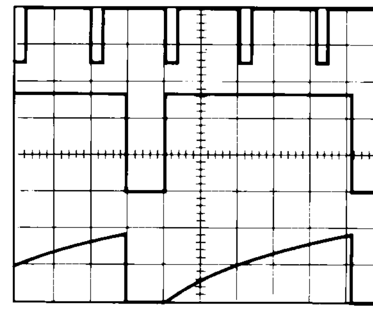


866913

FIGURE 6. Free Running Frequency

FREQUENCY DIVIDER

The monostable circuit of *Figure 1* can be used as a frequency divider by adjusting the length of the timing cycle. *Figure 7* shows the waveforms generated in a divide by three circuit.



866914

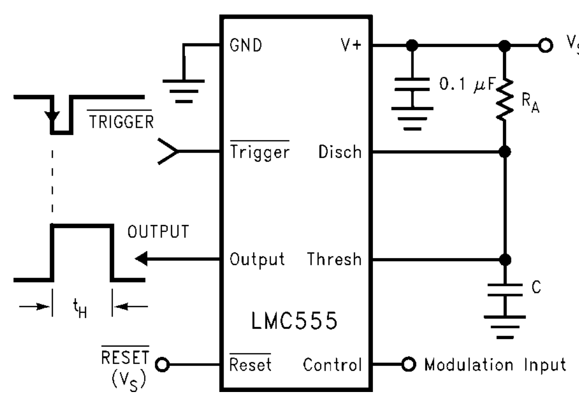
V_{CC} = 5V
TIME = 20 µs/Div.
R_A = 9.1 kΩ
C = 0.01 µF

Top Trace: Input 4 V/Div.
Middle Trace: Output 2 V/Div.
Bottom Trace: Capacitor 2 V/Div.

FIGURE 7. Frequency Divider Waveforms

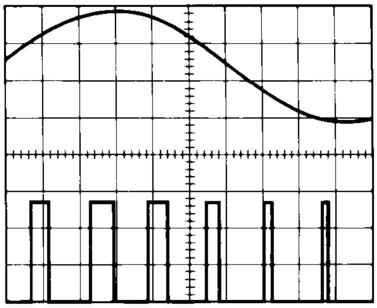
PULSE WIDTH MODULATOR

When the timer is connected in the monostable mode and triggered with a continuous pulse train, the output pulse width can be modulated by a signal applied to the Control Voltage Terminal. *Figure 8* shows the circuit, and in *Figure 9* are some waveform examples.



866920

FIGURE 8. Pulse Width Modulator



866915

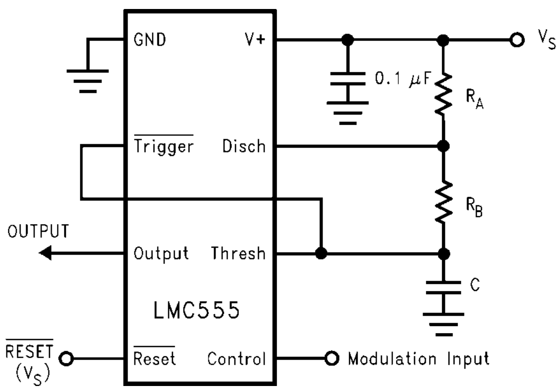
V_{CC} = 5V
TIME = 0.2 ms/Div.
R_A = 9.1 kΩ
C = 0.01 µF

Top Trace: Modulation 1 V/Div.
Bottom Trace: Output Voltage 2 V/Div.

FIGURE 9. Pulse Width Modulator Waveforms

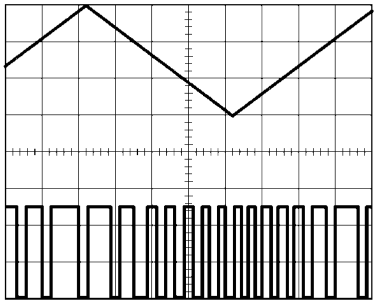
PULSE POSITION MODULATOR

This application uses the timer connected for astable operation, as in *Figure 10*, with a modulating signal again applied to the control voltage terminal. The pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied. *Figure 11* shows the waveforms generated for a triangle wave modulation signal.



866921

FIGURE 10. Pulse Position Modulator



866916

V_{CC} = 5V
TIME = 0.1 ms/Div.
R_A = 3.9 kΩ
R_B = 3 kΩ
C = 0.01 µF

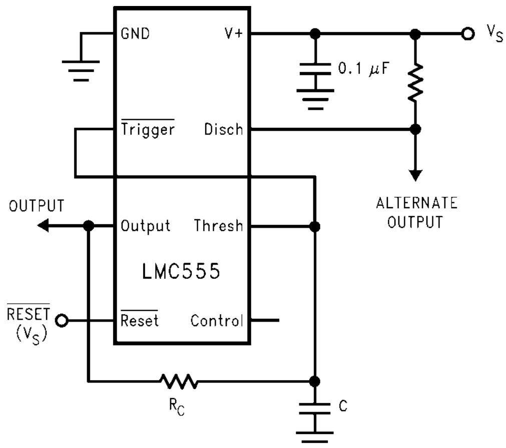
Top Trace: Modulation Input 1 V/Div.
Bottom Trace: Output Voltage 2 V/Div.

FIGURE 11. Pulse Position Modulator Waveforms

50% DUTY CYCLE OSCILLATOR

The frequency of oscillation is

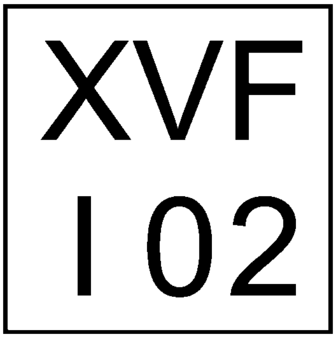
$$f = 1/(1.4\, R_C C)$$



866906

FIGURE 12. 50% Duty Cycle Oscillator

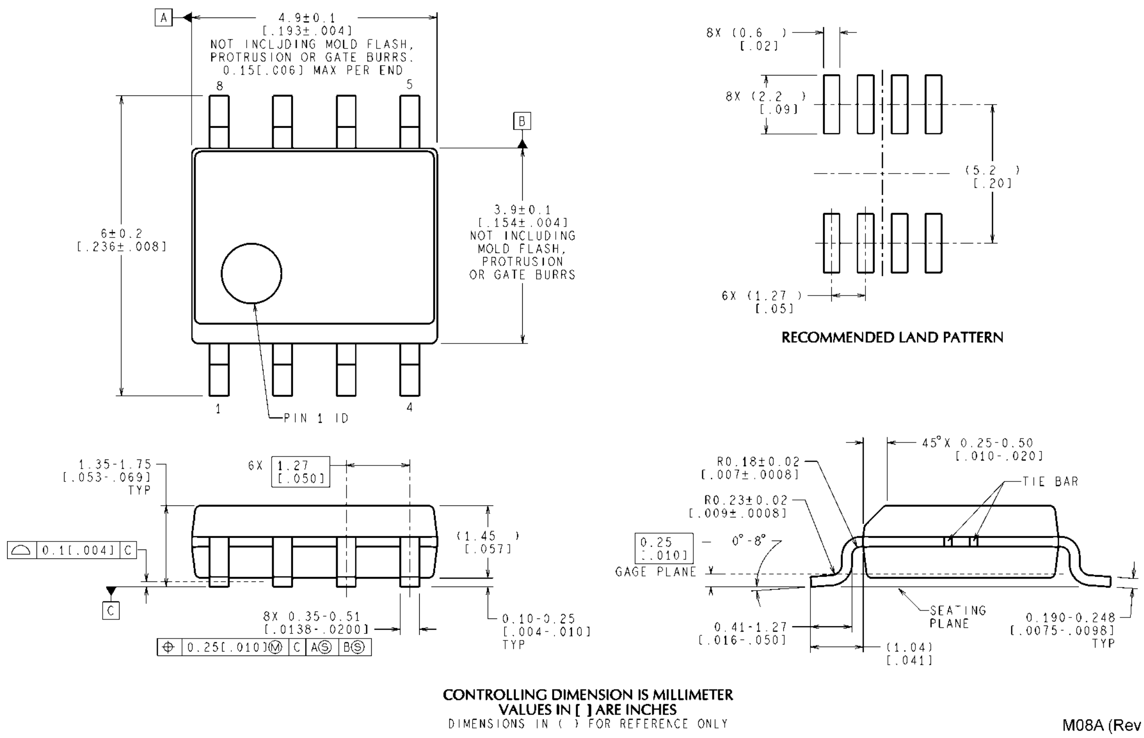
micro SMD Marking Orientation
Top View



X = 1 Digit Date Code
V = 1 Digit Die Run
I = Pin 1 Designator

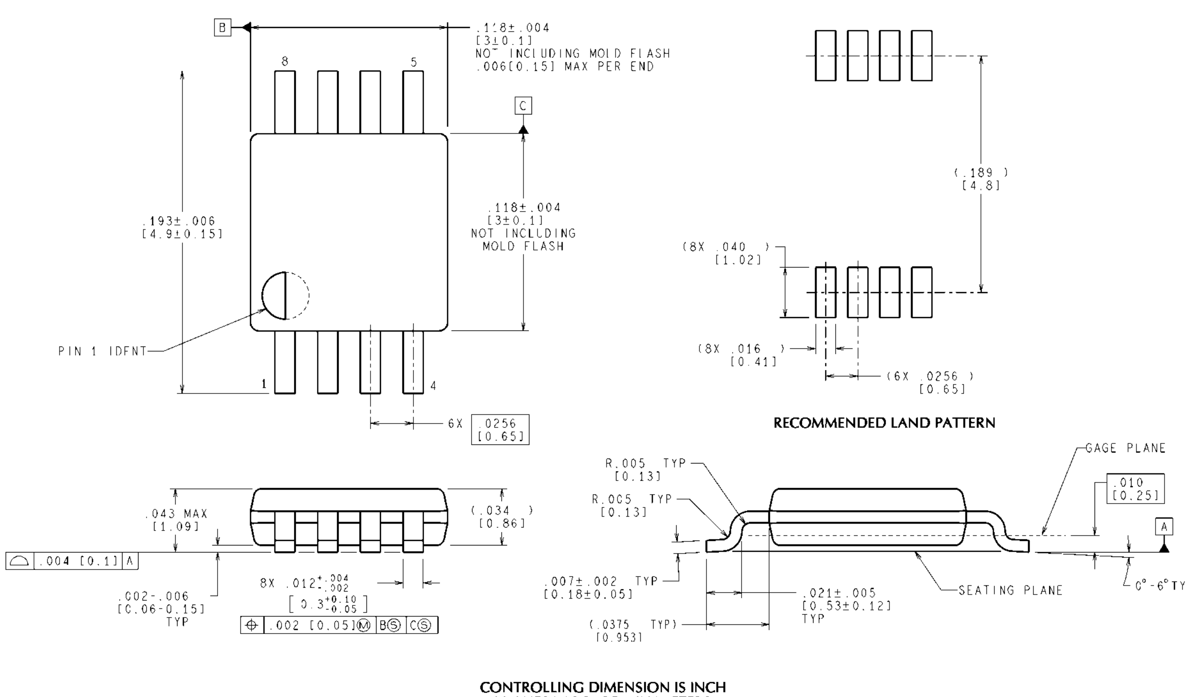
866926

Physical Dimensions inches (millimeters) unless otherwise noted



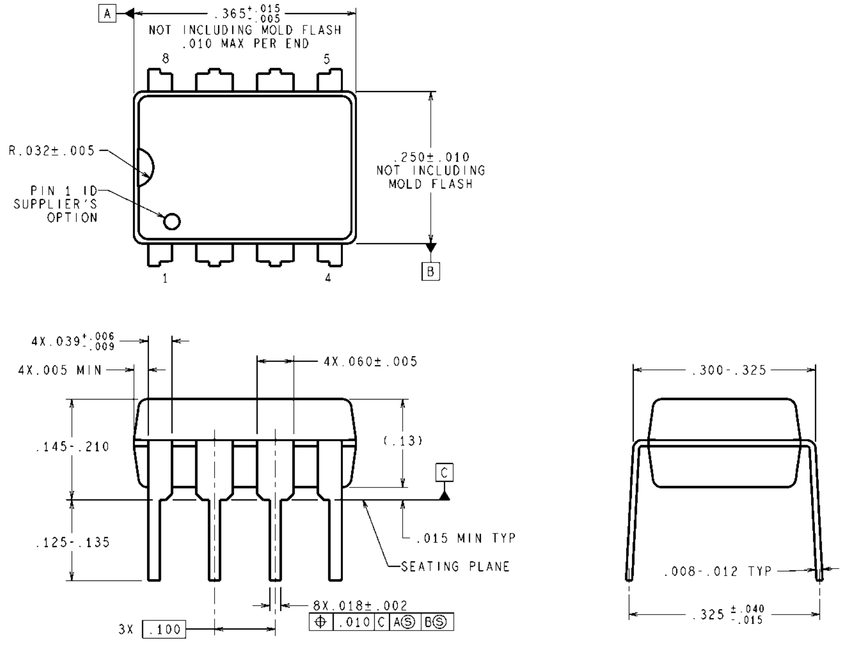
M08A (Rev M)

Molded Small Outline (SO) Package (M)
NS Package Number M08A



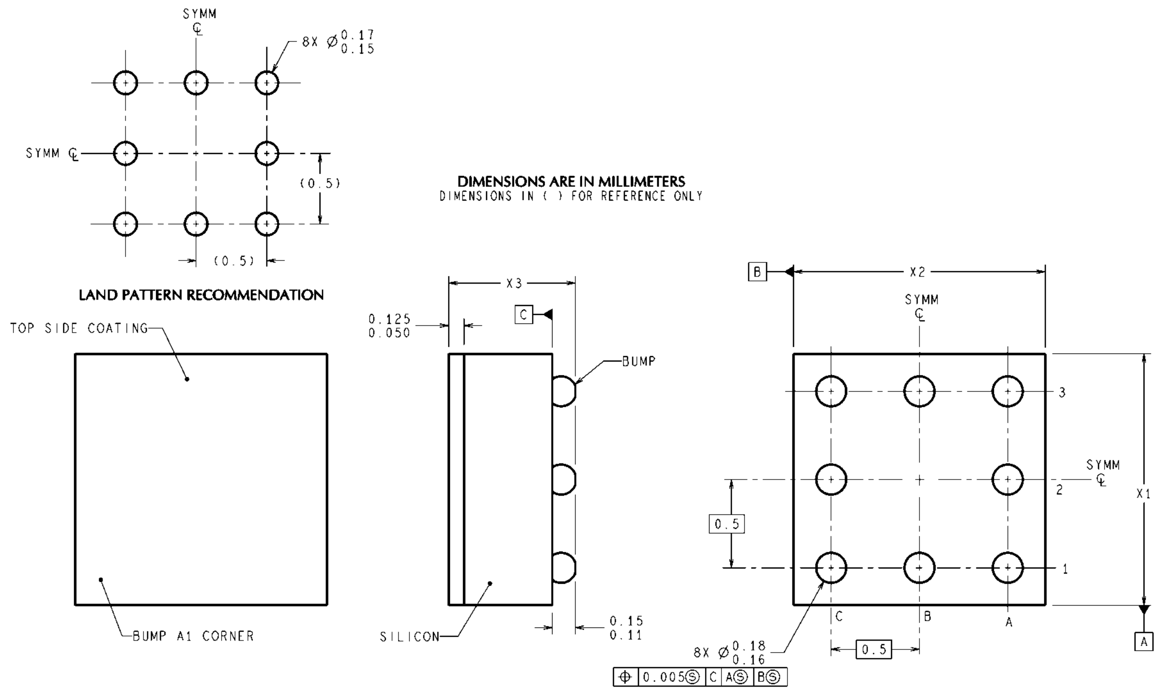
MUA08A (Rev F)

8-Pin (0.118" Wide) Molded Mini Small Outline Package
NS Package Number MUA08A



N08E (Rev G)

Molded Dual-in-line Package (N)
NS Package Number N08E



NOTES: UNLESS OTHERWISE SPECIFIED

1. EPOXY COATING
2. FOR SOLDER BUMP COMPOSITION, SEE “SOLDER INFORMATION” IN THE PACKAGING SECTION OF THE NATIONAL SEMICONDUCTOR WEB PAGE (www.national.com).
3. RECOMMEND NON-SOLDER MASK DEFINED LANDING PAD.
4. PIN A1 IS ESTABLISHED BY LOWER LEFT CORNER WITH RESPECT TO TEXT ORIENTATION.
5. XXX IN DRAWING NUMBER REPRESENTS PACKAGE SIZE VARIATION WHERE X1 IS PACKAGE WIDTH, X2 IS PACKAGE LENGTH AND X3 IS PACKAGE HEIGHT.
6. REFERENCE JEDEC REGISTRATION MO-211, VARIATION BC.

8-Bump micro SMD Package
NS Package Number TPA08FGA
X_1 = 1.412 X_2 = 1.438 X_3 = 0.500

Notes

Notes

For more National Semiconductor product information and proven design tools, visit the following Web sites at:
www.national.com

Products		Design Support	
Amplifiers	www.national.com/amplifiers	WEBENCH® Tools	www.national.com/webench
Audio	www.national.com/audio	App Notes	www.national.com/appnotes
Clock and Timing	www.national.com/timing	Reference Designs	www.national.com/refdesigns
Data Converters	www.national.com/adc	Samples	www.national.com/samples
Interface	www.national.com/interface	Eval Boards	www.national.com/evalboards
LVDS	www.national.com/lvds	Packaging	www.national.com/packaging
Power Management	www.national.com/power	Green Compliance	www.national.com/quality/green
Switching Regulators	www.national.com/switchers	Distributors	www.national.com/contacts
LDOs	www.national.com/ldo	Quality and Reliability	www.national.com/quality
LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback
Voltage References	www.national.com/vref	Design Made Easy	www.national.com/easy
PowerWise® Solutions	www.national.com/powerwise	Applications & Markets	www.national.com/solutions
Serial Digital Interface (SDI)	www.national.com/sdi	Mil/Aero	www.national.com/milaero
Temperature Sensors	www.national.com/tempsensors	SolarMagic™	www.national.com/solarmagic
PLL/VCO	www.national.com/wireless	PowerWise® Design University	www.national.com/training

For the most current product information visit us at www.national.com

National Semiconductor Americas Technical Support Center
Email: support@nsc.com
Tel: 1-800-272-9959

National Semiconductor Europe Technical Support Center
Email: europe.support@nsc.com

National Semiconductor Asia Pacific Technical Support Center
Email: ap.support@nsc.com

National Semiconductor Japan Technical Support Center
Email: jpn.feedback@nsc.com