TEXAS INSTRUMENTS

LMZ10501

1A SIMPLE SWITCHER® Nano Module with 5.5V Maximum Input Voltage

Electrical Specifications

- Up to 1A output current
- Input voltage range 2.7V to 5.5V
- Output voltage range 0.6V to 3.6V
- Efficiency up to 95%

Key Features

- Integrated inductor
- Miniature form factor (3.0 mm x 2.5 mm x 1.425 mm)
- 8-pin LLP footprint
- -40°C to 125°C junction temperature range
- Adjustable output voltage
- 2.0MHz fixed PWM switching frequency
- Integrated compensation
- Soft start function
- Current limit protection
- Thermal shutdown protection
- Input voltage UVLO for power-up, power-down, and brown-out conditions
- Only 5 external components — resistor divider and 3 ceramic capacitors

Applications

- Point of load conversions from 3.3V and 5V rails
- Space constrained applications
- Low output noise applications

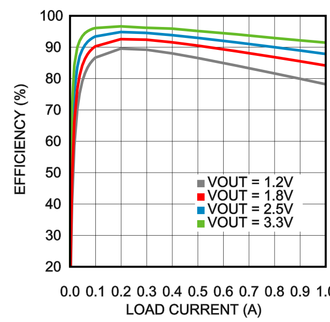
Performance Benefits

- Small solution size
- Low output voltage ripple
- Easy component selection and simple PCB layout
- High efficiency reduces system heat generation

System Performance

(Quick Overview Links: V_{OUT} = *1.2V*, *1.8V*, *2.5V*, *3.3V*)

Typical Efficiency at V_{IN} = 3.6V



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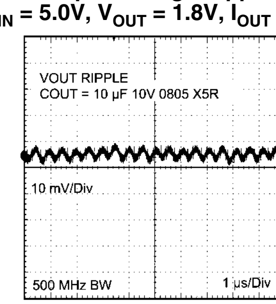
Output Voltage Ripple
V_{IN} = 5.0V, V_{OUT} = 1.8V, I_{OUT} = 1A



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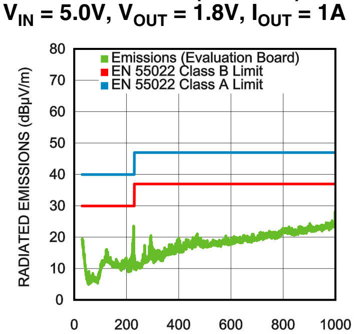
Radiated EMI (CISPR22)
V_{IN} = 5.0V, V_{OUT} = 1.8V, I_{OUT} = 1A



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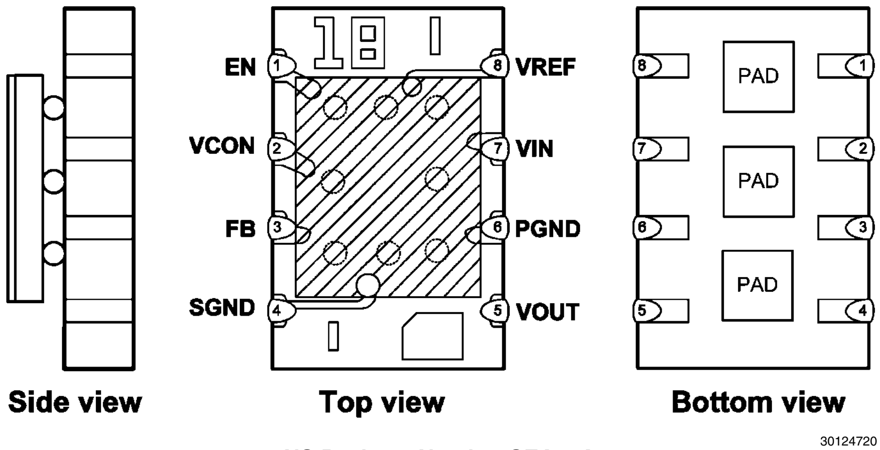
Connection Diagram



NS Package Number SEA08A

Order Information

Order Number	Package Marking (Note)	Supplied As
LMZ10501SHE	XT SP	250 units, Tape-and-Reel
LMZ10501SH	XT SP	1000 units, Tape-and-Reel
LMZ10501SHX	XT SP	3000 units, Tape-and-Reel

Note: The actual physical placement of the package marking will vary from part to part. The package marking “X” designates the date code. “T” is an internal code for die traceability. Both "X" and "T" will vary in production. “SP” identifies the device (part number).

Pin Descriptions

Pin #	Name	Description
1	EN	Enable Input. Set this digital input higher than 1.2V for normal operation. For shutdown, set low. Pin is internally pulled up to VIN and can be left floating for always-on operation.
2	VCON	Output voltage control pin. Connect to analog voltage from resisitve divider or DAC/controller to set the VOUT voltage. $V_{OUT} = 2.5 \times V_{CON}$. Connect a small (470pF) capacitor from this pin to SGND to provide noise filtering.
3	FB	Feedback of the error amplifier. Connect directly to output capacitor to sense V_{OUT}.
4	SGND	Ground for analog and control circuitry. Connect to PGND at a single point.
5	VOUT	Output Voltage. Connected to one terminal of the integrated inductor. Connect output filter capacitor between VOUT and PGND.
6	PGND	Power ground for the power MOSFETs and gate-drive circuitry.
7	VIN	Voltage supply input. Connect ceramic capacitor between VIN and PGND as close as possible to these two pins. Typical capacitor values are between 4.7µF and 22µF.
8	VREF	2.35V voltage reference output. Typically connected to VCON pin through a resistive divider to set the output voltage.
	PAD	The 3 pads underneath the module are not internally connected to any node. These pads should be connected to the ground plane for improved thermal performance.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

VIN, VREF to SGND	−0.2V to +6.0V
PGND to SGND	−0.2V to +0.2V
EN, FB, VCON	(SGND −0.2V) to (VIN +0.2V) w/6.0V max
VOUT	(PGND −0.2V) to (VIN +0.2V) w/6.0V max
Junction Temperature (T_{J-MAX})	+150°C
Storage Temperature Range	−65°C to +150°C
Maximum Lead Temperature	+260°C
ESD Susceptibility(Note 2)	±2kV

Operating Ratings (Note 1)

Input Voltage Range	2.7V to 5.5V
Recommended Load Current	0 mA to 1000 mA
Junction Temperature (T_J) Range	−40°C to +125°C

Thermal Properties

Junction-to-Ambient Thermal Resistance (θ_{JA}), SEA08A Package (Note 3)	120°C/W

Electrical Characteristics

(Note 4) Specifications with standard typeface are for T_J = 25°C only; Limits in **bold face** type apply over the operating junction temperature range T_J of -40°C to 125°C. Minimum and maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 3.6V, V_{EN} = 1.2V.

Symbol	Parameter	Conditions	Min (Note 4)	Typ (Note 5)	Max (Note 4)	Units
SYSTEM PARAMETERS						
V_{REF} x GAIN	Reference voltage x VCON to FB Gain	$V_{IN} = V_{EN}$ = 5.5V, V_{CON} = 1.44V	**5.7575**	5.875	**5.9925**	V
GAIN	VCON to FB Gain	V_{IN} = 5.5V, V_{CON} = 1.44V	**2.4375**	2.5	**2.5750**	V/V
VIN_{UVLO}	VIN rising threshold			2.4		V
VIN_{UVLO}	VIN falling theshold			2.25		V
I_{SHDN}	Shutdown supply current	V_{IN} = 3.6V, V_{EN} = 0.5V (Note 6)		11	**18**	µA
I_q	DC bias current into VIN	V_{IN} = 5.5V, V_{CON} = 1.6V, I_{OUT} = 0A		6.5	**8.5**	mA
$R_{DROPOUT}$	V_{IN} to V_{OUT}resistance	I_{OUT} = 200 mA		285	**425**	mΩ
I_{LIM}	DC Output Current Limit	V_{CON} = 0.24V (Note 7)	**1125**	1350		mA
F_{OSC}	Internal oscillator frequency		1.75	2.0	2.25	MHz
$V_{IH,ENABLE}$	Enable logic HIGH voltage		**1.2**			V
$V_{IL,ENABLE}$	Enable logic LOW voltage				**0.5**	V
T_{SD}	Thermal shutdown	Rising Threshold		150		°C
$T_{SD-HYST}$	Thermal shutdown hysteresis			20		°C
D_{MAX}	Maximum duty cycle			100		%
T_{ON-MIN}	Minimum on-time			50		ns

Symbol	Parameter	Conditions	Min (Note 4)	Typ (Note 5)	Max (Note 4)	Units
SYSTEM PARAMETERS						
θ_{JA}	Package Thermal Resistance	20mm x 20mm board 2 layers, 2 oz copper, 0.5W, no airlow		118		°C/W
		15mm x 15mm board 2 layers, 2 oz copper, 0.5W, no airlow		132		
		10mm x 10mm board 2 layers, 2 oz copper, 0.5W, no airlow		157		

System Characteristics

The following specifications are guaranteed by design providing the component values in the Typical Application Circuit are used (C_{IN} = C_{OUT} = 10 µF, 6.3V, 0603, TDK C1608X5R0J106K). **These parameters are not guaranteed by production testing.** Unless otherwise stated the following conditions apply: T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$\Delta V_{OUT}/V_{OUT}$	Output Voltage Regulation Over Line Voltage and Load Current	V_{OUT} = 0.6V ΔV_{IN} =2.7V to 4.2V ΔI_{OUT} = 0A to 1A		±1.75		%
$\Delta V_{OUT}/V_{OUT}$	Output Voltage Regulation Over Line Voltage and Load Current	V_{OUT} = 1.5V ΔV_{IN} = 2.7V to 5.5V ΔI_{OUT} = 0A to 1A		±0.92		%
$\Delta V_{OUT}/V_{OUT}$	Output Voltage Regulation Over Line Voltage and Load Current	V_{OUT} = 3.6V ΔV_{IN} = 4.0V to 5.5V ΔI_{OUT} = 0A to 1A		±0.38		%
VREF T_{RISE}	Rise time of reference voltage	EN = Low to High, V_{IN} = 4.2V V_{OUT} = 2.7V, I_{OUT} = 1A		10		µs
η	Peak Efficiency	V_{IN} = 5.0V, V_{OUT} = 3.3V I_{OUT} = 200 mA		95		%
	Full Load Efficiency	V_{IN} = 5.0V, V_{OUT} = 3.6V I_{OUT} = 1000 mA		91		
V_{OUT} Ripple	Output voltage ripple	V_{IN} = 5.0V, V_{OUT} = 1.8V I_{OUT} = 1000 mA (Note 8)		10		mV pk-pk
Line Transient	Line transient response	VIN = 2.7V to 5.5V, T_R = T_F= 10 µs, VOUT = 1.8V, I_{OUT} = 1000mA		30		mV pk-pk
Load Transient	Load transient response	VIN = 5.0V T_R = T_F = 40 µs, V_{OUT} = 1.8V I_{OUT} = 100mA to 1000 mA		30		mV pk-pk

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: The human body model is a 100pF capacitor discharged through a 1.5 kΩ resistor into each pin. Test method is per JESD-22-114.

Note 3: Junction-to-ambient thermal resistance (θ_{JA}) is based on 4 layer board thermal measurements, performed under the conditions and guidelines set forth in the JEDEC standards JESD51-1 to JESD51-11. θ_{JA} varies with PCB copper area, power dissipation, and airflow.

Note 4: Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate the Average Outgoing Quality Level (AOQL).

Note 5: Typical numbers are at 25°C and represent the most likely parametric norm.

Note 6: Shutdown current includes leakage current of the high side PFET.

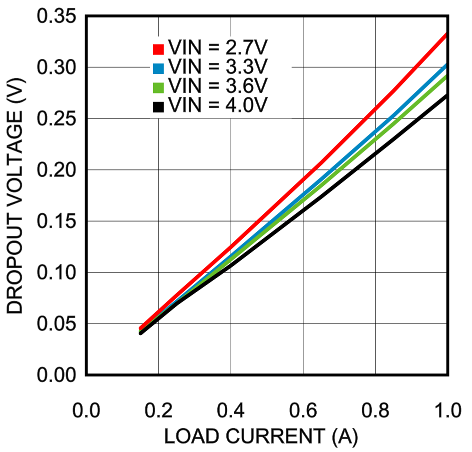
Note 7: Current limit is built-in, fixed, and not adjustable.

Note 8: Ripple voltage should be measured across C_{OUT} on a well-designed PC board using the suggested capacitors.

Typical Performance Characteristics

Unless otherwise specified the following conditions apply: V_{IN} = 3.6V, T_A = 25°C

Dropout Voltage vs Load Current and Input Voltage



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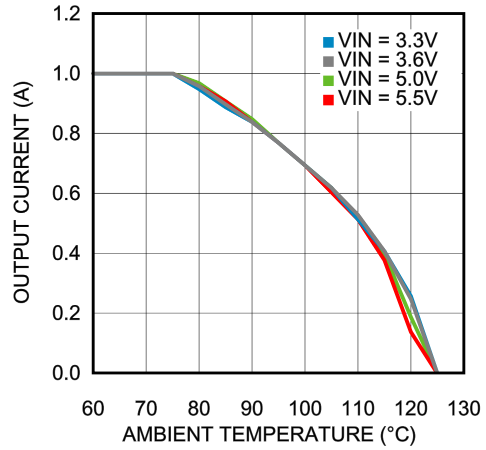
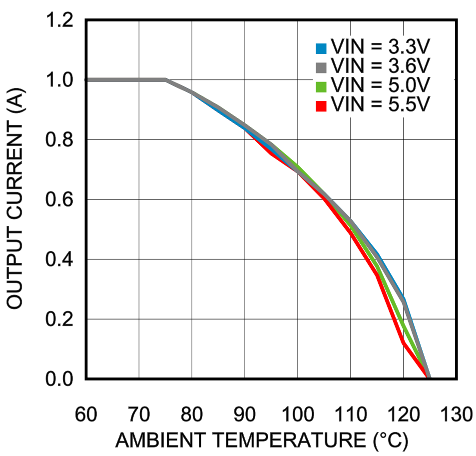
Thermal Derating V_{OUT} = 1.2V, θ_{JA} = 120°C/W



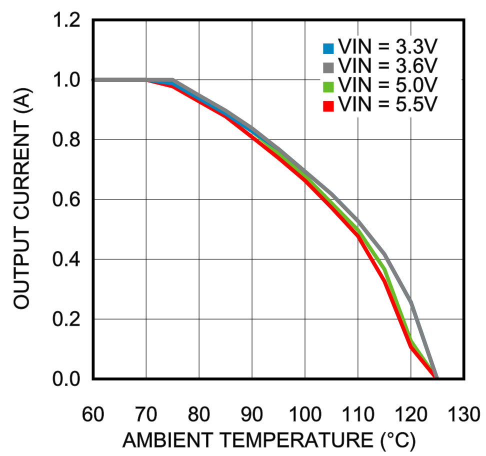
30124744

Thermal Derating V_{OUT} = 1.8V, θ_{JA} = 120°C/W



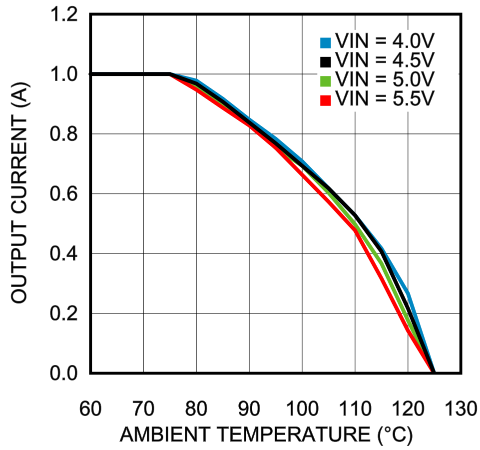
30124743

Thermal Derating V_{OUT} = 2.5V, θ_{JA} = 120°C/W



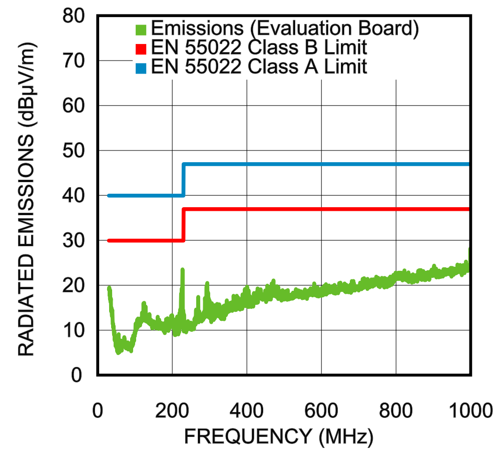
30124742

Thermal Derating V_{OUT} = 3.3V, θ_{JA} = 120°C/W



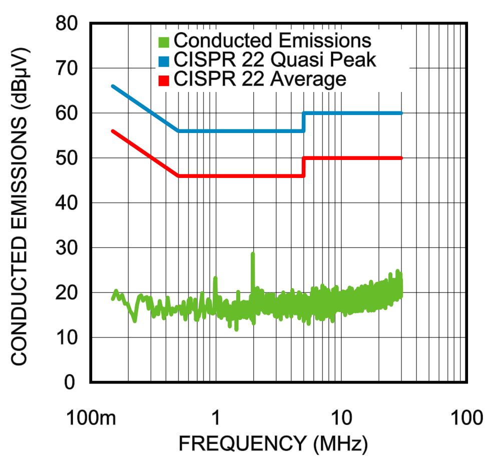
30124741

Radiated EMI (CISPR22)
V_{IN} = 5.0V, V_{OUT} = 1.8V, I_{OUT} = 1A
Default evaluation board BOM



30124732

Conducted EMI
V_{IN} = 5.0V, V_{OUT} = 1.8V, I_{OUT} = 1A
Default evaluation board BOM with additional 1µH 1µF LC input filter



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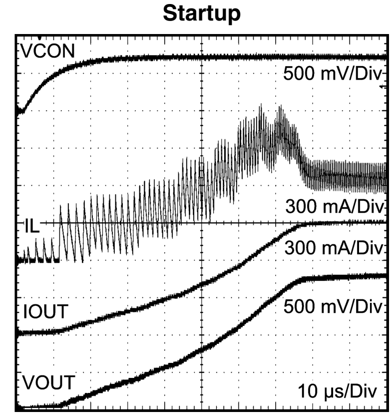
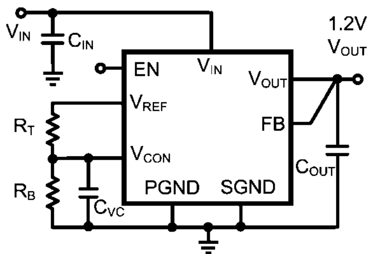
Startup



30124734

1.2V

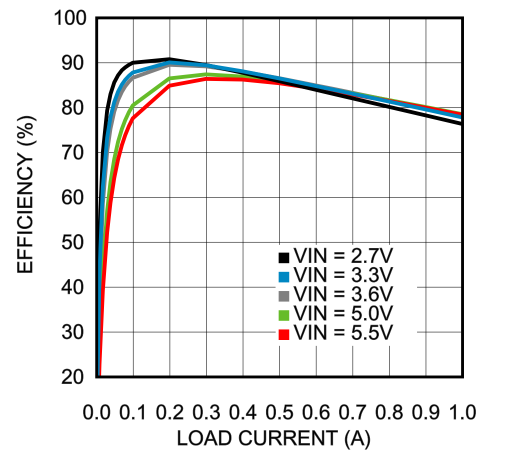
Schematic V_{OUT} = 1.2V



C_{IN}	10 µF	≥ 6.3V	0805	X7R or X5R
C_{OUT}	10 µF	≥ 6.3V	0805	X7R or X5R
C_{VC}	470 pF	≥ 6.3V	0603	X7R or X5R
R_T	243 kΩ	1%	0603	
R_B	63.4 kΩ	1%	0603	

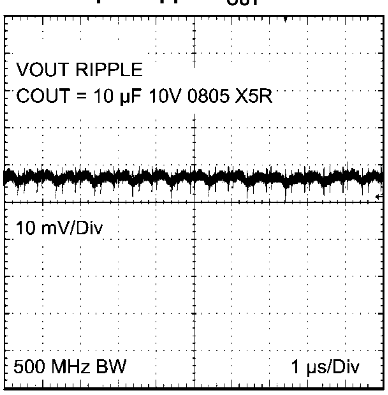
30124722

Efficiency V_{OUT} = 1.2V



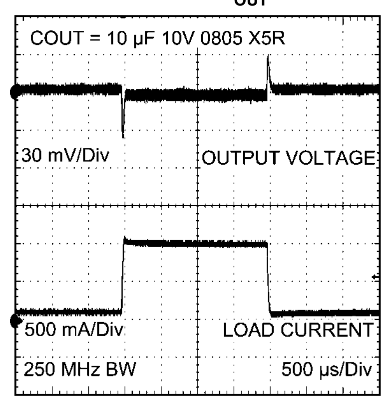
30124727

Output Ripple V_{OUT} = 1.2V



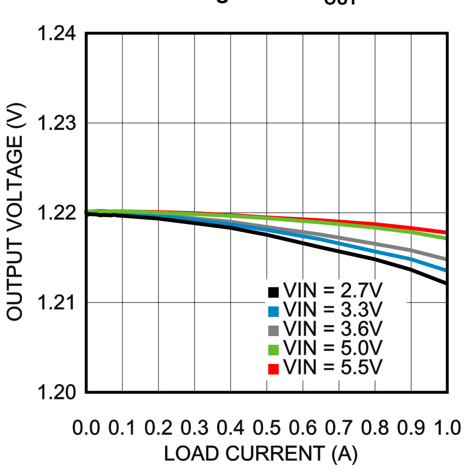
30124755

Load Transient V_{OUT} = 1.2V



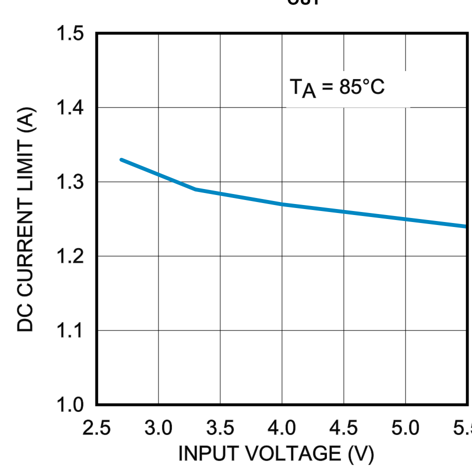
30124757

Line and Load Regulation V_{OUT} = 1.2V



30124737

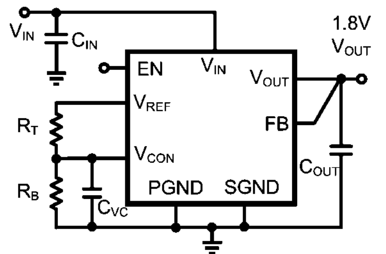
DC Current Limit V_{OUT} = 1.2V



30124751

1.8V

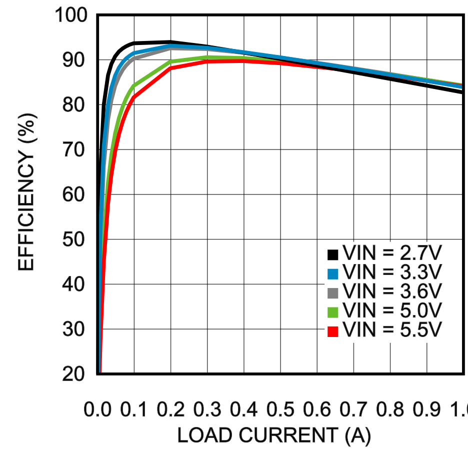
Schematic V_{OUT} = 1.8V



C_{IN}	10 µF	≥ 6.3V	0805	X7R or X5R
C_{OUT}	10 µF	≥ 6.3V	0805	X7R or X5R
C_{VC}	470 pF	≥ 6.3V	0603	X7R or X5R
R_T	187 kΩ	1%	0603	
R_B	82.5 kΩ	1%	0603	

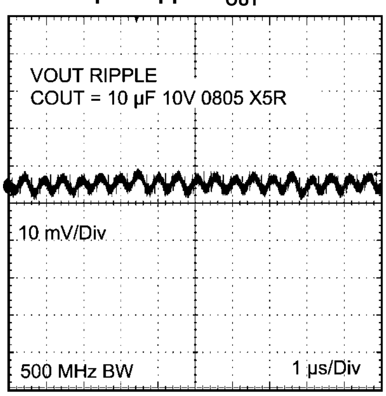
30124723

Efficiency V_{OUT} = 1.8V



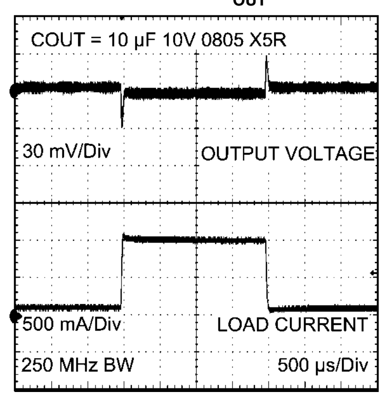
30124726

Output Ripple V_{OUT} = 1.8V



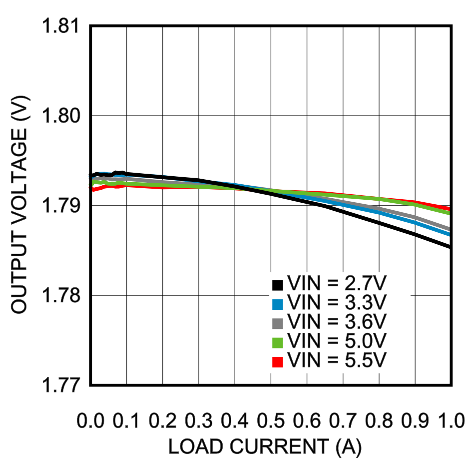
30124733

Load Transient V_{OUT} = 1.8V



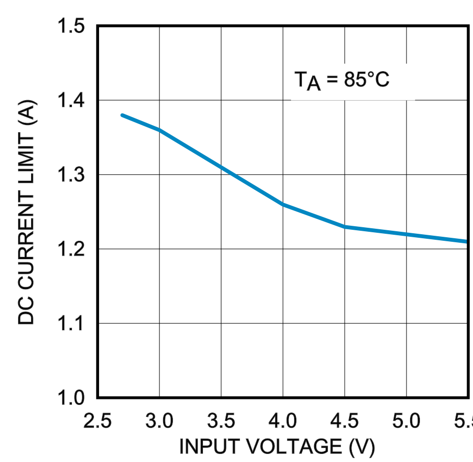
30124758

Line and Load Regulation V_{OUT} = 1.8V



30124738

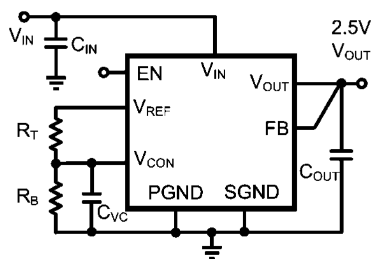
DC Current Limit V_{OUT} = 1.8V



30124752

2.5V

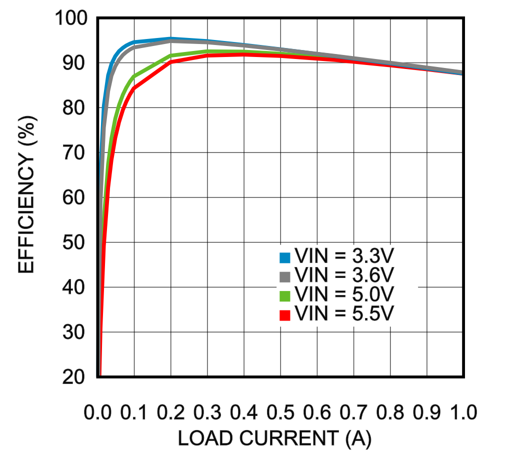
Schematic V_{OUT} = 2.5V



C_{IN}	10 µF	≥ 6.3V	0805	X7R or X5R
C_{OUT}	10 µF	≥ 6.3V	0805	X7R or X5R
C_{VC}	470 pF	≥ 6.3V	0603	X7R or X5R
R_T	150 kΩ	1%	0603	
R_B	118 kΩ	1%	0603	

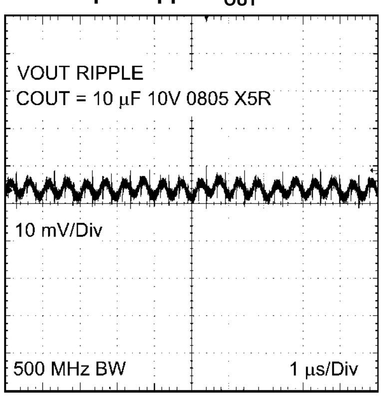
30124724

Efficiency V_{OUT} = 2.5V



30124728

Output Ripple V_{OUT} = 2.5V



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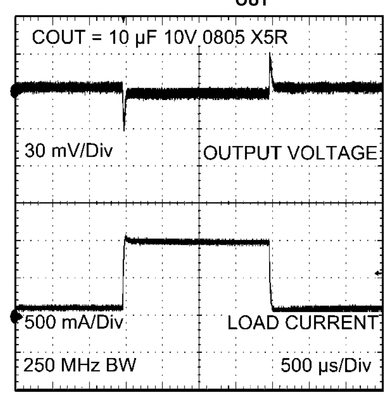
Load Transient V_{OUT} = 2.5V



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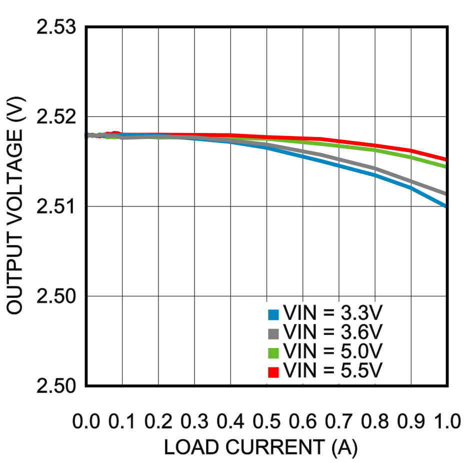
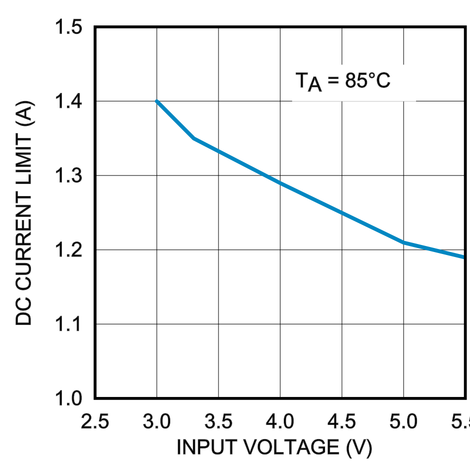
Line and Load Regulation V_{OUT} = 2.5V



30124739

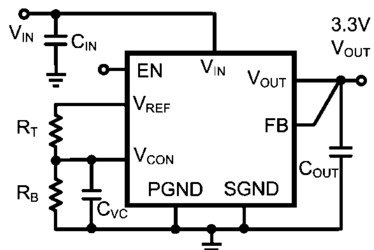
DC Current Limit V_{OUT} = 2.5V



30124753

3.3V

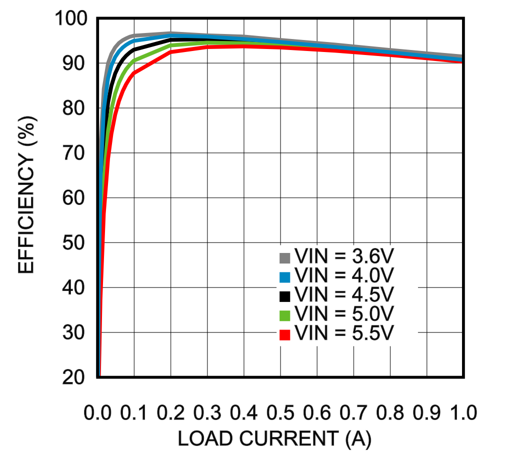
Schematic V_{OUT} = 3.3V



C_{IN}	10 µF	≥ 6.3V	0805	X7R or X5R
C_{OUT}	10 µF	≥ 6.3V	0805	X7R or X5R
C_{VC}	470 pF	≥ 6.3V	0603	X7R or X5R
R_T	118 kΩ	1%	0603	
R_B	150 kΩ	1%	0603	

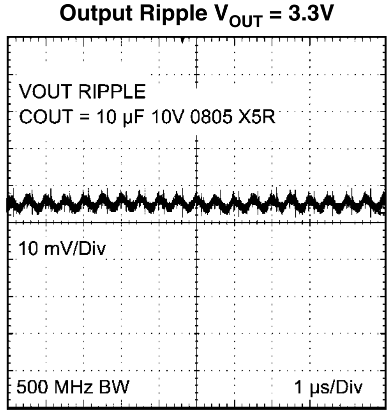
30124725

Efficiency V_{OUT} = 3.3V



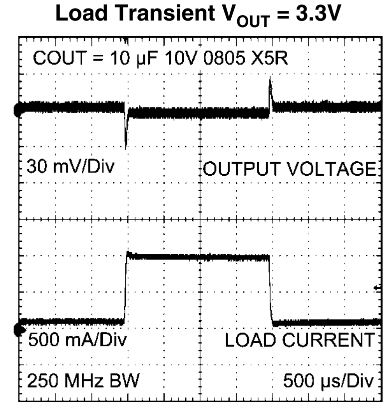
30124729

Output Ripple V_{OUT} = 3.3V



30124756

Load Transient V_{OUT} = 3.3V



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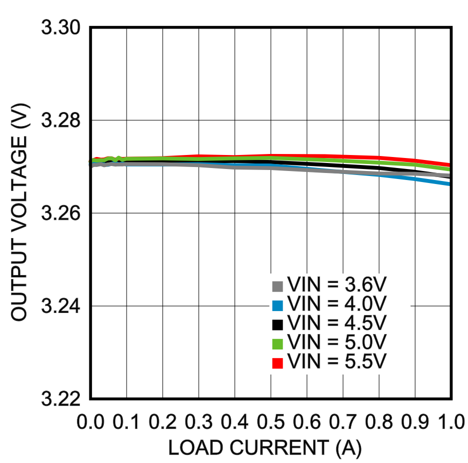
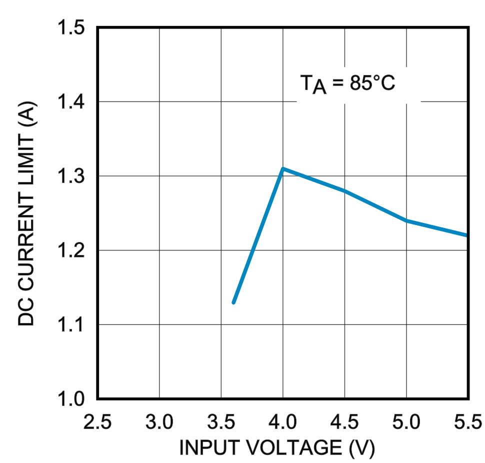
Line and Load Regulation V_{OUT} = 3.3V



30124740

DC Current Limit V_{OUT} = 3.3V



30124754

Block Diagram

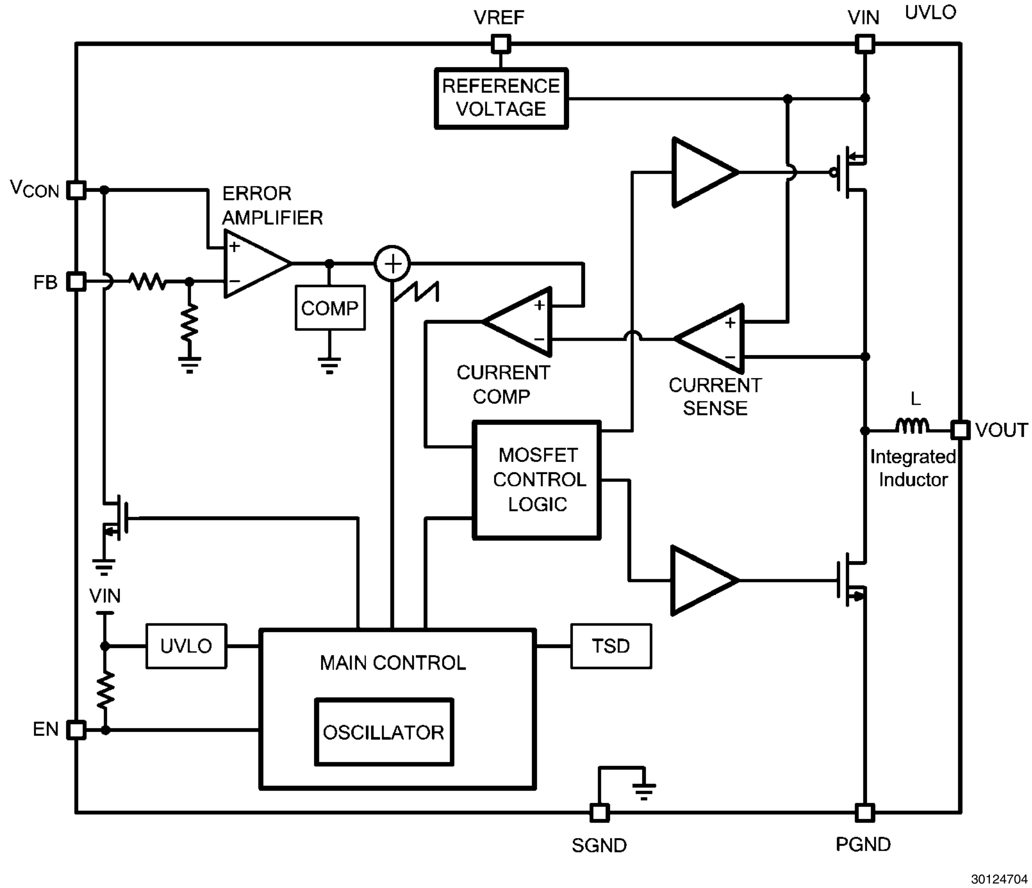


FIGURE 1. Functional Block Diagram

Overview

The LMZ10501 SIMPLE SWITCHER® nano module is an easy-to-use step-down DC-DC solution capable of driving up to 1A load in space-constrained applications. Only an input capacitor, an output capacitor, a small V_{CON} filter capacitor, and two resistors are required for basic operation. The nano module comes in 8-pin LLP footprint package with an integrated inductor. The LMZ10501 operates in fixed 2.0MHz PWM (Pulse Width Modulation) mode, and is designed to deliver power at maximum efficiency. The output voltage is typically set by using a resistive divider between the built-in reference voltage V_{REF} and the control pin V_{CON}. The V_{CON} pin is the positive input to the error amplifier. The output voltage of the LMZ10501 can also be dynamically adjusted between 0.6V and 3.6V by driving the V_{CON} pin externally. Internal current limit based softstart function, current overload protection, and thermal shutdown are also provided.

CIRCUIT OPERATION

The LMZ10501 is a synchronous Buck power module using a PFET for the high side switch and an NFET for the synchronous rectifier switch. The output voltage is regulated by modulating the PFET switch on-time. The circuit generates a duty-cycle modulated rectangular signal. The rectangular signal is averaged using a low pass filter formed by the integrated inductor and an output capacitor. The output voltage is equal to the average of the duty-cycle modulated rectangular signal. In PWM mode, the switching frequency is constant. The energy per cycle to the load is controlled by modulating the PFET on-time, which controls the peak inductor current. In current mode control architecture, the inductor current is compared with the slope compensated output of the error amplifier. At the rising edge of the clock, the PFET is turned ON, ramping up the inductor current with a slope of $(V_{IN} - V_{OUT})/L$. The PFET is ON until the current signal equals the error signal. Then the PFET is turned OFF and NFET is turned ON, ramping down the inductor current with a slope of V_{OUT} /L. At the next rising edge of the clock, the cycle repeats. An increase of load pulls the output voltage down, resulting in an increase of the error signal. As the error signal goes up, the peak inductor current is increased, elevating the average inductor current and responding to the heavier load. To ensure stability, a slope compensation ramp is subtracted from the error signal and internal loop compensation is provided.

INPUT UNDER VOLTAGE DETECTION

The LMZ10501 implements an under voltage lock out (UVLO) circuit to ensure proper operation during startup, shutdown and input supply brownout conditions. The circuit monitors the voltage at the V_{IN} pin to ensure that sufficient voltage is present to bias the regulator. If the under voltage threshold is not met, all functions of the controller are disabled and the controller remains in a low power standby state.

SHUTDOWN MODE

To shutdown the LMZ10501, pull the EN pin low (<0.5V). In the shutdown mode all internal circuits are turned OFF.

EN PIN OPERATION

The EN pin is internally pulled up to V_{IN} through a 790kΩ (typ.) resistor. This allows the nano module to be enabled by default when the EN pin is left floating. In such cases V_{IN} will set EN high when V_{IN} reaches 1.2V. As the input voltage continues to rise, operation will start once V_{IN} exceeds the under-voltage lockout (UVLO) threshold. To set EN high externally, pull it up to 1.2V or higher. Note that the voltage on EN must remain at less than VIN+ 0.2V due to absolute maximum ratings of the device.

INTERNAL SYNCHRONOUS RECTIFICATION

The LMZ10501 uses an internal NFET as a synchronous rectifier to minimize the switch voltage drop and increase efficiency. The NFET is designed to conduct through its intrinsic body diode during the built-in dead time between the PFET on-time and the NFET on-time. This eliminates the need for an external diode. The dead time between the PFET and NFET connection prevents shoot through current from V_{IN} to PGND during the switching transitions.

CURRENT LIMIT

The LMZ10501 current limit feature protects the module during an overload condition. The circuit employs positive peak current limit in the PFET and negative peak current limit in the NFET switch. The positive peak current through the PFET is limited to 1.7A (typ.). When the current reaches this limit threshold the PFET switch is immediately turned off until the next switching cycle. This behavior continues on a cycle-by-cycle basis until the overload condition is removed from the output. The typical negative peak current limit through the NFET switch is -0.6A (typ.).

The ripple of the inductor current depends on the input and output voltages. This means that the DC level of the output current when the peak current limiting occurs will also vary over the line voltage and the output voltage level. Refer to the DC Output Current Limit plots in the Typical Performance Characteristics section for more information.

STARTUP BEHAVIOR AND SOFTSTART

The LMZ10501 features a current limit based soft start circuit in order to prevent large in-rush current and output overshoot as V_{OUT} is ramping up. This is achieved by gradually increasing the PFET current limit threshold to the final operating value as the output voltage ramps during startup. The maximum allowed current in the inductor is stepped up in a staircase profile for a fixed number of switching periods in each step. Additionally, the switching frequency in the first step is set at 450kHz and is then increased for each of the following steps until it reaches 2MHz at the final step of current limiting. This current limiting behavior is illustrated in the following figure and allows for a smooth V_{OUT} ramp up.

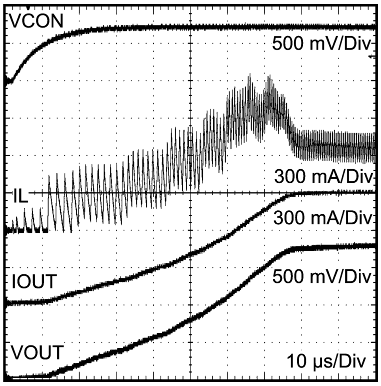


FIGURE 2. Startup behavior of current limit based softstart.

The soft start rate is also limited by the V_{CON} ramp up rate. The V_{CON} pin is discharged internally through a pull down device before startup occurs. This is done to deplete any residual charge on the V_{CON} filter capacitor and allow the V_{CON} voltage to ramp up from 0V when the part is started. The events that cause V_{CON} discharge are thermal shutdown, UVLO, EN low, or output short circuit detection. The minimum recommended capacitance on V_{CON} is 220pF and the maximum is 1nF. The duration of startup current limiting sequence takes approximately 75µs. After the sequence is completed, the feedback voltage is monitored for output short circuit events.

OUTPUT SHORT CIRCUIT PROTECTION

In addition to cycle by cycle current limit, the LMZ10501 features a second level of short circuit protection. If the load pulls the output voltage down and the feedback voltage falls to 0.375V, the output short circuit protection will engage. In this mode the internal PFET switch is turned OFF after the current limit comparator trips and the beginning of the next cycle is inhibited for approximately 230µs. This forces the inductor current to ramp down and limits excessive current draw from the input supply when the output of the regulator is shorted. The synchronous rectifier is always OFF in this mode. After 230µs of non-switching a new startup sequence is initiated. During this new startup sequence the current limit is gradually stepped up to the nominal value as illustrated in the *STARTUP BEHAVIOR AND SOFTSTART* section. After the startup sequence is completed again, the feedback voltage is monitored for output short circuit. If the short circuit is still persistent after the new startup sequence, switching will be stopped again and there will be another 230µs off period. A persistent output short condition results in a hiccup behavior where the LMZ10501 goes through the normal startup sequence, then detects the output short at the end of startup, terminates switching for 230µs, and repeats this cycle until the output short is released. This behavior is illustrated in the following figure.

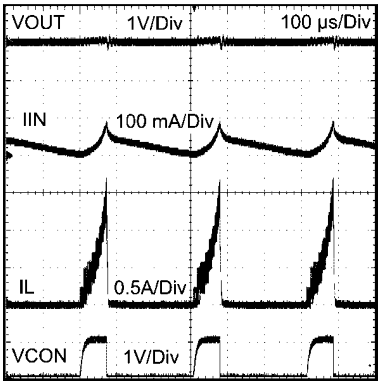


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FIGURE 3. Hiccup behavior with persistent output short circuit.

Since the output current is limited during normal startup by the softstart function, the current charging the output capacitor is also limited. This results in a smooth V_{OUT} ramp up to nominal voltage. However, using excessively large output capacitance or V_{CON} capacitance under normal conditions can prevent the output voltage from reaching 0.375V at the end of the startup sequence. In such cases the module will maintain the described above hiccup mode and the output voltage will not ramp up to final value. To cause this condition, one would have to use unnecessarily large output capacitance for 1A load applications. See the *INPUT AND OUTPUT CAPACITOR SELECTION* section for guidance on maximum capacitances for different output voltage settings.

HIGH DUTY CYCLE OPERATION

The LMZ10501 features a transition mode designed to extend the output regulation range to the minimum possible input voltage. As the input voltage decreases closer and closer to V_{OUT}, the off-time of the PFET gets smaller and smaller and the duty cycle eventually needs to reach 100% to support the output voltage. The input voltage at which the duty cycle reaches 100% is the edge of regulation. When the LMZ10501 input voltage is lowered, such that the off-time of the PFET reduces to less than 35ns, the LMZ10501 doubles the switching period to extend the off-time for that V_{IN} and maintain regulation. If V_{IN} is lowered even more, the off-time of the PFET will reach the 35ns mark again. The LMZ10501 will then reduce the frequency again, achieving less than 100% duty cycle operation and maintaining regulation. As V_{IN} is lowered even more, the LMZ10501 will continue to scale down the frequency, aiming to maintain at least 35ns off time. Eventually, as the input voltage decreases further, 100% duty cycle is reached. This behavior of extending the V_{IN} regulation range is illustrated in the following plot.

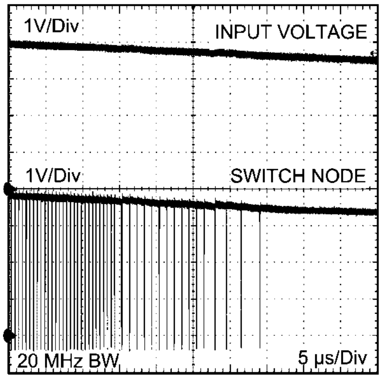

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FIGURE 4. High duty cycle operation and switching frequency reduction.

THERMAL OVERLOAD PROTECTION

The junction temperature of the LMZ10501 should not be allowed to exceed its maximum operating rating of 125°C. Thermal protection is implemented by an internal thermal shutdown circuit which activates at 150°C (typ). When this temperature is reached, the device enters a low power standby state. In this state switching remains off causing the output voltage to fall. Also, the V_{CON} capacitor is discharged to SGND. When the junction temperature falls back below 130 °C (typ) normal startup occurs and V_{OUT} rises smoothly from 0V. Applications requiring maximum output current may require derating at elevated ambient temperature. See the Typical Performance Characteristics section for thermal derating plots for various output voltages.

Application Information

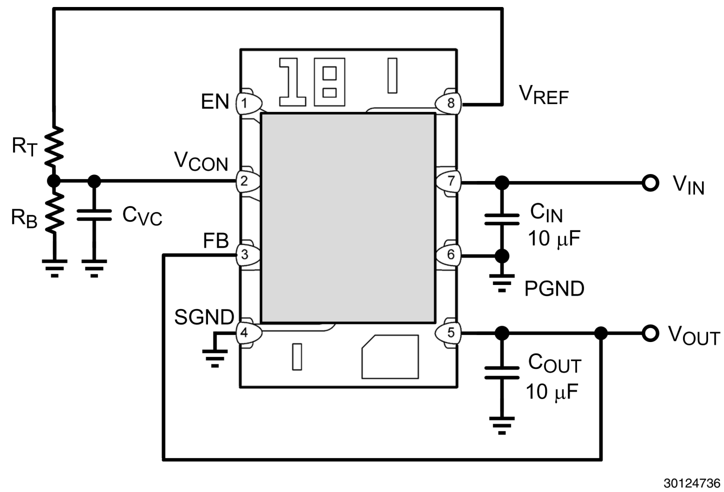


FIGURE 5. Typical Application Circuit

SETTING THE OUTPUT VOLTAGE

The LMZ10501 provides a fixed 2.35V V_{REF} voltage output. As shown in *Figure 5* above, a resistive divider formed by R_T and R_B sets the V_{CON} pin voltage level. The V_{OUT} voltage tracks V_{CON} and is governed by the following relationship:

$$V_{OUT} = GAIN \times V_{CON} \quad (1)$$

where GAIN is 2.5V/V from V_{CON} to V_{FB}.

This equation is valid for output voltages between 0.6V and 3.6V and corresponds to V_{CON} voltage between 0.24V and 1.44V, respectively.

R_T and R_B Selection for Fixed V_{OUT}

The parameters affecting the output voltage setting are the R_T, R_B, and the product of the V_{REF} voltage x GAIN. The V_{REF} voltage is typically 2.35V. Since V_{CON} is derived from V_{REF} via R_T and R_B,

$$V_{CON} = V_{REF} \times R_B / (R_B + R_T) \quad (2)$$

After substitution,

$$V_{OUT} = V_{REF} \times GAIN \times R_B / (R_B + R_T) \quad (3)$$

$$R_T = (GAIN \times V_{REF} / V_{OUT} - 1) \times R_B \quad (4)$$

The ideal product of GAIN x V_{REF} = 5.875V.

Choose R_T to be between 80kΩ and 300kΩ. Then, R_B can be calculated using equation (5) below.

$$R_B = (V_{OUT} / (5.875V - V_{OUT})) \times R_T \quad (5)$$

Note that the resistance of R_T should be ≥ 80kΩ. This ensures that the V_{REF} output current loading is not exceeded and the reference voltage is maintained. The current loading on V_{REF} should not be greater than 30 µA.

OUTPUT VOLTAGE ACCURACY OPTIMIZATION

Each nano module is optimized to achieve high V_{OUT} accuracy. Equation (1) shows that, by design, the output voltage is a function of the V_{CON} voltage and the gain from V_{CON} to V_{FB}. The voltage at V_{CON} is derived from V_{REF}. Therefore, as shown in equation (3), the accuracy of the output voltage is a function of the V_{REF} x GAIN product as well as the tolerance of the R_T and R_B resistors. The typical V_{REF} x GAIN product by design is 5.875V. Each nano module's V_{REF} voltage is trimmed so that this product is as close to the ideal 5.875V value as possible, achieving high V_{OUT} accuracy. See the *Electrical Specifications* section for the V_{REF} x GAIN product tolerance limits.

DYNAMIC OUTPUT VOLTAGE SCALING

The V_{CON} pin on the LMZ10501 can be driven externally by a DAC to scale the output voltage dynamically. The output voltage V_{OUT} = 2.5V/V x V_{CON}. When driving V_{CON} with a source different than V_{REF} place a 1.5kΩ resistor in series with the V_{CON} pin. Current limiting the external V_{CON} helps to protect this pin and allows the V_{CON} capacitor to be fully discharged to 0V after fault conditions.

INTEGRATED INDUCTOR

The LMZ10501 uses a Low Temperature Co-fired Ceramic (LTCC) type 2.6 µH inductor with over 1.2A DC current rating and soft saturation profile for up to 2A. This inductor allows for the 1.425mm maximum package height providing an easy to use, compact solution with reduced EMI.

INPUT AND OUTPUT CAPACITOR SELECTION

The LMZ10501 is designed for use with low ESR multi-layer ceramic capacitors (MLCC) for its input and output filters. Using a 10 µF 0603 or 0805 with 6.3V or 10V rating ceramic input capacitor typically provides sufficient V_{IN} bypass. Use of multiple 4.7 µF or 2.2µF capacitors can also be considered. Ceramic capacitors with X5R and X7R temperature characteristics are recommended for both input and output filters. These provide an optimal balance between small size, cost, reliability, and performance for space sensitive applications.

The DC voltage bias characteristics of the capacitors must be considered when selecting the DC voltage rating and case size of these components. The effective capacitance of an MLCC is typically reduced by the DC voltage bias applied across its terminals. For example, a typical 0805 case size X5R 6.3V 10 µF ceramic capacitor may only have 4.8 µF left in it when a 5.0V DC bias is applied. Similarly, a typical 0603 case size X5R 6.3V 10 µF ceramic capacitor may only have 2.4 µF at the same 5.0V DC. Smaller case size capacitors may have even larger percentage drop in value with DC bias.

The optimum output capacitance value is application dependent. Too small output capacitance can lead to instability due to lower loop phase margin. On the other hand, if the output capacitor is too large, it may prevent the output voltage from reaching the 0.375V required voltage level at the end of the startup sequence. In such cases, the output short circuit protection can be engaged and the nano module will enter a hiccup mode as described in the *OUTPUT SHORT CIRCUIT PROTECTION* section. The table below sets the minimum output capacitance for stability and maximum output capacitance for proper startup for various output voltage settings. Note that the maximum C_{OUT} value in *Table 1* assumes that the filter capacitance on V_{CON} is the maximum recommended value of 1nF and the R_T resistor value is less than 300kΩ. Lower V_{CON} capacitance can extend the maximum C_{OUT} range. There is no great performance benefit in using excessive C_{OUT} values.

TABLE 1. Output Capacitance Range

Output Voltage	Minimum C_{OUT}	Suggested C_{OUT}	Maximum C_{OUT}
0.6V	4.7µF	10µF	47µF
1.0V	3.3µF	10µF	47µF
1.2V	3.3µF	10µF	47µF
1.8V	3.3µF	10µF	68µF
2.5V	3.3µF	10µF	100µF
3.3V	3.3µF	10µF	100µF

Use of multiple 4.7 µF or 2.2µF output capacitors can be considered for reduced effective ESR and smaller output voltage ripple. In addition to the main output capacitor, small 0.1µF – 0.01µF parallel capacitors can be used to reduce high frequency noise.

PACKAGE CONSIDERATIONS

The nano module package includes an LTCC inductor on the bottom and a micro SMD die mounted on top. The die has exposed edges and can be sensitive to ambient light. For applications with direct high intensity ambient red, infrared, LED, or natural light it is recommended to have the device shielded from the light source to avoid abnormal behavior.

Since the die is exposed on top of the package, care should be taken when picking and placing the module on the board.

Use the following recommendations when utilizing machine placement:

- Use 1.06mm (42mil) or smaller nozzle size so that the nozzle head does not touch the outer area of the exposed die.
- Use a soft tip pick and place head.
- Add 0.05mm to the component thickness so that the device will be released 0.05mm (2mil) into the solder paste without putting pressure or splashing the solder paste.
- Slow the pick arm when picking the part from the tape and reel carrier and when depositing the IC on the board.
- If the machine releases the component by force, use minimum force or no more than 3 Newtons.
- For PCBs with surface mount components on both sides, it is suggested to put the LMZ10501 on the top side. In case the application requires bottom side placement, a reflow fixture may be required to protect the module during the second reflow.

For manual placement:

- Use a vacuum pick up hand tool with soft tip head.
- If vacuum pick up tool is not available, use non-metal tweezers and hold the part by the inductor body side terminals rather than the micro SMD die on top.
- Use minimal force when picking and placing the module on the board.
- In case a heat gun is required for rework, make sure that the heat source is pointing at the interface between the inductor and the PCB. Do not apply heat gun directly on top of the component since it may affect the solder joint between the micro SMD and the inductor. Using hot air station provides better temperature control and better controlled air flow than a heat gun.
- Go to the video section at www.ti.com/product/lmz10501 for a quick video on how to solder rework the LMZ10501.

Board Layout Considerations

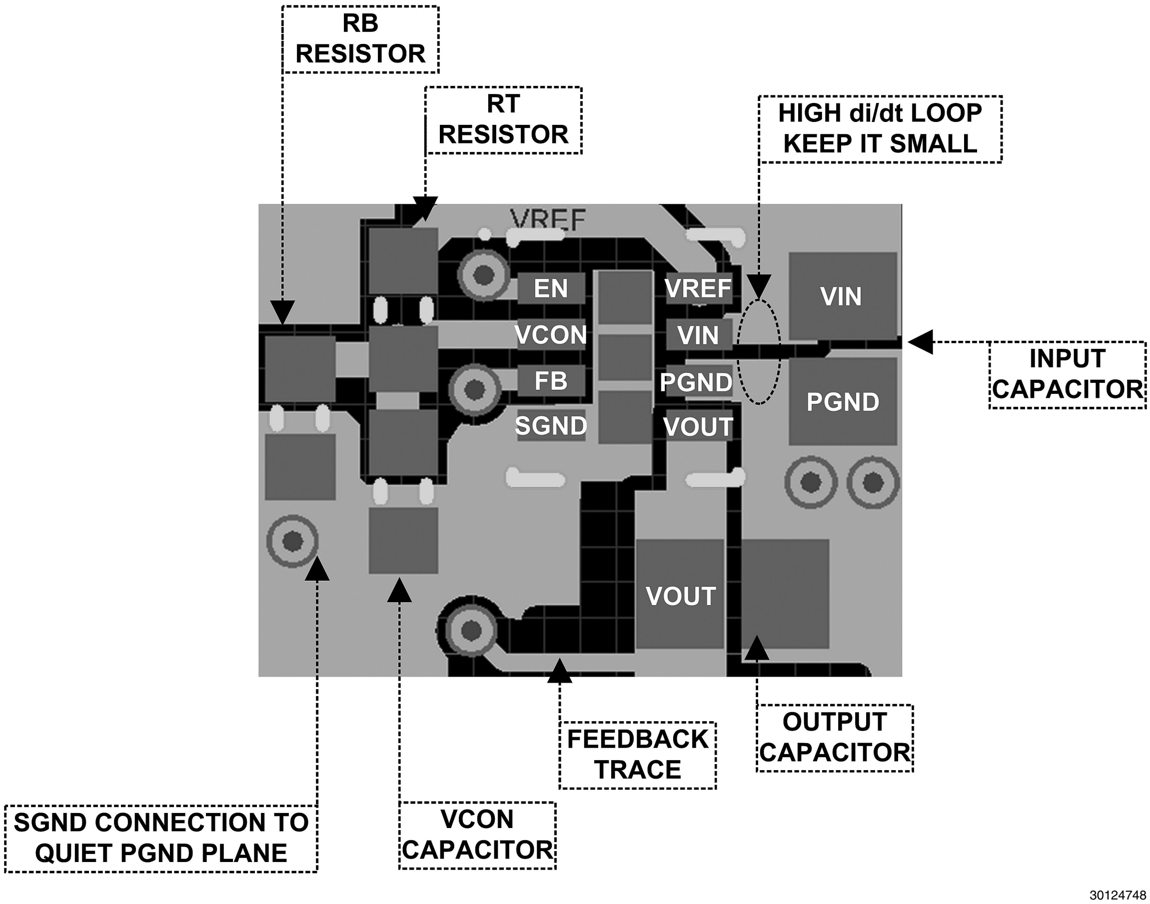


FIGURE 6. Example Top Layer Board Layout

The board layout of any DC-DC switching converter is critical for the optimal performance of the design. Bad PCB layout design can disrupt the operation of an otherwise good schematic design. Even if the regulator still converts the voltage properly, the board layout can mean the difference between passing or failing EMI regulations. In a Buck converter, the most critical board layout path is between the input capacitor ground terminal and the synchronous rectifier ground. The loop formed by the input capacitor and the power FETs is a path for the high di/dt switching current during each switching period. This loop should always be kept as short as possible when laying out a board for any Buck converter.

The LMZ10501 integrates the inductor and simplifies the DC-DC converter board layout. Refer to the example layout in *Figure 6*. There are a few basic requirements to achieve a good LMZ10501 layout.

1. Place the input capacitor C_{IN} as close as possible to the V_{IN} and PGND terminals. V_{IN} (pin 7) and PGND (pin 6) on the LMZ10501 are next to each other which makes the input capacitor placement simple.

2. Place the V_{CON} filter capacitor C_{VC} and the R_B R_T resistive divider as close as possible to the V_{CON} and SGND terminals. The C_{VC} capacitor (not R_B) should be the component closer to the V_{CON} pin, as shown in *Figure 6*. This allows for better bypass of the control voltage set at V_{CON}.

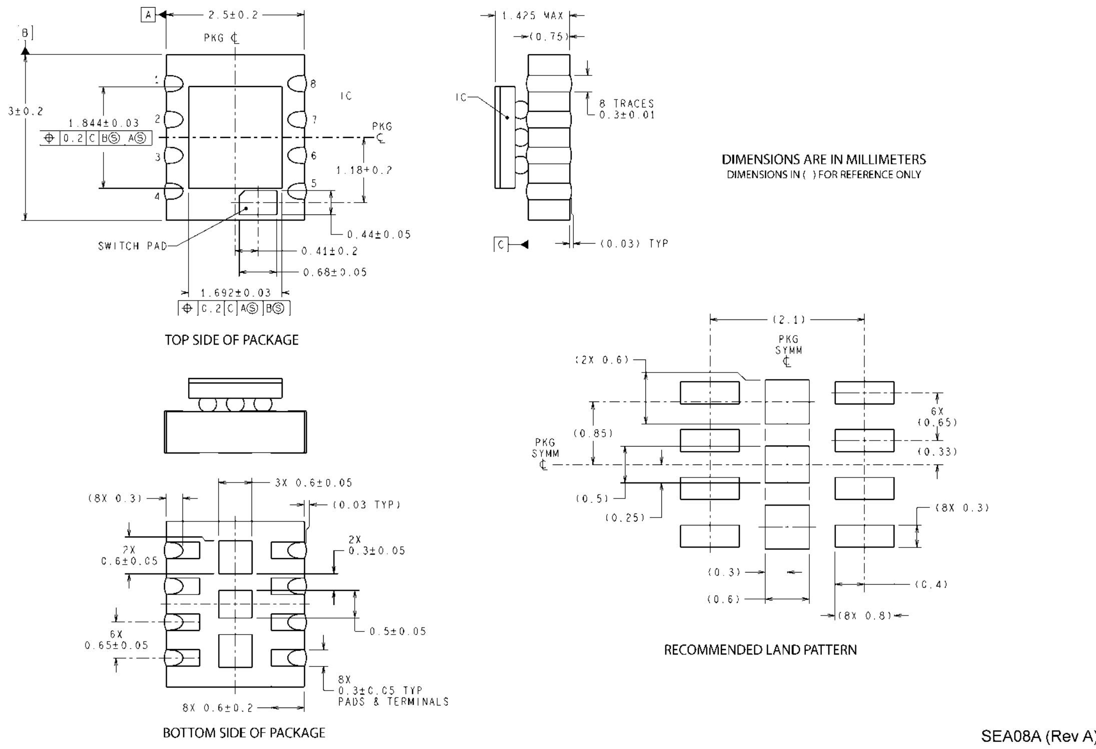
3. Run the feedback trace (from V_{OUT} to FB) away from noise sources.

4. Connect SGND to a quiet GND plane.

5. Provide enough PCB area for proper heatsinking. Refer to the Electrical Characteristics table for example θ_{JA} values for different board areas. Also, refer to AN-2020 for additional thermal design hints.

Refer to the evaluation board application note (AN-2166) for a complete board layout example.

Physical Dimensions inches (millimeters) unless otherwise noted



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Notes