MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC54/74HC132

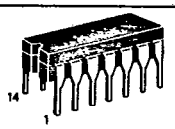
Quad 2-Input NAND Gate with Schmitt-Trigger Inputs

High-Performance Silicon-Gate CMOS

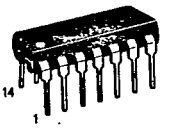
The MC54/74HC132 is identical in pinout to the LS132. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC132 can be used to enhance noise immunity or to square up slowly changing waveforms.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 72 FETs or 18 Equivalent Gates



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06

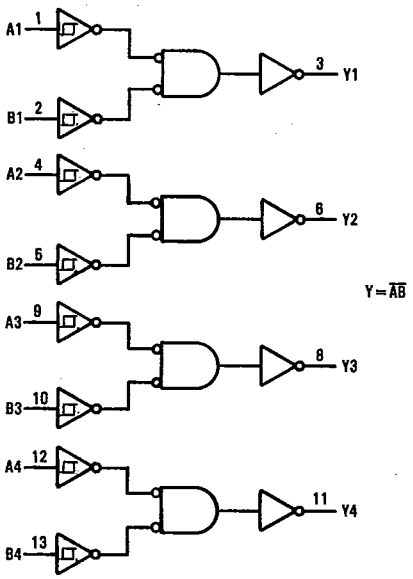
D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXD	SOIC

$T_A = -55°$ to 125°C for all packages.
Dimensions in Chapter 7.

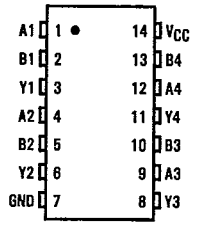
LOGIC DIAGRAM



$Y = \overline{AB}$

PIN 14 = V_{CC}
PIN 7 = GND

PIN ASSIGNMENT



FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

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MC54/74HC132

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: −10 mW/°C from 65° to 125°C
Ceramic DIP: −10 mW/°C from 100° to 125°C
SOIC Package: −7 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 4.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	−55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	no limit*	ns

*When V_{in} ~0.5 V_{CC}, I_{CC} > > quiescent current.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit 25°C	Guaranteed Limit −40°C to +85°C	Guaranteed Limit −55°C to +125°C	Unit
V_{T+}max	Maximum Positive-Going Input Threshold Voltage (Figure 3)	V_{out}=0.1 V $\|I_{out}\|$ ≤20 μA	2.0 4.5 6.0	1.50 3.15 4.20	1.50 3.15 4.20	1.50 3.15 4.20	V
V_{T+}min	Minimum Positive-Going Input Threshold Voltage (Figure 3)	V_{out}=0.1 V $\|I_{out}\|$ ≤20 μA	2.0 4.5 6.0	1.00 2.30 3.00	0.95 2.25 2.95	0.95 2.25 2.95	V
V_{T-}max	Maximum Negative-Going Input Threshold Voltage (Figure 3)	V_{out}=V_{CC}−0.1 V $\|I_{out}\|$ ≤20 μA	2.0 4.5 6.0	0.90 2.00 2.60	0.95 2.05 2.65	0.95 2.05 2.65	V
V_{T-}min	Minimum Negative-Going Input Threshold Voltage (Figure 3)	V_{out}=V_{CC}−0.1 V $\|I_{out}\|$ ≤20 μA	2.0 4.5 6.0	0.30 0.90 1.20	0.30 0.90 1.20	0.30 0.90 1.20	V
$V_H$max Note 2	Maximum Hysteresis Voltage (Figure 3)	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$ ≤20 μA	2.0 4.5 6.0	1.20 2.25 3.00	1.20 2.25 3.00	1.20 2.25 3.00	V
$V_H$min Note 2	Minimum Hysteresis Voltage (Figure 3)	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$ ≤20 μA	2.0 4.5 6.0	0.20 0.40 0.50	0.20 0.40 0.50	0.20 0.40 0.50	V

NOTES:
1. Information on typical parametric values can be found in Chapter 4.
2. $V_H$min > (V_{T+}min) − (V_{T-}max); $V_H$max = (V_{T+}max) + (V_{T-}min).

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DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to −55°C	≤85°C	≤125°C	
V_{OH}	Minimum High-Level Output Voltage	$V_{in} \le V_{T-}$ min or V_{T+} max $\|I_{out}\| \le 20\ \mu A$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} \le V_{T-}$ min or V_{T+} max $\|I_{out}\| \le 4.0$ mA $\|I_{out}\| \le 5.2$ mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} \ge V_{T+}$ max $\|I_{out}\| \le 20\ \mu A$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} \ge V_{T+}$ max $\|I_{out}\| \le 4.0$ mA $\|I_{out}\| \le 5.2$ mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0\ \mu A$	6.0	2	20	40	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to −55°C	≤85°C	≤125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 2)	2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:
1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

C_{PD}	Power Dissipation Capacitance (Per Gate) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, V_{CC} = 5.0 V 24	pF

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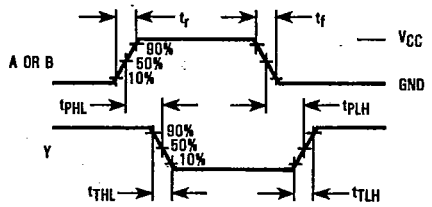
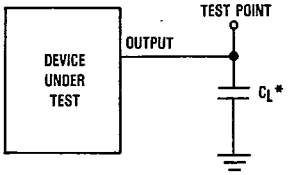


Figure 1. Switching Waveforms



*Includes all probe and jig capacitance.

Figure 2. Test Circuit

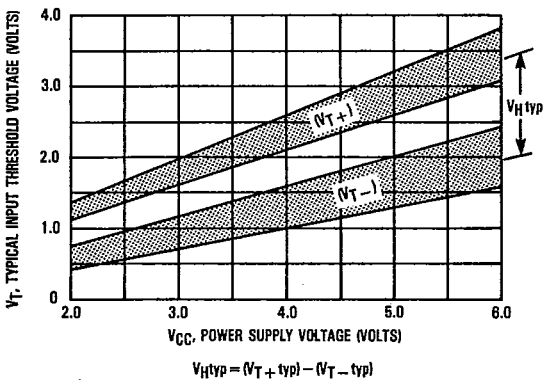


Figure 3. Typical Input Threshold, V_{T+}, V_{T-}, Versus Power Supply Voltage

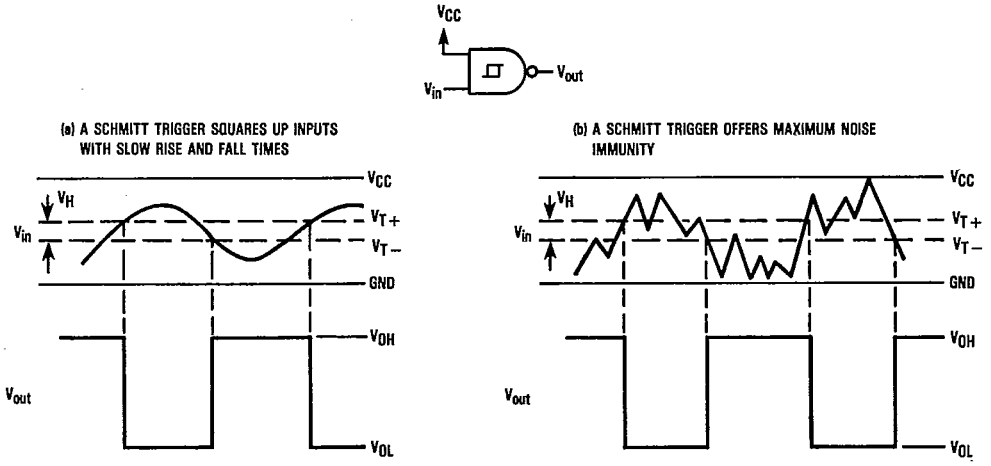


Figure 4. Typical Schmitt-Trigger Applications

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