High Voltage, Rail-to-Rail Input/Output, Precision Operational Amplifiers, e-trim™ Series

Check for Samples: OPA192, OPA2192, OPA4192

FEATURES

- **Low Offset Voltage: ±5 µV**
- **Low Offset Voltage Drift: ±0.2µV/°C**
- **Low Noise: 5.5 nV/√Hz at 1 kHz**
- **Wide Bandwidth: 10 MHz GBW (G = 100)**
- **High Slew Rate : 20 V/µs**
- **Low Quiescent Current: 1 mA per Amplifier**
- **Rail-to-Rail Input and Output**
- **Wide Supply: ±2.25 V to ±18 V, +4.5 V to +36 V**
- **EMI/RFI Filtered Inputs**
- **High Common-Mode Rejection: 140 dB**
- **Low Bias Current: ±5 pA**
- **Differential Input Voltage Range to Supply Rail**
- **High Capacitive Load Drive Capability: 1 nF**
- **Industry standard packages:**
  - **Single in SO-8, MSOP-8 and SOT23-5**
  - **Dual in SO-8 and MSOP-8**
  - **Quad in SO-14 and TSSOP-14**

APPLICATIONS

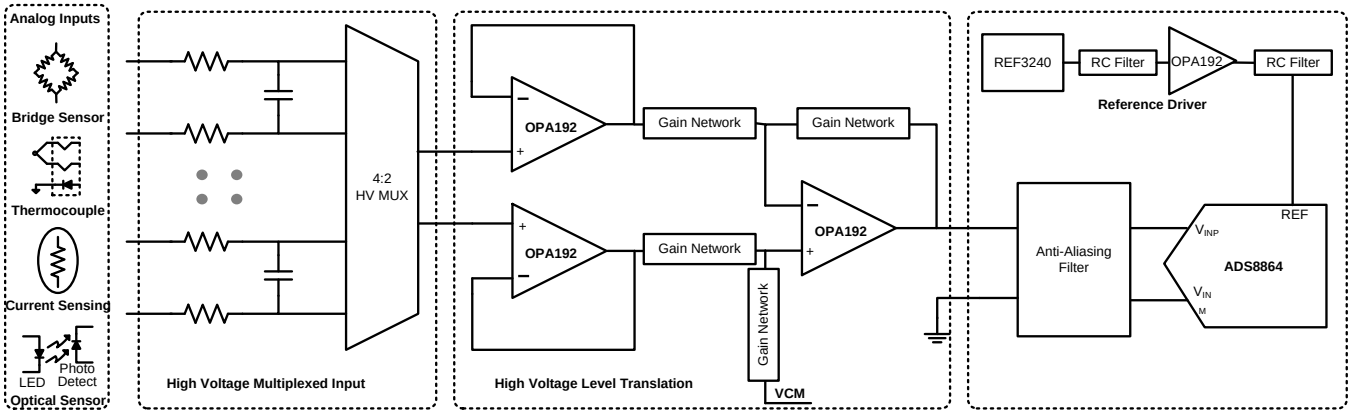
- High-Resolution ADC Driver Amplifiers
- Multiplexed Data-Acquisition Systems
- SAR ADC Reference Buffers
- Programmable Logic Controllers
- Test and Measurement Equipment
- High-Side and Low-Side Current Sensing
- High Precision Comparator

DESCRIPTION

The OPA192 family (1) (OPA192, OPA2192, and OPA4192) is a new generation of 36-V, e-trim operational amplifiers. These devices offer outstanding dc precision and ac performance, including rail-to-rail input/output, low offset (±5 µV, typ), low offset drift (±0.2 µV/°C, typ), and 10MHz bandwidth. Unique features such as differential input-voltage range to the supply rail, high output current and high capacitive load drive of up to 1 nF, and high slew rate make the OPA192 a robust, high-performance operational amplifier for high-voltage industrial applications. The OPA192 family of op amps is available in standard packages and is specified from –40°C to +125°C.

(1) OPA192 SO-8 package is production data. All other devices are product preview.

OPA192 IN A HIGH-VOLTAGE, MULTIPLEXED, DATA-ACQUISITION SYSTEM



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE AND ORDERING INFORMATION(1)

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

			VALUE	UNIT
Supply voltage			±20 (+40, single supply)	V
Signal input terminals	Voltage	Common-mode	(V–) – 0.5 to (V+) + 0.5	V
		Differential	(V+) - (V-) + 0.2	V
	Current		±10	mA
Output short circuit(2)			Continuous	
Operating temperature			–55 to +150	°C
Storage temperature			–65 to +150	°C
Junction temperature			+150	°C
Electrostatic discharge (ESD) ratings	Human body model (HBM)		4	kV
	Charged device model (CDM)		1	kV

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) Short-circuit to ground, one amplifier per package.

ELECTRICAL CHARACTERISTICS: V_S= ±4 V to ±18 V (V_S= +8 V to +36 V)

At T_A = +25°C, V_{CM} = V_{OUT} = V_S / 2, and R_{LOAD} = 10 kΩ connected to V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		OPA192 MIN	OPA192 TYP	OPA192 MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				±5	±25	µV
		T_A = –40°C to +125°C				±75	µV
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +125°C	(V–) – 0.1 V < V_{CM} < (V+) – 3 V		±0.2	±0.5	µV/°C
PSRR	Power-supply rejection ratio	T_A = –40°C to +125°C			±0.3	±1.0	µV/V
INPUT BIAS CURRENT							
I_B	Input bias current				±5	±20	pA
		T_A = –40°C to +125°C				±5	nA
I_{OS}	Input offset current				±2	±20	pA
		T_A = –40°C to +125°C				±2	nA
NOISE							
E_n	Input voltage noise	(V–) – 0.1 V < V_{CM} < (V+) – 3V	f = 0.1 Hz to 10 Hz		1.30		μV_{PP}
		(V+) – 1.5 V < V_{CM} < (V+) + 0.1 V	f = 0.1 Hz to 10 Hz		4		μV_{PP}
e_n	Input voltage noise density	(V–) – 0.1 V < V_{CM} < (V+) – 3 V	f = 100 Hz		10.5		nV/√Hz
			f = 1 kHz		5.5		nV/√Hz
		(V+) – 1.5 V < V_{CM} < (V+) + 0.1 V	f = 100 Hz		32		nV/√Hz
			f = 1 kHz		12.5		nV/√Hz
i_n	Input current noise density		f = 1kHz		1.5		fA/√Hz

ELECTRICAL CHARACTERISTICS: V_S= ±4 V to ±18 V (V_S= +8 V to +36 V) (continued)

At T_A = +25°C, V_{CM} = V_{OUT} = V_S / 2, and R_{LOAD} = 10 kΩ connected to V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		OPA192 MIN	OPA192 TYP	OPA192 MAX	UNIT
INPUT VOLTAGE							
V_{CM}	Common-mode voltage range			(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio		(V–) – 0.1 V < V_{CM} < (V+) – 3 V	120	140		dB
			(V+) – 3 V < V_{CM} < (V+) - 1.5 V	See Typical Characteristics			
			(V+) – 1.5 V < V_{CM} < (V+) + 0.1 V	100	120		dB
		T_A = –40°C to +125°C	(V–) – 0.1 V < V_{CM} < (V+) – 3 V	114	126		dB
			(V+) – 1.5 V < V_{CM} < (V+) + 0.1 V	86	100		dB
INPUT IMPEDANCE							
Z_{ID}	Differential				100 || 1.6		MΩ || pF
Z_{IC}	Common-mode				1 || 6.4		10^{13}Ω || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V–) + 0.6 V < V_O < (V+) – 0.6 V	R_{LOAD} = 2 kΩ	120	134		dB
		(V–) + 0.6 V < V_O < (V+) – 0.6 V T_A = –40°C to +125°C	R_{LOAD} = 2 kΩ	114	126		dB
		(V–) + 0.3 V < V_O < (V+) – 0.3 V	R_{LOAD} = 10 kΩ	126	140		dB
		(V–) + 0.3 V < V_O < (V+) – 0.3 V T_A = –40°C to +125°C	R_{LOAD} = 10 kΩ	120	134		dB
FREQUENCY RESPONSE							
GBW	Unity gain bandwidth				10		MHz
SR	Slew rate	G = 1, 10-V step			20		V/µs
t_s	Settling time	To 0.01%	V_S = ±18 V, G = 1, 10-V step		1.4		µs
			V_S = ±18 V, G = 1, 5-V step		0.9		µs
		To 0.001%	V_S = ±18 V, G = 1, 10-V step		2.1		µs
			V_S = ±18 V, G = 1, 5-V step		1.8		µs
t_{OR}	Overload recovery time	V_{IN} × G = V_S			200		ns
THD+N	Total harmonic distortion + noise	G = 1, f = 1 kHz, V_O = 3.5 V_{RMS}			0.00008		%
OUTPUT							
V_O	Voltage output swing from rail	Positive rail	No load		5	10	mV
			R_{LOAD} = 10 kΩ		95	110	mV
			R_{LOAD} = 2 kΩ		430	500	mV
		Negative rail	No load		5	10	mV
			R_{LOAD} = 10 kΩ		95	110	mV
			R_{LOAD} = 2 kΩ		430	500	mV
I_{SC}	Short-circuit current				±65		mA
C_{LOAD}	Capacitive load drive			See Typical Characteristics			pF
Z_O	Open-loop output impedance	f = 1 MHz, I_O = 0 A, See Figure 23			375		Ω

ELECTRICAL CHARACTERISTICS: V_S= ±2.25 V to ±4 V (V_S= +4.5 V to +8 V)

At T_A = +25°C, V_{CM} = V_{OUT} = V_S / 2, and R_{LOAD} = 10 kΩ connected to V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		OPA192 MIN	OPA192 TYP	OPA192 MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_{CM} = (V+) – 3 V			±5	±25	µV
		V_{CM} = V_S / 2		See *Common-Mode Voltage Range* section			µV
		V_{CM} = (V+) – 1.5 V			±10	±25	µV
		T_A = –40°C to +125°C, V_{CM} = (V+) – 3 V				±75	µV
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +125°C	(V–) – 0.1 V < V_{CM} < (V+) – 1.5 V		±0.2	±0.5	µV/°C
			(V+) – 1.5 V < V_{CM} < (V+) + 0.1 V		±0.5	±3	µV/°C
PSRR	Power-supply rejection ratio	V_{CM} = (V-)			±0.5		µV/V
		T_A = –40°C to +125°C			±1		µV/V
INPUT BIAS CURRENT							
I_B	Input bias current				±5	±20	pA
		T_A = –40°C to +125°C				±5	nA
I_{OS}	Input offset current				±2	±20	pA
		T_A = –40°C to +125°C				±2	nA
NOISE							
E_n	Input voltage noise	(V–) – 0.1 V < V_{CM} < (V+) – 3 V, f = 0.1 Hz to 10 Hz			1.30		$µV_{PP}$
		(V+) – 1.5 V < V_{CM} < (V+) + 0.1 V, f = 0.1 Hz to 10 Hz			4		$µV_{PP}$
e_n	Input voltage noise density	(V–) – 0.1 V < V_{CM} < (V+) – 3 V	f = 100 Hz		10.5		nV/√Hz
			f = 1 kHz		5.5		nV/√Hz
		(V+) – 1.5 V < V_{CM} < (V+) + 0.1 V	f = 100 Hz		32		nV/√Hz
			f = 1 kHz		12.5		nV/√Hz
i_n	Input current noise density		f = 1kHz		1.5		fA/√Hz
INPUT VOLTAGE							
V_{CM}	Common-mode voltage range			(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio		(V–) – 0.1 V < V_{CM} < (V+) – 3 V	94	110		dB
			(V+) – 3 V < V_{CM} < (V+) – 1.5 V	See Typical Characteristics			dB
			(V+) – 1.5V < V_{CM} < (V+) + 0.1 V	100	120		dB
		T_A = –40°C to +125°C	(V–) – 0.1 V < V_{CM} < (V+) – 3 V	90	104		dB
INPUT IMPEDANCE							
Z_{ID}	Differential				100 || 1.6		MΩ || pF
Z_{IC}	Common-mode				1 || 6.4		10^{13}Ω || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V–) + 0.6 V < V_O < (V+) – 0.6 V	R_{LOAD} = 2 kΩ	110	120		dB
		(V–) + 0.6 V < V_O < (V+) – 0.6 V T_A = –40 °C to +125 °C	R_{LOAD} = 2 kΩ	100	114		dB
		(V–) + 0.3 V < V_O < (V+) – 0.3 V	R_{LOAD} = 10 kΩ	110	126		dB
		(V–) + 0.3 V < V_O < (V+) – 0.3 V T_A = –40°C to +125°C	R_{LOAD} = 10 kΩ	110	120		dB
FREQUENCY RESPONSE							
GBW	Unity gain bandwidth				10		MHz
SR	Slew rate	G = 1, 10-V step			20		V/µs
t_s	Settling time	To 0.01%	V_S = ±3 V, G = 1, 5-V step		1		µs
t_{OR}	Overload recovery time	V_{IN}× G = V_S			200		ns

ELECTRICAL CHARACTERISTICS

At T_A = +25°C, V_{CM} = V_{OUT} = V_S / 2, and R_{LOAD} = 10 kΩ connected to V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_S	Specified voltage range		+4.5		+36	V
I_Q	Quiescent current per amplifier	I_O = 0 A		1	1.2	mA
		T_A = –40°C to +125°C, I_O = 0 A			1.5	mA
TEMPERATURE						
	Specified range		–40		+125	°C
	Operating range		–55		+150	°C
	Thermal protection			+140		°C

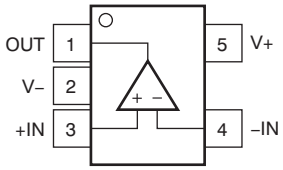
THERMAL INFORMATION: OPA192

THERMAL METRIC(1)		OPA192			UNITS
		D (SO)	DBV (SOT23)	DGK (MSOP)	
		8 PINS	5 PINS	8 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	115.8	TBD	TBD	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	60.1	TBD	TBD	
θ_{JB}	Junction-to-board thermal resistance	56.4	TBD	TBD	
ψ_{JT}	Junction-to-top characterization parameter	12.8	TBD	TBD	
ψ_{JB}	Junction-to-board characterization parameter	55.9	TBD	TBD	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	N/A	TBD	TBD	

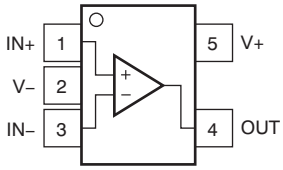
(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

PIN CONFIGURATIONS

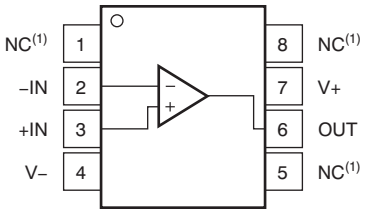
DBV PACKAGE: OPA192
SOT23-5
(TOP VIEW)



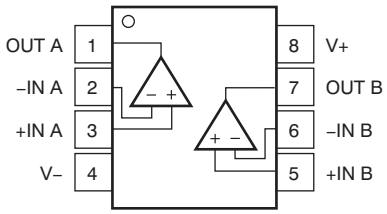
DCK PACKAGE: OPA192
SC-70
(TOP VIEW)



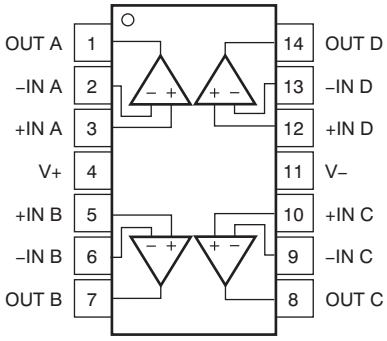
D AND DGK PACKAGES: OPA192
SO-8 AND MSOP-8
(TOP VIEW)



D AND DGK PACKAGES: OPA2192
SO-8 AND MSOP-8
(TOP VIEW)



D AND PW PACKAGES: OPA4192
SO-14 AND TSSOP-14
(TOP VIEW)



(1) NC = No internal connection.

NOTE: OPA192 SO-8 package is production data. All other packages are product preview.

TYPICAL CHARACTERISTICS: Table of Graphs

Table 1. Characteristic Performance Measurements

DESCRIPTION	FIGURE
Offset Voltage Production Distribution	Figure 1
Offset Voltage Drift Distribution	Figure 2
Offset Voltage vs Temperature	Figure 3
Offset Voltage vs Common-Mode Voltage	Figure 4, Figure 5, Figure 6
Offset Voltage vs Power Supply	Figure 7
Open-Loop Gain and Phase vs Frequency	Figure 8
Closed-Loop Gain and Phase vs Frequency	Figure 9
Input Bias Current vs Common-Mode Voltage	Figure 10
Input Bias Current vs Temperature	Figure 11
Output Voltage Swing vs Output Current (maximum supply)	Figure 12
CMRR and PSRR vs Frequency	Figure 13
CMRR vs Temperature	Figure 14
PSRR vs Temperature	Figure 15
0.1-Hz to 10-Hz Noise	Figure 16
Input Voltage Noise Spectral Density vs Frequency	Figure 17
THD+N Ratio vs Frequency	Figure 18
THD+N vs Output Amplitude	Figure 19
Quiescent Current vs Supply Voltage	Figure 20
Quiescent Current vs Temperature	Figure 21
Open Loop Gain vs Temperature	Figure 22
Open Loop Output Impedance vs Frequency	Figure 23
Small Signal Overshoot vs Capacitive Load (100-mV output step)	Figure 24, Figure 25
No Phase Reversal	Figure 26
Positive Overload Recovery	Figure 27
Negative Overload Recovery	Figure 28
Small-Signal Step Response (100 mV)	Figure 29, Figure 30
Large-Signal Step Response	Figure 31
Settling Time	Figure 32, Figure 33, Figure 34, Figure 35
Short-Circuit Current vs Temperature	Figure 36
Maximum Output Voltage vs Frequency	Figure 37
Propagation Delay Rising Edge	Figure 38
Propagation Delay Falling Edge	Figure 39

TYPICAL CHARACTERISTICS

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

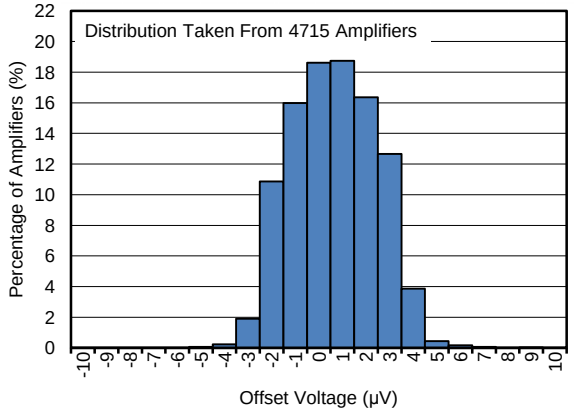


Figure 1. OFFSET VOLTAGE PRODUCTION DISTRIBUTION

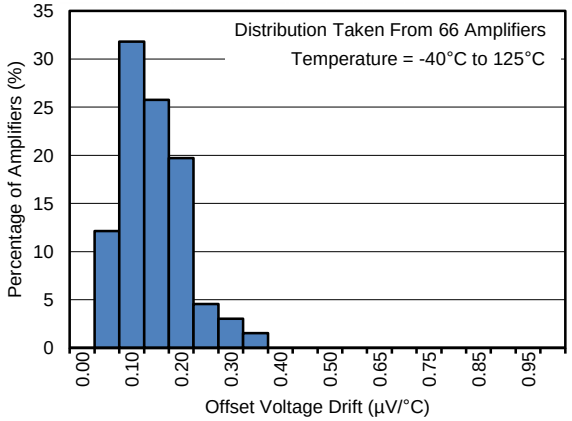


Figure 2. OFFSET VOLTAGE DRIFT DISTRIBUTION

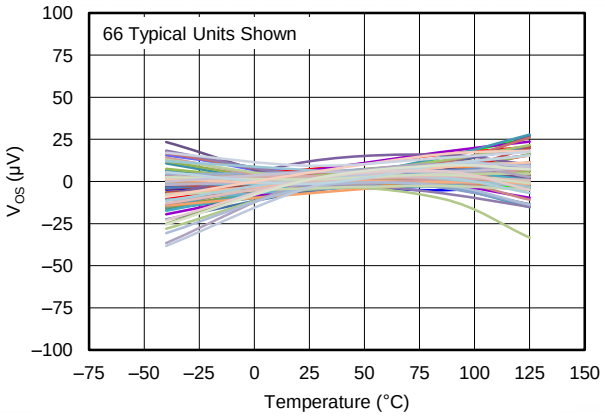


Figure 3. OFFSET VOLTAGE vs TEMPERATURE

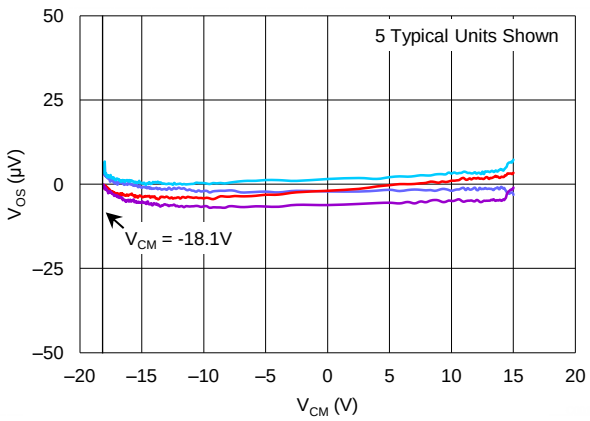


Figure 4. OFFSET VOLTAGE vs COMMON-MODE VOLTAGE

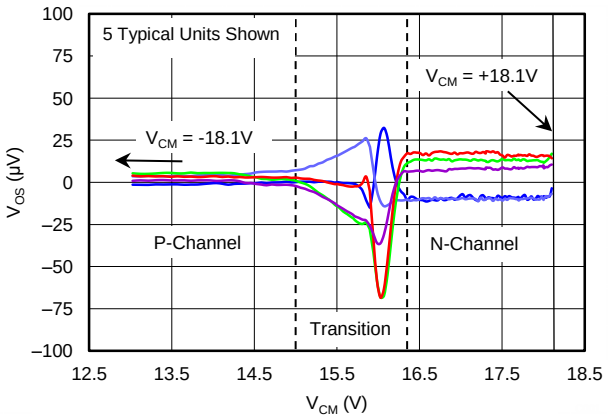


Figure 5. OFFSET VOLTAGE vs COMMON-MODE VOLTAGE

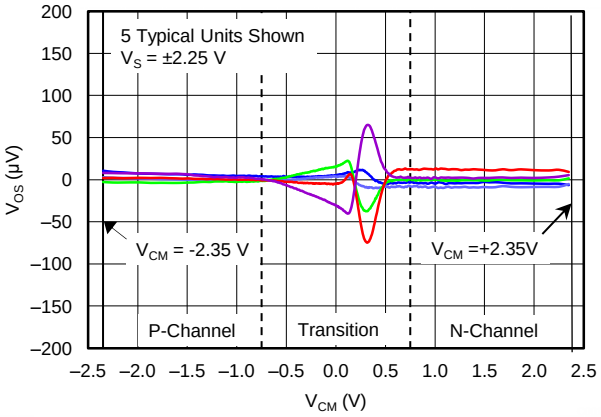


Figure 6. OFFSET VOLTAGE vs COMMON-MODE VOLTAGE

TYPICAL CHARACTERISTICS (continued)

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

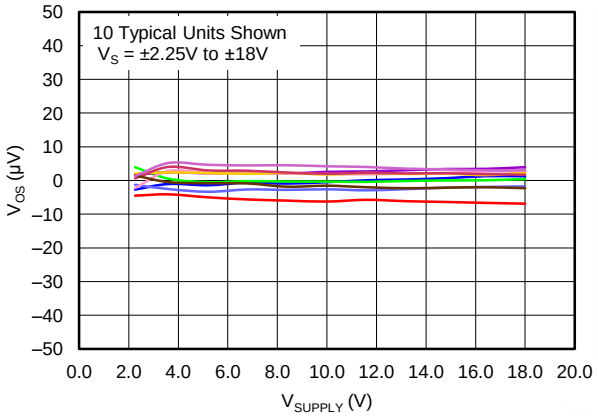


Figure 7. OFFSET VOLTAGE vs POWER SUPPLY

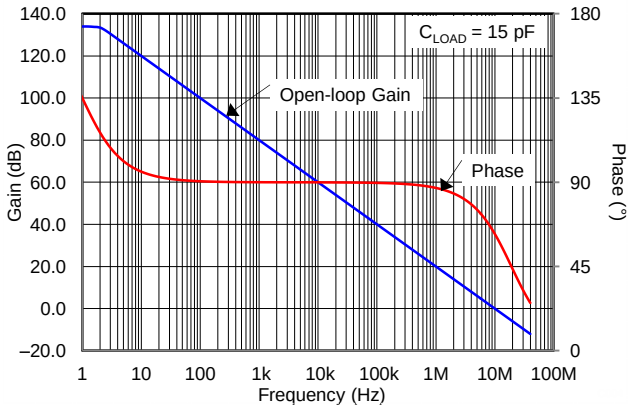


Figure 8. OPEN-LOOP GAIN AND PHASE vs FREQUENCY

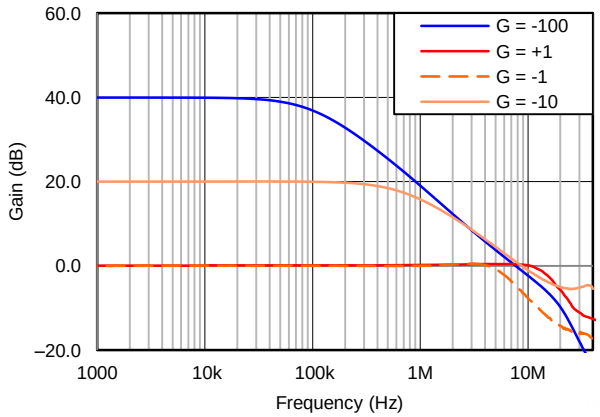


Figure 9. CLOSED-LOOP GAIN AND PHASE vs FREQUENCY

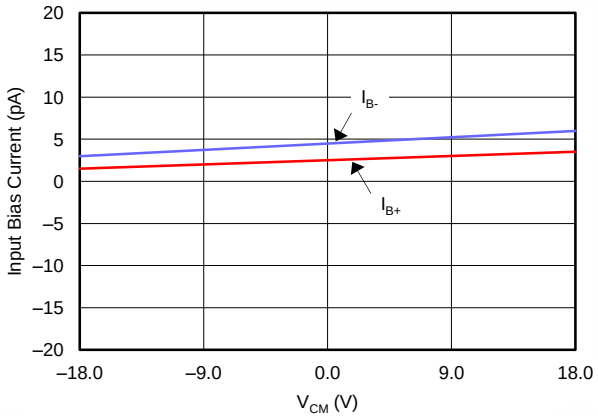


Figure 10. INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE

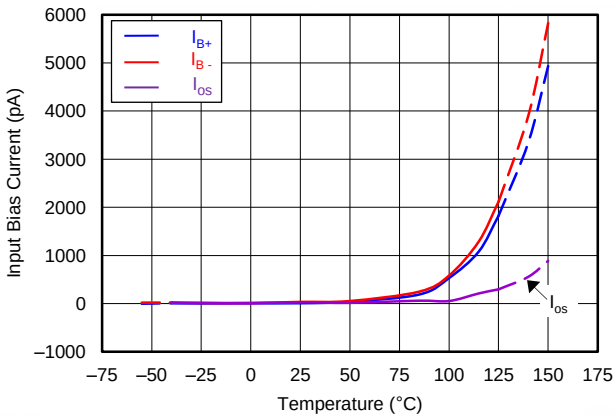


Figure 11. INPUT BIAS CURRENT vs TEMPERATURE

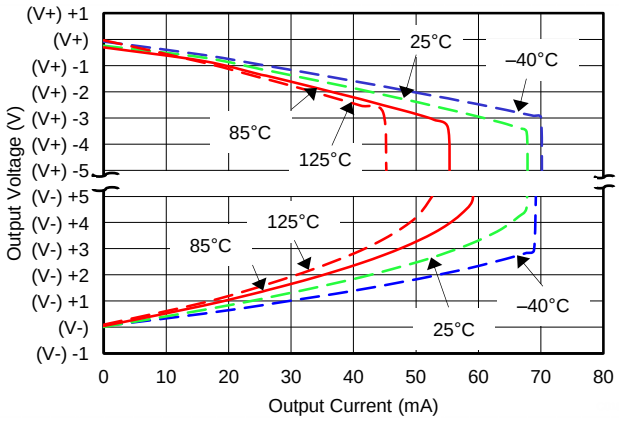


Figure 12. OUTPUT VOLTAGE SWING vs OUTPUT CURRENT (Maximum Supply)

TYPICAL CHARACTERISTICS (continued)

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

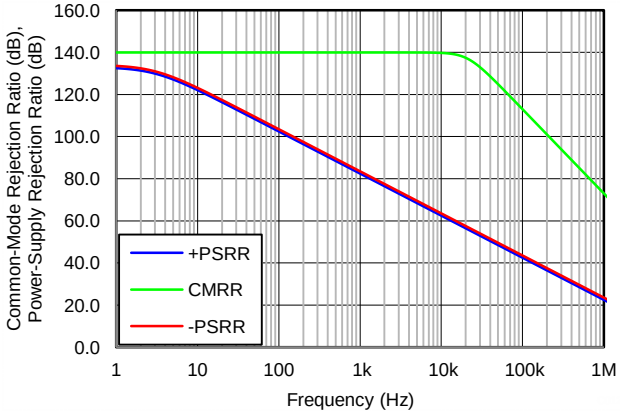


Figure 13. CMRR AND PSRR vs FREQUENCY

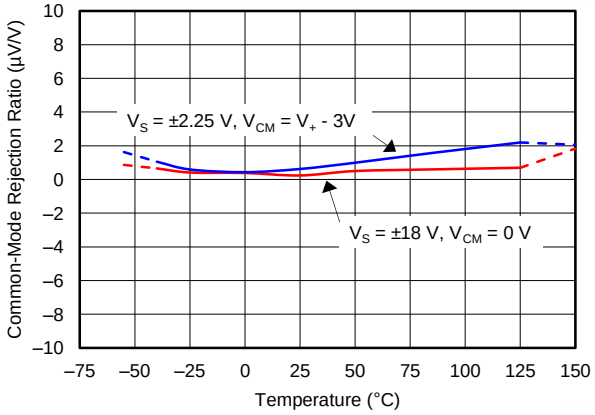


Figure 14. CMRR vs TEMPERATURE

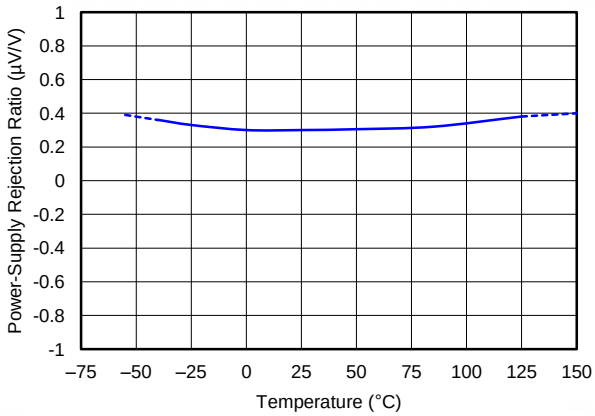


Figure 15. PSRR vs TEMPERATURE

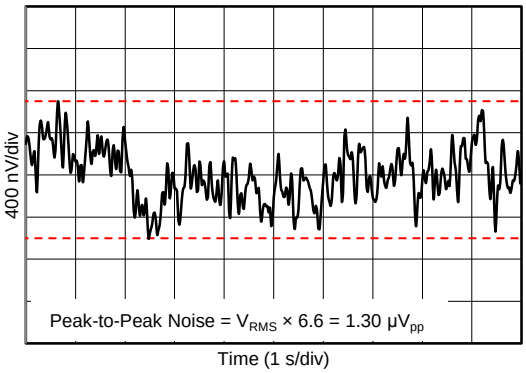


Figure 16. 0.1-Hz to 10-Hz NOISE

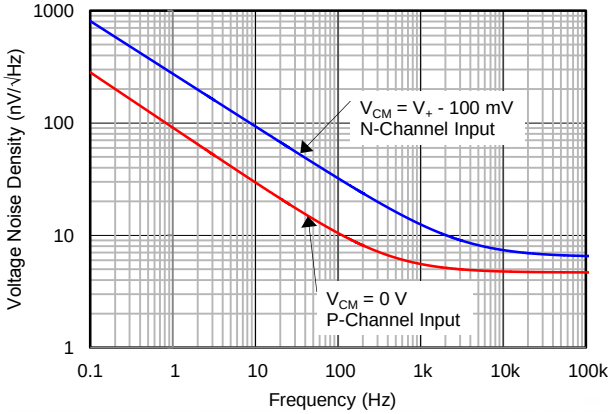


Figure 17. INPUT VOLTAGE NOISE SPECTRAL DENSITY vs FREQUENCY

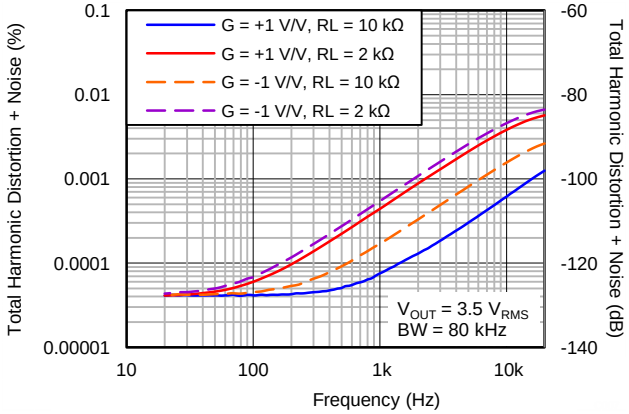


Figure 18. THD+N RATIO vs FREQUENCY

TYPICAL CHARACTERISTICS (continued)

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

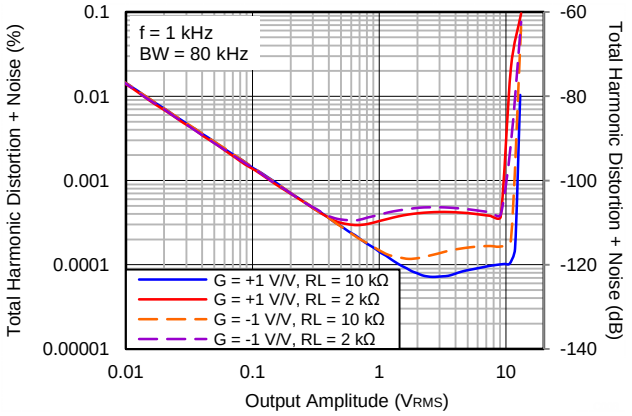


Figure 19. THD+N vs OUTPUT AMPLITUDE

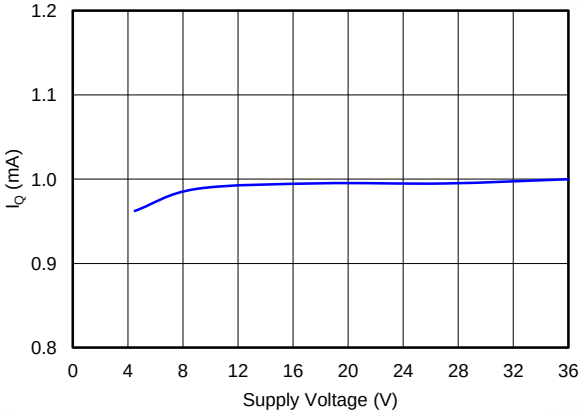


Figure 20. QUIESCENT CURRENT vs SUPPLY VOLTAGE

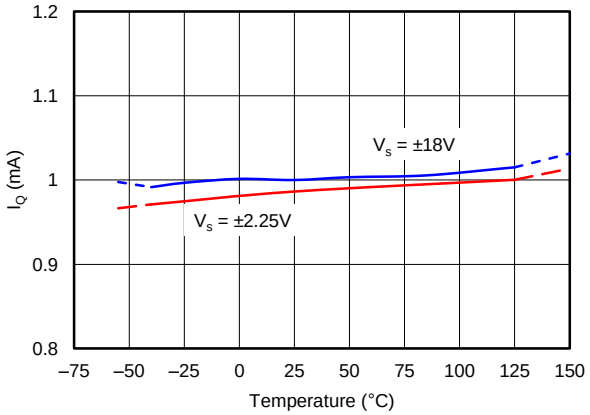


Figure 21. QUIESCENT CURRENT vs TEMPERATURE

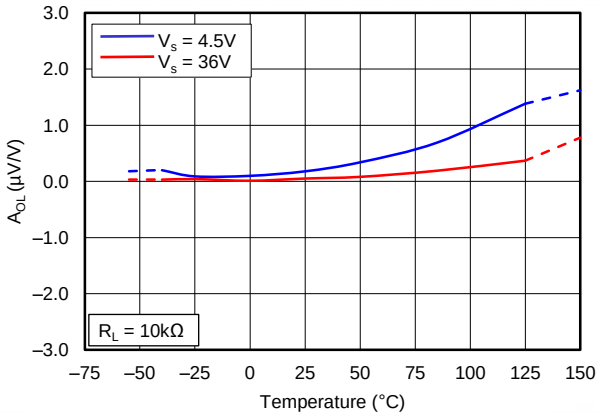


Figure 22. OPEN-LOOP GAIN vs TEMPERATURE

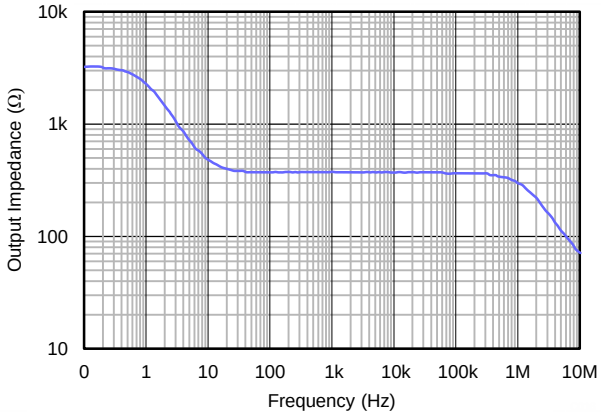


Figure 23. OPEN-LOOP OUTPUT IMPEDANCE vs FREQUENCY

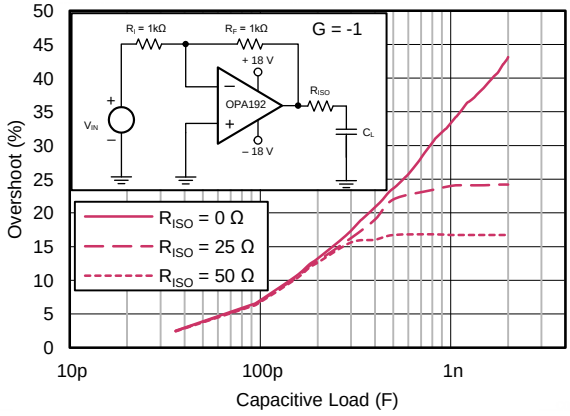


Figure 24. SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD (100-mV Output Step)

TYPICAL CHARACTERISTICS (continued)

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

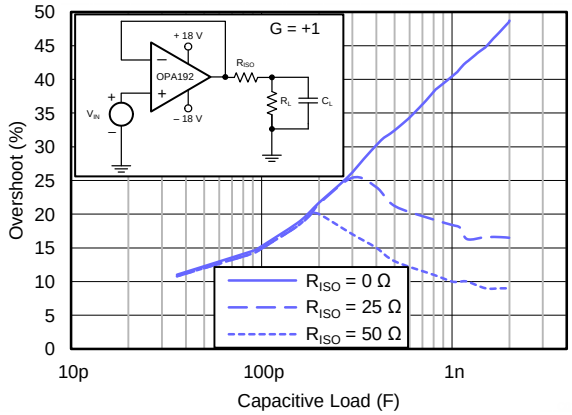


Figure 25. SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD (100-mV Output Step)

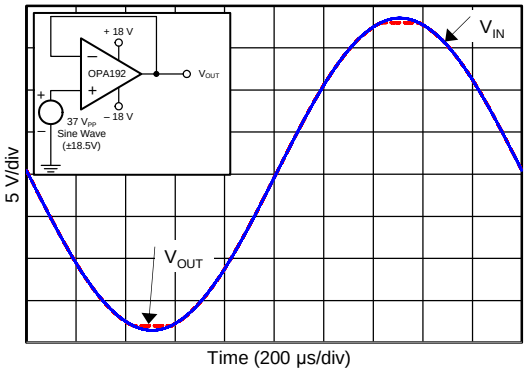


Figure 26. NO PHASE REVERSAL

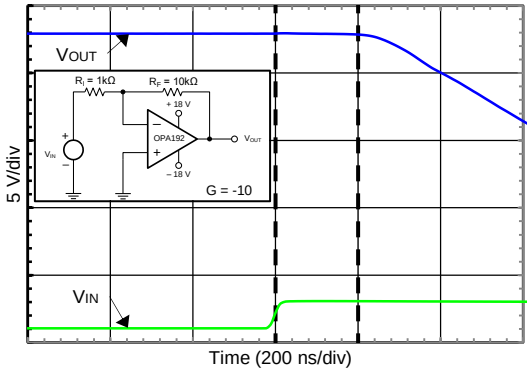


Figure 27. POSITIVE OVERLOAD RECOVERY

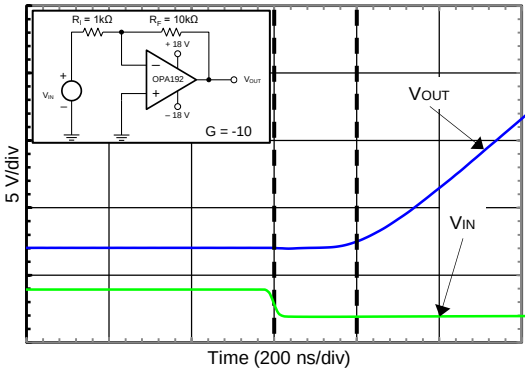


Figure 28. NEGATIVE OVERLOAD RECOVERY

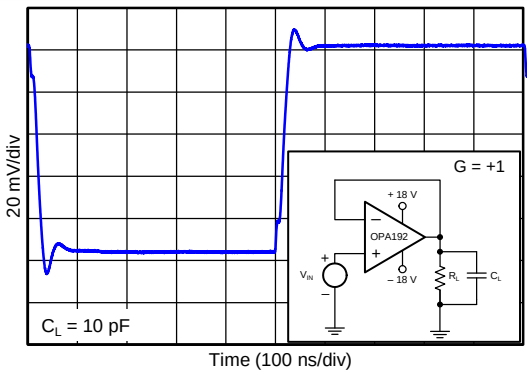


Figure 29. SMALL-SIGNAL STEP RESPONSE (100 mV)

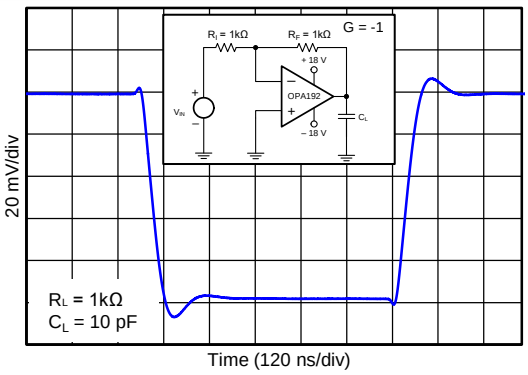


Figure 30. SMALL-SIGNAL STEP RESPONSE (100 mV)

TYPICAL CHARACTERISTICS (continued)

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

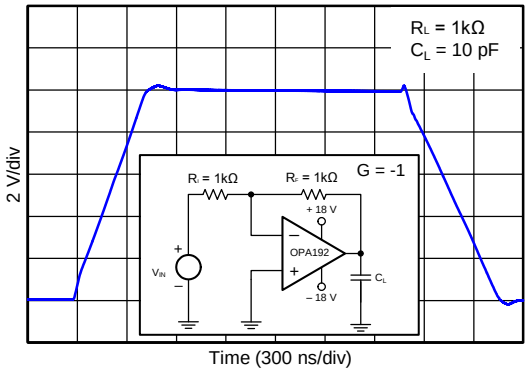


Figure 31. LARGE-SIGNAL STEP RESPONSE

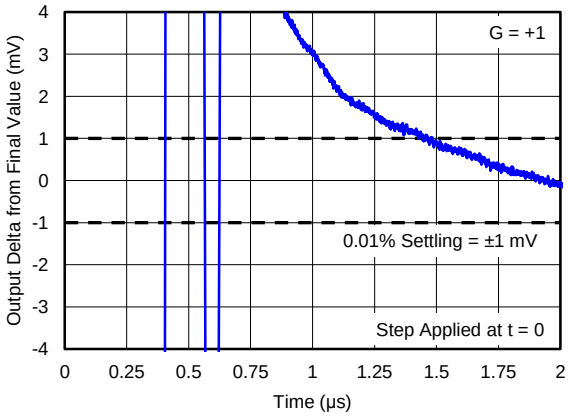


Figure 32. SETTLING TIME (10-V Positive Step)

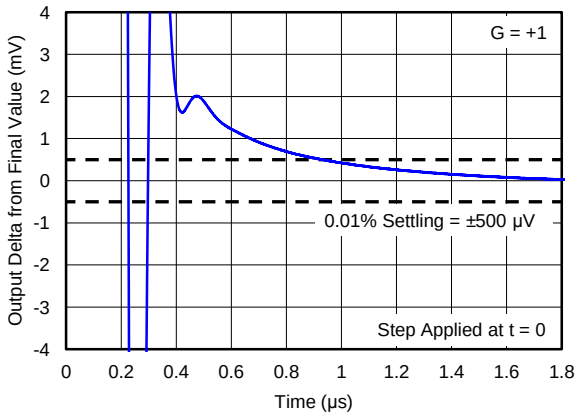


Figure 33. SETTLING TIME (5-V Positive Step)

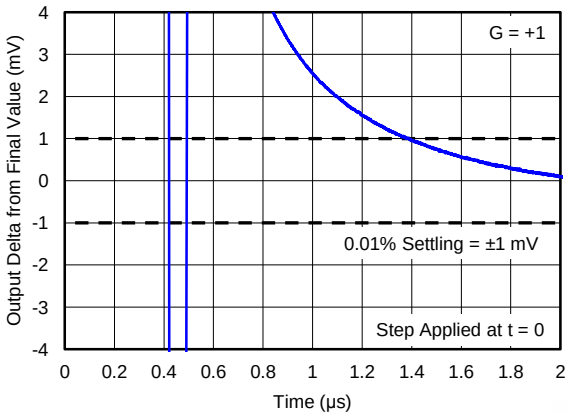


Figure 34. SETTLING TIME (10-V Negative Step)

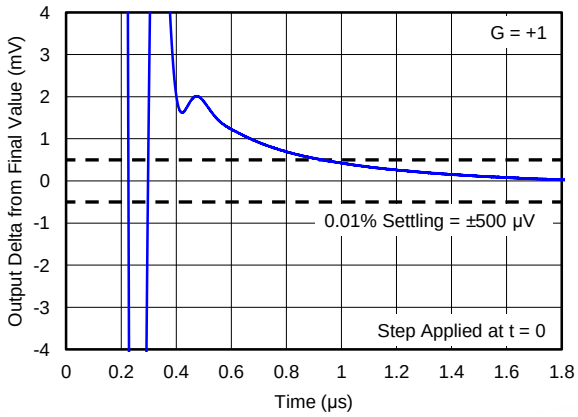


Figure 35. SETTLING TIME (5-V Negative Step)

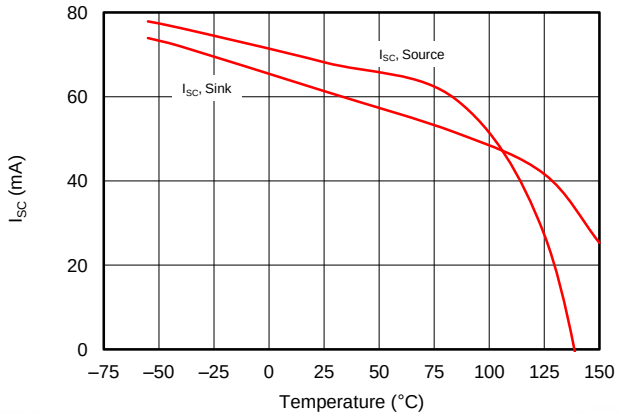


Figure 36. SHORT-CIRCUIT CURRENT vs TEMPERATURE

TYPICAL CHARACTERISTICS (continued)

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

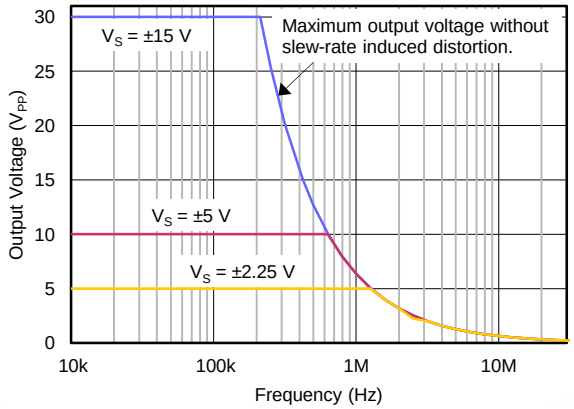


Figure 37. MAXIMUM OUTPUT VOLTAGE vs FREQUENCY

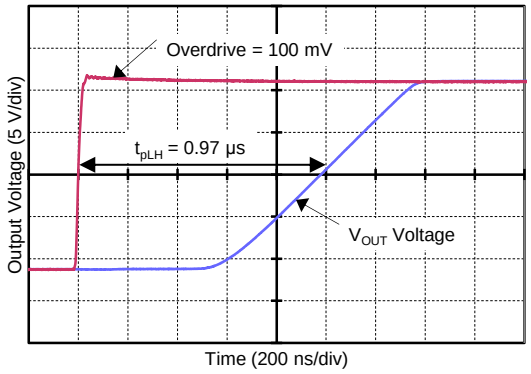


Figure 38. PROPAGATION DELAY RISING EDGE

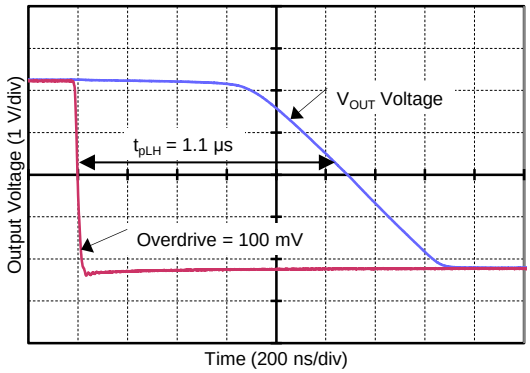


Figure 39. PROPAGATION DELAY FALLING EDGE

DETAILED DESCRIPTION

OVERVIEW

The OPA192 family of operational amplifiers use *e-trim*, a method of package-level trim for offset and offset temperature drift implemented during the final steps of manufacturing after the plastic molding process. This method minimizes the influence of inherent input transistor mismatch, as well as errors induced during package molding. The trim communication occurs on the output pin of the standard pinout, and after the trim points are set, further communication to the trim structure is permanently disabled. Figure 40 shows the simplified diagram of OPA192 with e-trim.

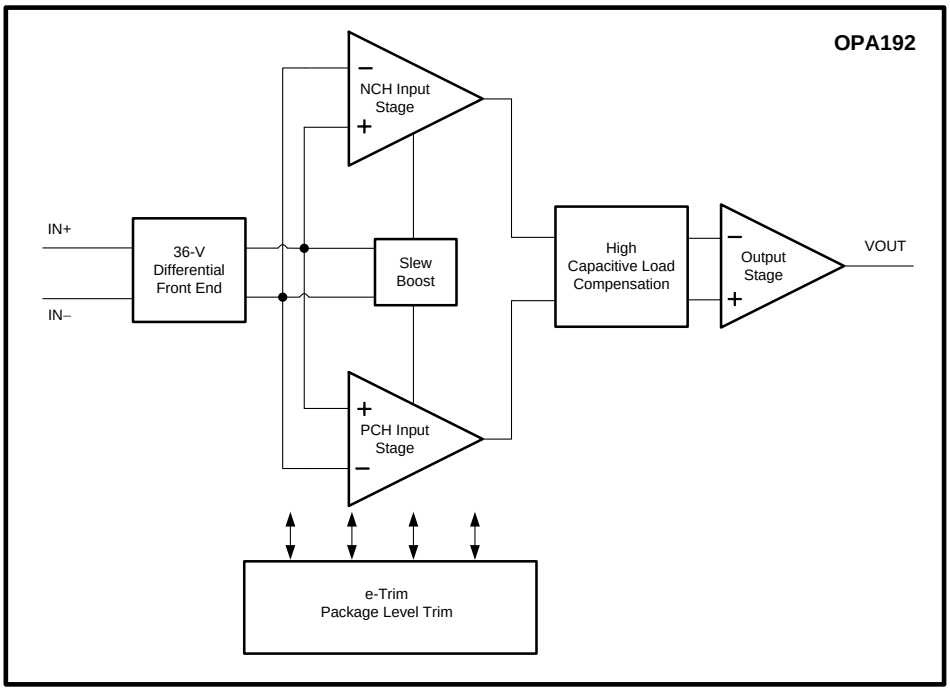


Figure 40. Simplified Schematic

Unlike previous e-trim op amps, the OPA192 uses a patented two-temperature trim architecture to achieve a very low offset voltage of 25 µV (max) and low voltage offset drift of 0.5 µV/°C (max) over the full specified temperature range. This level of precision performance at wide supply voltages makes these amplifiers useful for high-impedance industrial sensors, filters, and high-voltage data acquisition.

As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1-µF capacitors are adequate.

OPERATING VOLTAGE

The OPA192 is specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V). Many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the Typical Characteristics.

CAUTION

Supply voltages larger than 40 V can permanently damage the device; see the Absolute Maximum Ratings.

In addition, key parameters are assured over the specified temperature of T_A = –40°C to +125°C. Parameters that vary significantly with operating voltage or temperature are shown in the Typical Characteristics.

EMI REJECTION

The OPA192 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the OPA192 benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. Figure 41 shows the results of this testing on the OPA192. Table 2 shows the EMIRR IN+ values for the OPA192 at particular frequencies commonly encountered in real-world applications. Applications listed in Table 2 may be centered on or operated near the particular frequency shown. Detailed information can also be found in the Application Report SBOA128, *EMI Rejection Ratio of Operational Amplifiers*, available for download from www.ti.com.

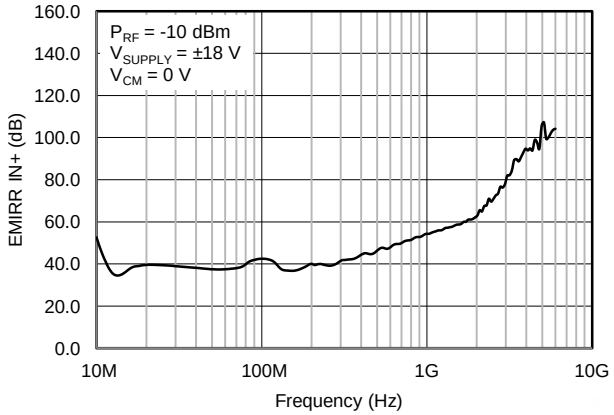


Figure 41. EMIRR Testing

Table 2. OPA192 EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	44.1 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	52.8 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	61.0 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	69.5 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	88.7 dB
5.0 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	105.5 dB

ELECTRICAL OVERSTRESS

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress (EOS). These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. See Figure 42 for an illustration of the ESD circuits contained in the OPAx192 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device or the power-supply ESD cell, internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

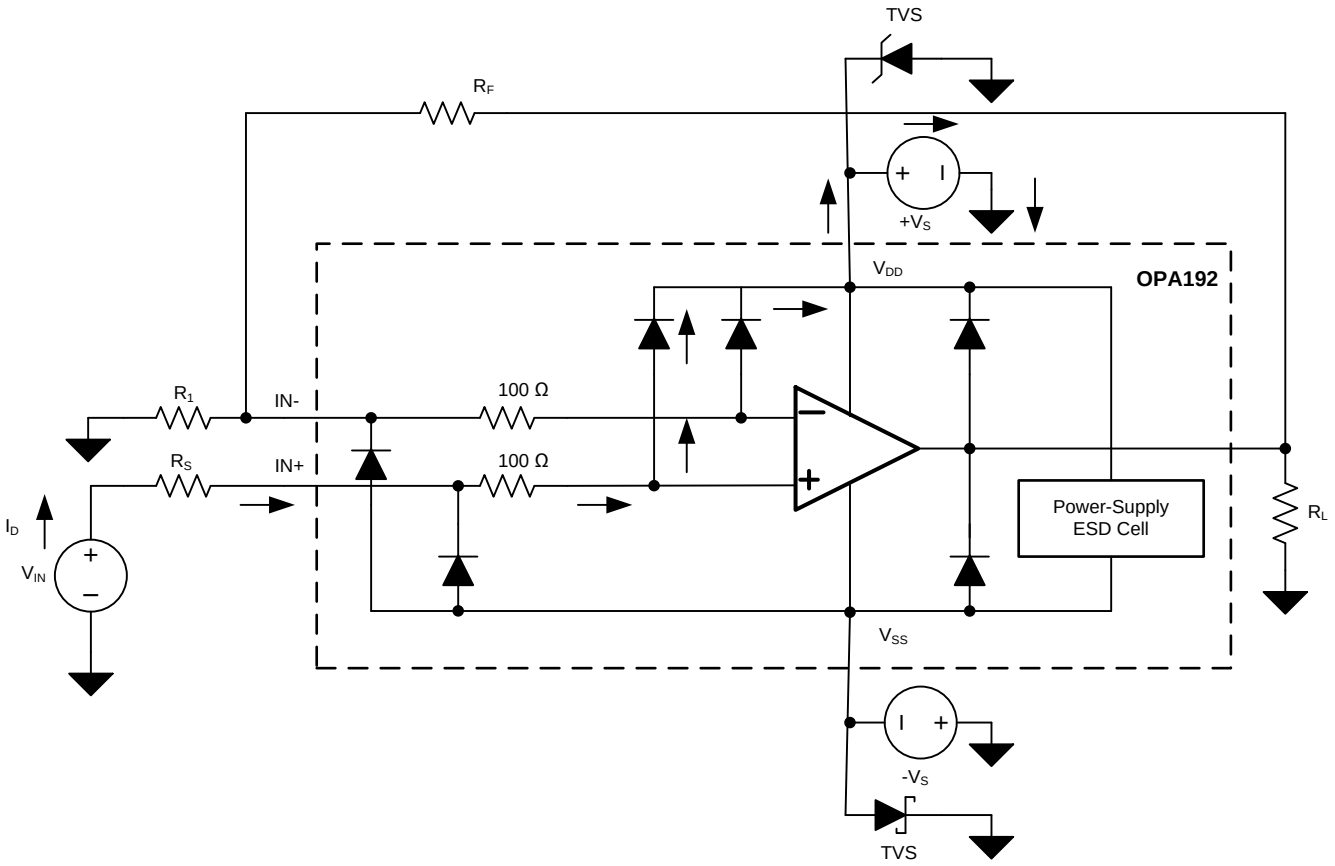


Figure 42. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event is very short in duration and very high voltage (for example, 1 kV, 100 ns), whereas an EOS event is long duration and lower voltage (for example, 50 V, 100 ms). The ESD diodes are designed for out-of-circuit ESD protection (that is, during assembly, test, and storage of the device before it is soldered to the PCB). During an ESD event, the ESD signal is passed through the ESD steering diodes to an absorption circuit (labeled ESD power-supply circuit). The ESD absorption circuit clamps the supplies to a safe level.

While this behavior is necessary for out-of-circuit protection, it causes excessive current and damage if activated in-circuit. A transient voltage suppressors (TVS) can be used to prevent against damage caused by turning on the ESD absorption circuit during an in-circuit ESD event. Using the appropriate current limiting resistors and TVS diodes allows for the use of device ESD diodes to protect against EOS events.

COMMON-MODE VOLTAGE RANGE

The OPA192 is a 36-V, true rail-to-rail input operational amplifier with an input common-mode range that extends 100 mV beyond either supply rail. This is achieved with paralleled complementary N-channel and P-channel differential input pairs, as shown in Figure 43. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 3 V to 100 mV above the positive supply. The P-channel pair is active for inputs from 100 mV below the negative supply to approximately (V+) – 1.5 V. There is a small transition region, typically (V+) –3 V to (V+) – 1.5 V) in which both input pairs are on. This transition region can vary modestly with process variation, and within this region PSRR, CMRR, offset voltage, offset drift, noise and THD performance may be degraded compared to operation outside this region.

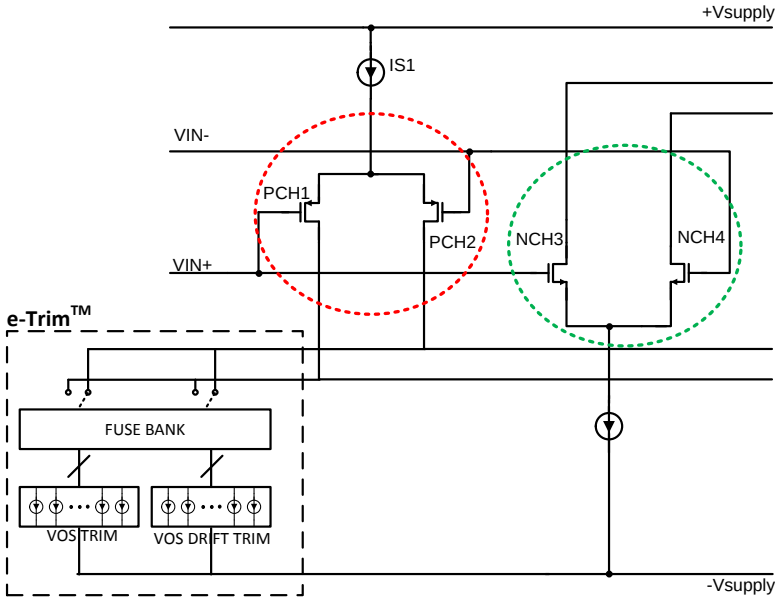


Figure 43. Rail-to-Rail Input Stage

To achieve the best performance for two-stage rail-to-rail input amplifiers, avoid the transition region when possible. The OPA192 uses a precision trim for both the N-channel and P-channel regions. This technique enables significantly lower levels of offset than previous-generation devices, causing variance in the transition region of the input stages to appear exaggerated relative to offset over the full common-mode range, as shown in Figure 44.

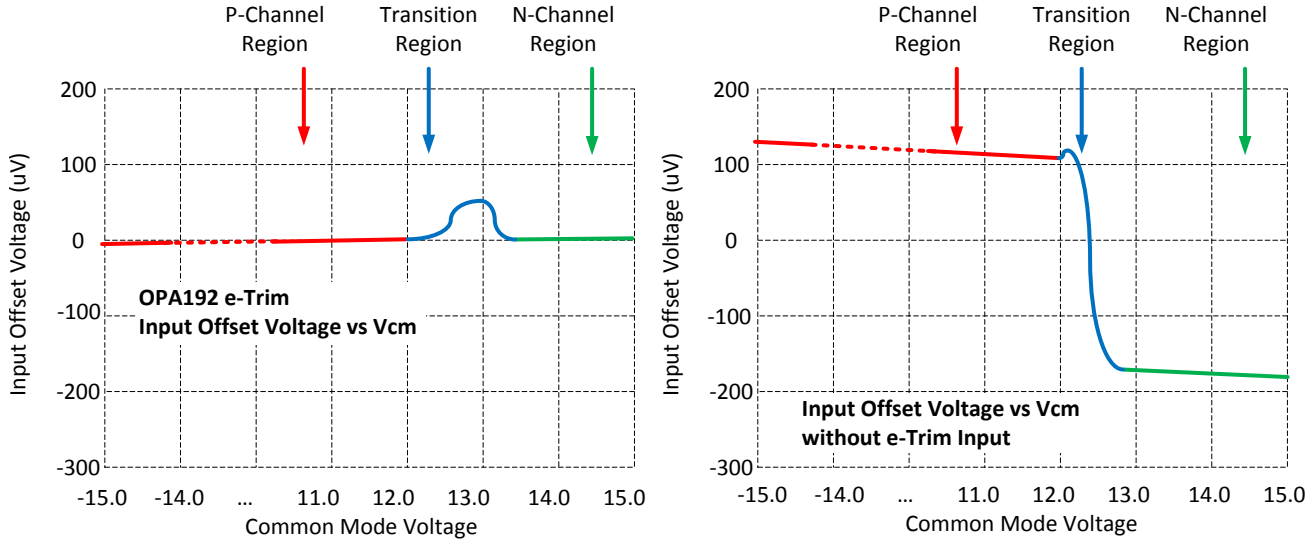


Figure 44. Common-Mode Transition vs Standard Rail-to-Rail Amplifiers

INPUT PROTECTION CIRCUITRY

The OPA192 uses a unique input architecture to eliminate the need for input protection diodes but still provides robust input protection under transient conditions. Conventional input diode protection schemes shown in Figure 45 can be activated by fast transient step responses and can introduce signal distortion and settling time delays due to alternate current paths, as shown in Figure 46. For low-gain circuits, these fast-ramping input signals forward-bias back-to-back diodes causing an increase in input current and resulting in extended settling time, as seen in Figure 47.

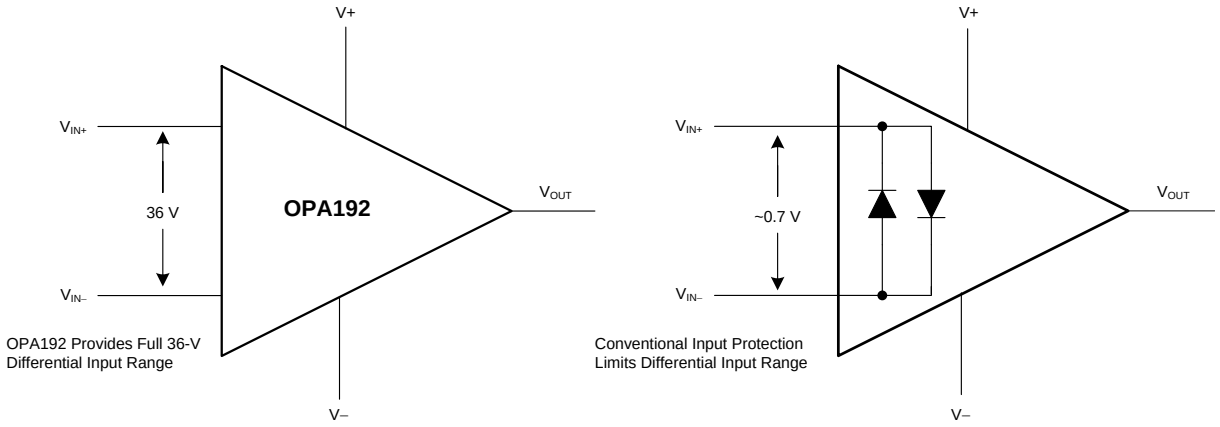


Figure 45. OPA192 Input Protection Does Not Limit Differential Input Capability

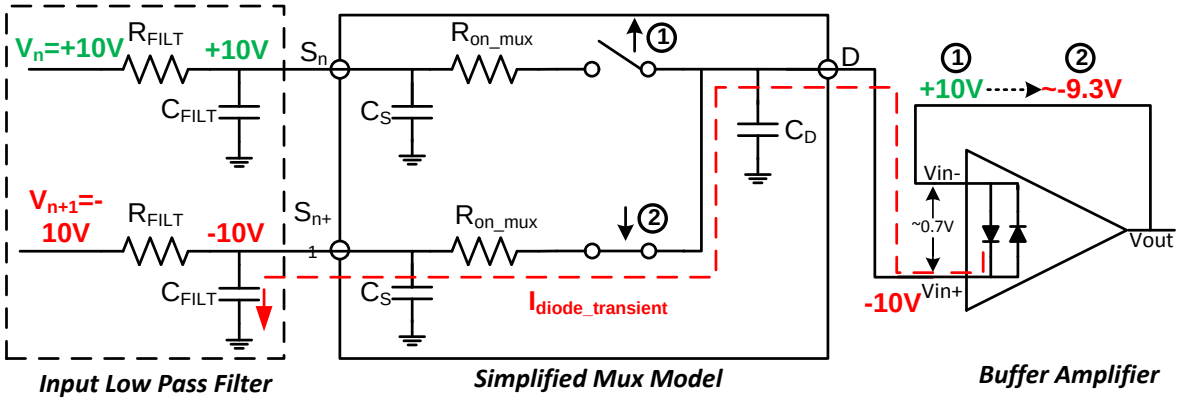


Figure 46. Back-to-Back Diodes Create Settling Issues

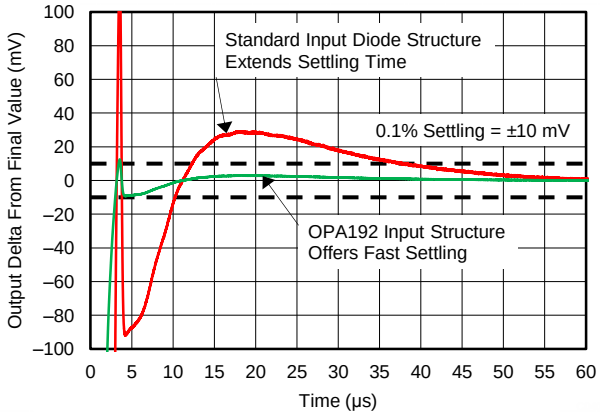


Figure 47. OPA192 Protection Circuit Maintains Fast-Settling Transient Response

The OPA192 family of operational amplifiers provides a true high-impedance differential input capability for high-voltage applications. This patented input protection architecture does not introduce additional signal distortion or delayed settling time, making it an optimal op amp for multichannel, high-switched, input applications. The OPA192 can tolerate a maximum differential swing (voltage between inverting and noninverting terminal of the op amp) of up to 36 V, making it suitable for use as a comparator or in applications with fast-ramping input signals, such as multiplexed data-acquisition systems, as shown in Figure 55.

PHASE REVERSAL PROTECTION

The OPA192 family has internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The OPA192 is a rail-to-rail input op amp; therefore, the common-mode range can extend up to the rails. Input signals beyond the rails do not cause phase reversal; instead, the output limits into the appropriate rail. This performance is shown in Figure 48.

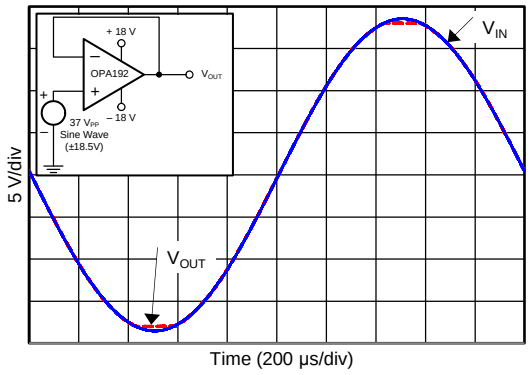


Figure 48. No Phase Reversal

THERMAL PROTECTION

The internal power dissipation of any amplifier causes its internal (junction) temperature to rise. This phenomenon is called *self heating*. The absolute maximum junction temperature of the OPA192 is +150°C. Exceeding this temperature causes damage to the device. The OPA192 has a thermal protection feature that prevents damage from self heating. The protection works by monitoring the temperature of the device and turning off the op amp output drive for temperatures above +140°C. Figure 49 shows an application example for the OPA192 that will have significant self heating (+159°C) because of its power dissipation (0.81 W). Thermal calculations indicate that for an ambient temperature of +65°C the device junction temperature should reach +187°C. The actual device, however, turns off the output drive to maintain a safe junction temperature. Figure 49 depicts how the circuit behaves during thermal protection. During normal operation, the device acts as a buffer so the output is 3 V. When self heating causes the device junction temperature to increase above +140°C, the thermal protection forces the output to a high-impedance state and the output is pulled to ground through resistor RL.

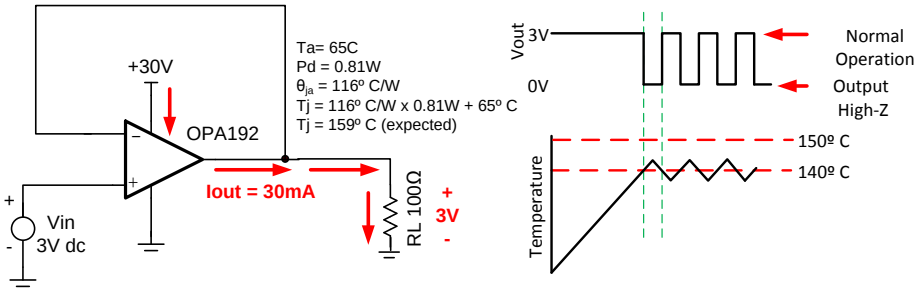


Figure 49. Thermal Protection

OVERLOAD RECOVERY

Overload recovery is defined as the time it takes for the op amp output to recover from a saturated state to a linear state. The output devices of the op amp enter a saturation region when the output voltage exceeds the rated operating voltage, either due to the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the OPAx192 is approximately 200 ns.

GENERAL LAYOUT GUIDELINES

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable to single-supply applications.
- In order to reduce parasitic coupling, run the input traces as far away from the supply lines as possible.
- A ground plane helps distribute heat and reduces EMI noise pickup.
- Place the external components as close to the device as possible. This configuration prevents parasitic errors (such as the Seebeck effect) from occurring.

CAPACITIVE LOAD AND STABILITY

The OPA192 features a patented output stage capable of driving large capacitive loads, and in a unity-gain configuration, can directly drive up to 1 nF of pure capacitive load. Increasing the gain enhances the ability of the amplifier to drive greater capacitive loads, as shown in Figure 50 and Figure 51. The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier will be stable in operation.

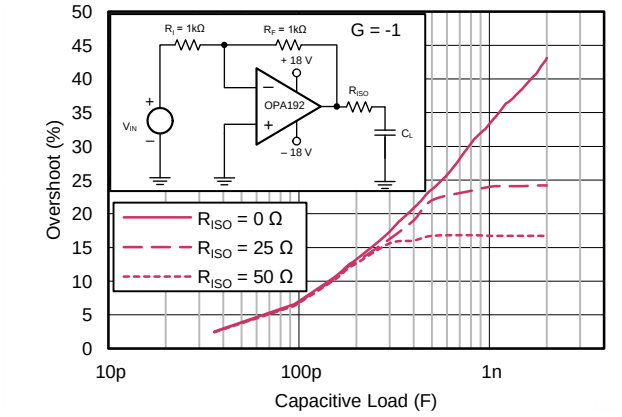


Figure 50. Small-Signal Overshoot vs Capacitive Load (100-mV output step)

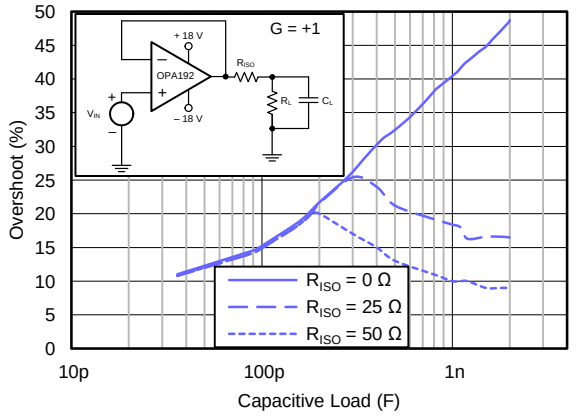


Figure 51. Small-Signal Overshoot vs Capacitive Load (100-mV output step)

For additional drive capability in unity-gain configurations, capacitive load drive can be improved by inserting a small (10 Ω to 20 Ω) resistor, R_{ISO}, in series with the output, as shown in Figure 52. This resistor significantly reduces ringing while maintaining dc performance for purely capacitive loads. However, if there is a resistive load in parallel with the capacitive load, a voltage divider is created, introducing a gain error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio R_{ISO} / R_L, and is generally negligible at low output levels. A high capacitive load drive makes the OPA192 well suited for applications such as reference buffers, MOSFET gate drives, and cable-shield drives. The circuit shown in Figure 52 uses an isolation resistor (R_{ISO}) to stabilize the output of an op amp. R_{ISO} modifies the open-loop gain of the system for increased phase margin, and results using the OPA192 are summarized in Table 3. For additional information on techniques to optimize and design using this circuit, TI Precision Design TIDU032 details complete design goals, simulation, and test results.

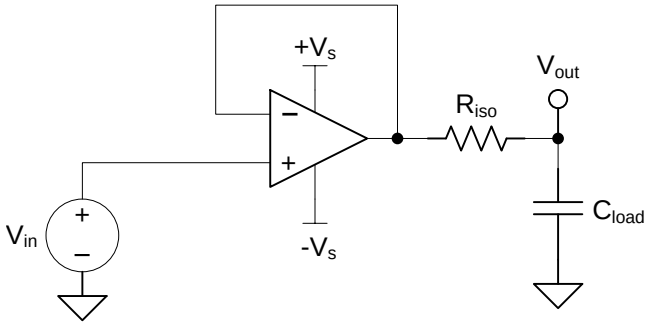


Figure 52. Extending Capacitive Load Drive with the OPA192

Table 3. OPA192 Capacitive Load Drive Solution Using Isolation Resistor Comparison of Calculated and Measured Results

Capacitive Load	100 pF		1000 pF		0.01 µF		0.1 µF		1 µF	
Phase Margin	45°	60°	45°	60°	45°	60°	45°	60°	45°	60°
R_{ISO} (Ω)	47.0	360.0	24.0	100.0	20.0	51.0	6.2	15.8	2.0	4.7
Measured Overshoot (%)	23.2 8.6	10.4	22.5	9.0	22.1	8.7	23.1	8.6	21.0	8.6
Calculated PM	45.1°	58.1°	45.8°	59.7°	46.1°	60.1°	45.2°	60.2°	47.2°	60.2°

For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, refer to *TI Precision Design TIDU032 - Capacitive Load Drive Solution using an Isolation Resistor*

APPLICATION INFORMATION

TI PRECISION DESIGNS

The OPA192 is featured in several TI Precision Designs, available online at http://www.ti.com/ww/en/analog/precision-designs/. TI Precision Designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits.

SLEW RATE LIMIT FOR INPUT PROTECTION

In control systems for valves or motors, abrupt changes in voltages or currents can cause mechanical damages. By controlling the slew rate of the command voltages into the drive circuits, the load voltages can ramp up and down at a safe rate. For symmetrical slew-rate applications (positive slew rate equals negative slew rate) one additional op amp provides slew-rate control for a given analog gain stage. The unique input protection and high output current and slew rate of the OPA192 make it an optimal amplifier to achieve slew rate control for both dual- and single-supply systems. Figure 53 shows the OPA192 in a slew-rate limit design.

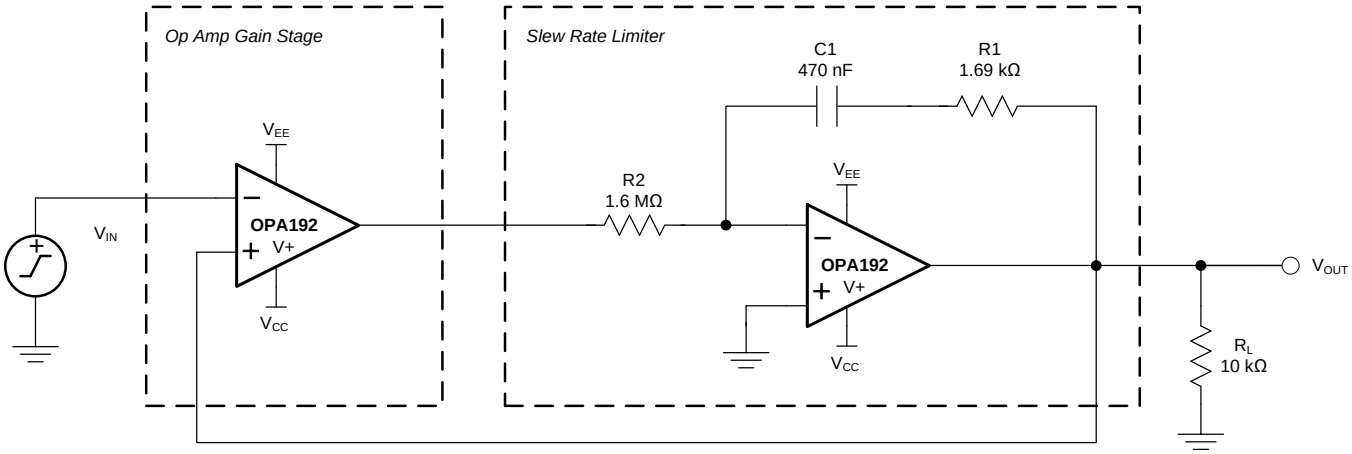


Figure 53. Slew Rate Limiter Uses One Op Amp

For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, refer to *TI Precision Design TIDU026 - Slew Rate Limiter Uses One Op Amp*

PRECISION REFERENCE BUFFER

The OPA192 features high output current drive capability and low input offset voltage, making it an excellent reference buffer to provide an accurate buffered output with ample drive current for transients. For the 10-µF ceramic capacitor shown in Figure 54, R_{ISO}, a 37.4-Ω isolation resistor, provides separation of two feedback paths for optimal stability. Feedback path number one is through R_F and is directly at the output, V_{OUT}. Feedback path number two is through R_{Fx} and C_F and is connected at the output of the op amp. The optimized stability components shown for the 10-µF load give a closed-loop signal bandwidth at V_{OUT} of 4 kHz, while still providing a loop gain phase margin of 89°. Any other load capacitances require recalculation of the stability components: R_F, R_{Fx}, C_F, and R_{ISO}.

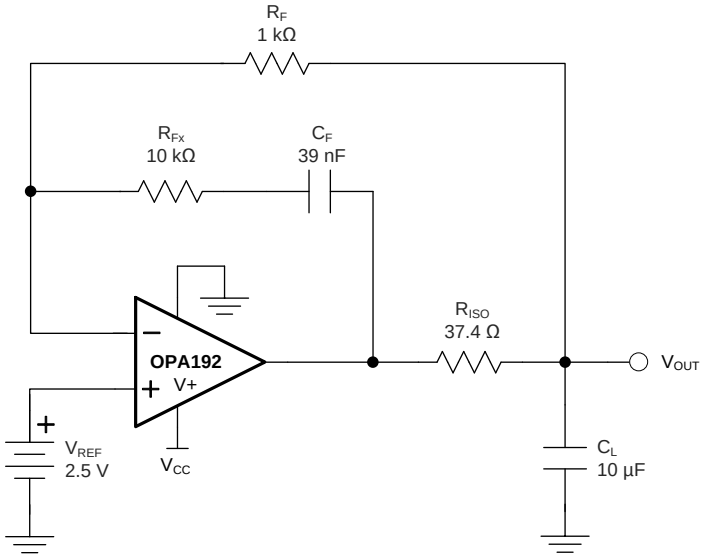


Figure 54. Precision Reference Buffer

16-BIT PRECISION MULTIPLEXED DATA-ACQUISITION SYSTEM

Figure 55 shows a 16-bit, differential, 4-channel, multiplexed data-acquisition system. This example is typical in industrial applications that require low distortion and a high-voltage differential input. The circuit uses the ADS8864, a 16-bit, 400-kSPS successive-approximation-resistor (SAR) analog-to-digital converter (ADC), along with a precision, high-voltage, signal-conditioning front end, and a 4-channel differential multiplexer (mux). This TI Precision Design details the process for optimizing the precision, high-voltage, front-end drive circuit using the OPA192 and OPA140 to achieve excellent dynamic performance and linearity with the ADS8864.

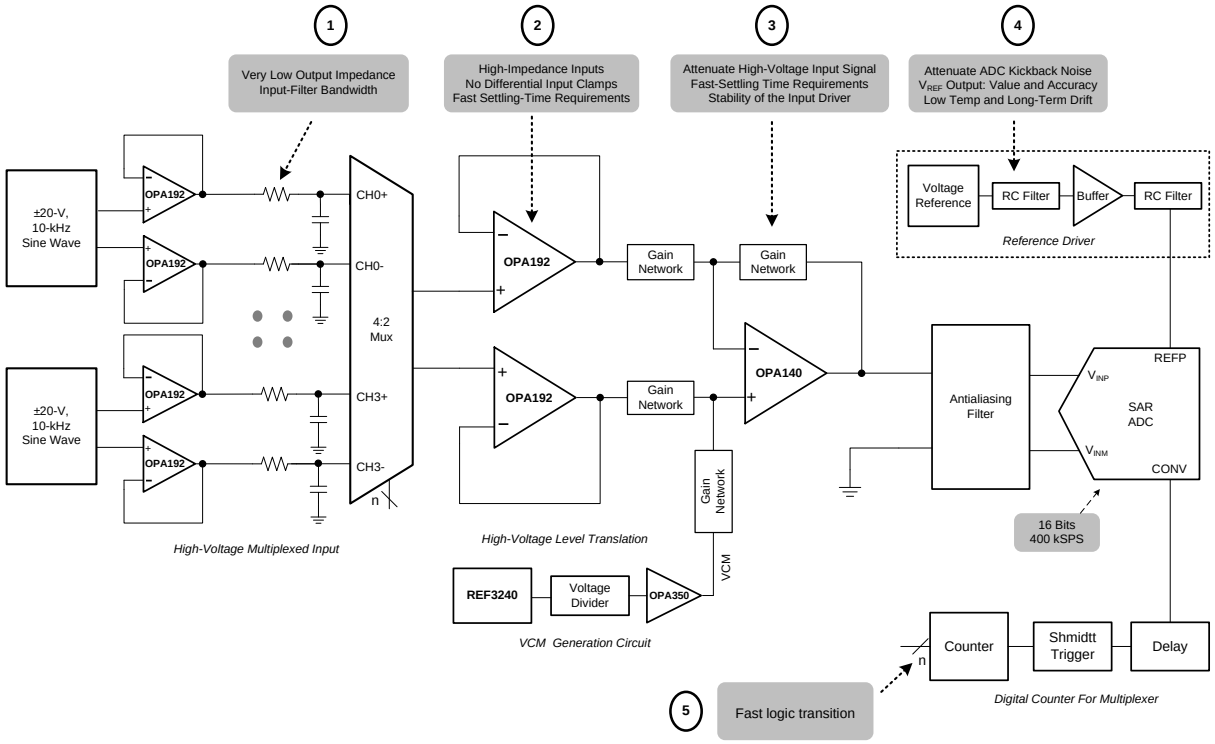


Figure 55. OPA192 in 16-Bit, 400-kSPS, 4-Channel, Multiplexed Data Acquisition System for High-Voltage Inputs with Lowest Distortion

For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, refer to *TI Precision Design TIDU181 - 16-bit, 400-kSPS, 4-Channel, Multiplexed Data Acquisition System for High Voltage Inputs with Lowest Distortion*

TINA-TI™ (Free Download Software)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

NOTE

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (December 2013) to Revision A	Page
• Changed first paragraph of *16-BIT PRECISION MULTIPLEXED DATA-ACQUISITION SYSTEM* section	25
• Changed Figure 55 and title	25
• Changed TIDU181 reference design title	25

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA192IDBVR	PREVIEW	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OUYS	
OPA192IDBVT	PREVIEW	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OUYS	
OPA192IDGKR	PREVIEW	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OUXS	
OPA192IDGKT	PREVIEW	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OUXS	
OPA2192ID	PREVIEW	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2192	
OPA2192IDGK	PREVIEW	VSSOP	DGK	8	80	TBD	Call TI	Call TI	-40 to 125		
OPA2192IDGKR	PREVIEW	VSSOP	DGK	8	2500	TBD	Call TI	Call TI	-40 to 125		
OPA2192IDR	PREVIEW	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2192	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

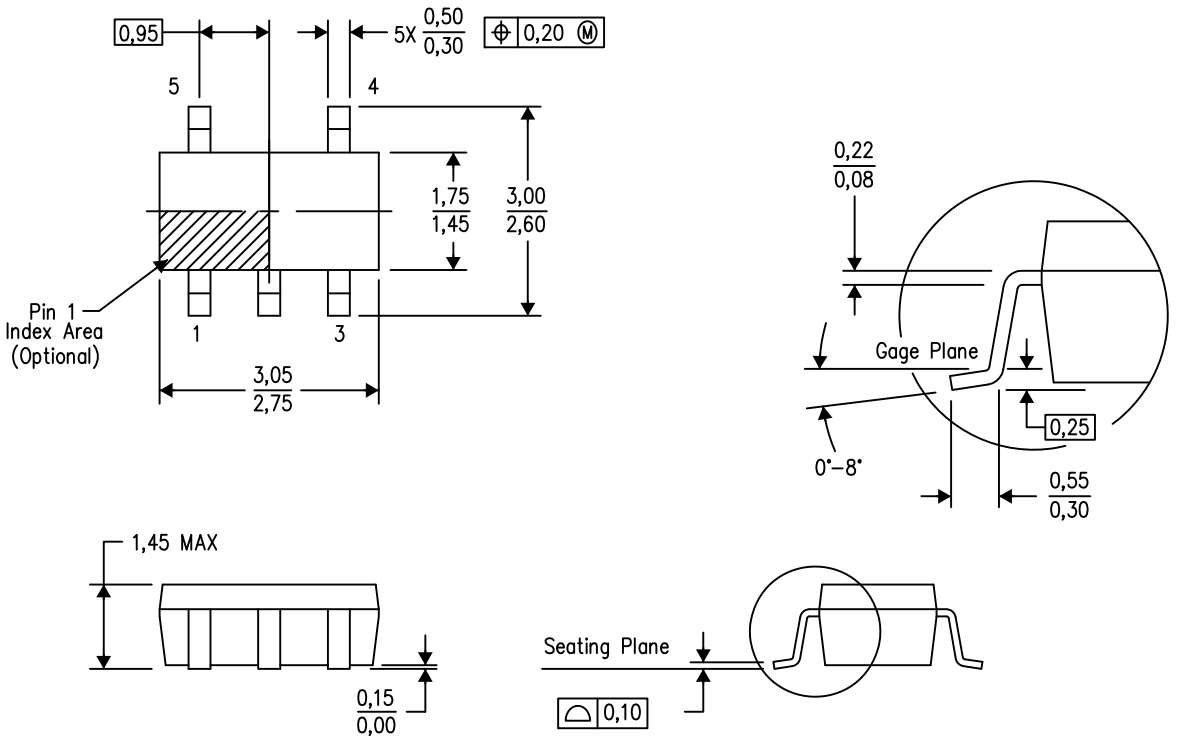
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

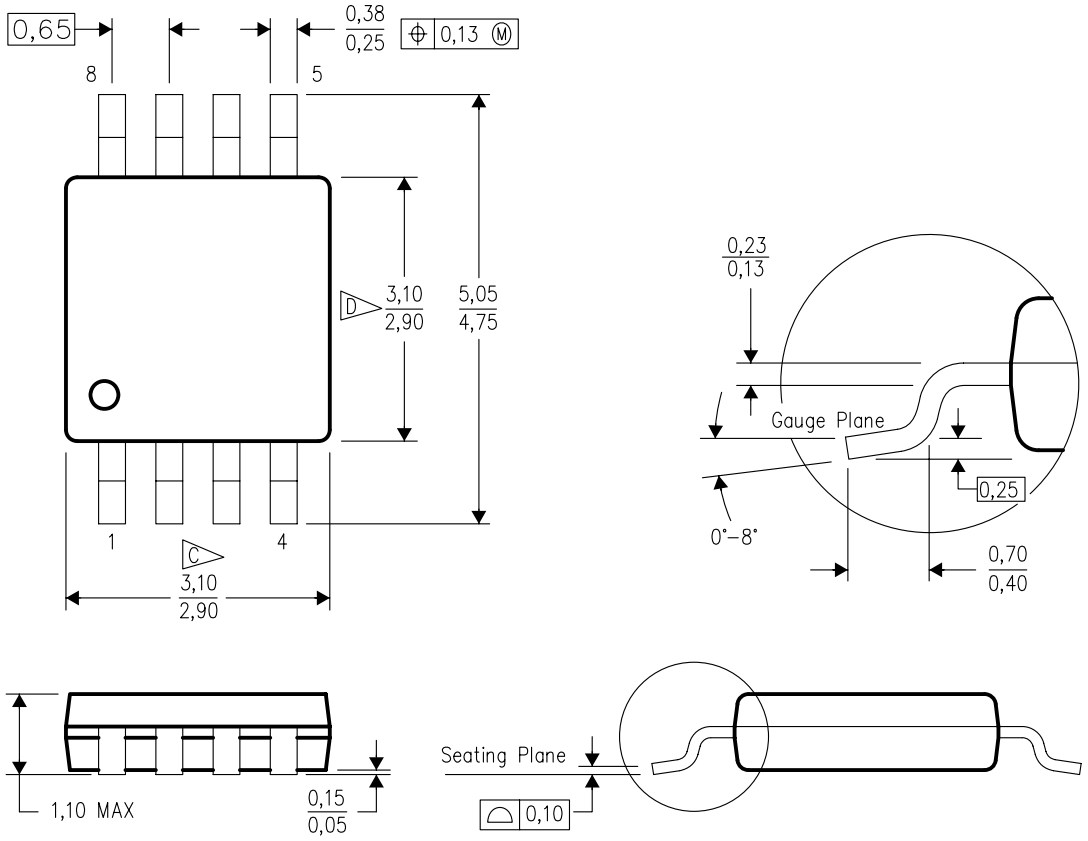
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/L 08/2013

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
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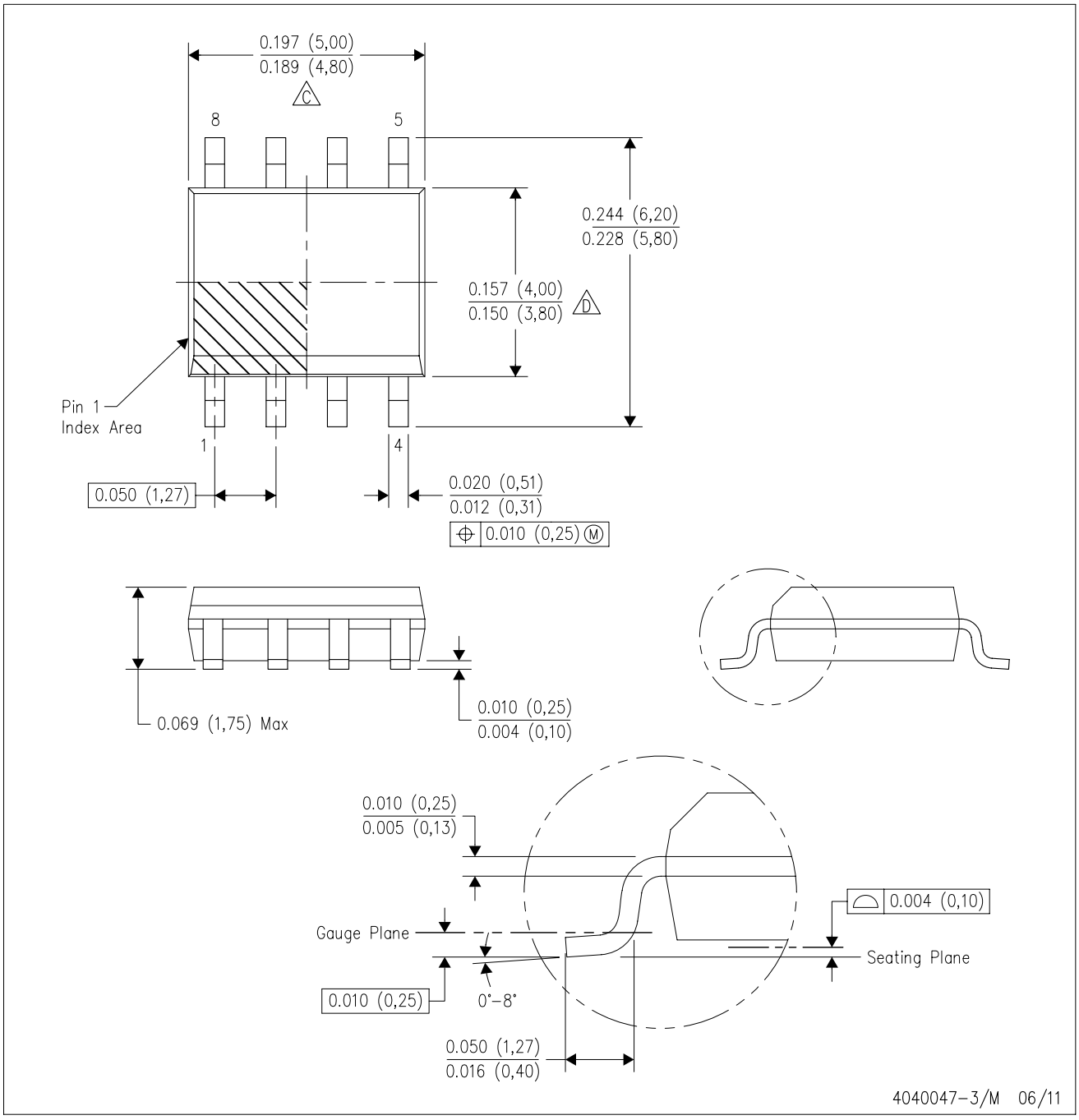
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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