PI74ALVCH16721

3.3V 20-Bit Flip-Flop with 3-STATE Outputs

Product Features

- PI74ALVCH16721 is designed for low voltage operation
- V_{CC} = 2.3V to 3.6V
- Hysteresis on all inputs
- Typical V_{OLP} (Output Ground Bounce) < 0.8V at V_{CC} = 3.3V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) < 2.0V at V_{CC} = 3.3V, T_A = 25°C
- Bus Hold retains last active bus state during 3-STATE, eliminating the need for external pullup resistors
- Industrial operation at –40°C to +85°C
- Packages available:
  – 56-pin 240 mil wide plastic TSSOP (A)
  – 56-pin 300 mil wide plastic SSOP (V)

Product Description

Pericom Semiconductor's PI74ALVCH series of logic circuits are produced in the Company's advanced 0.5 micron CMOS technology, achieving industry leading speed.

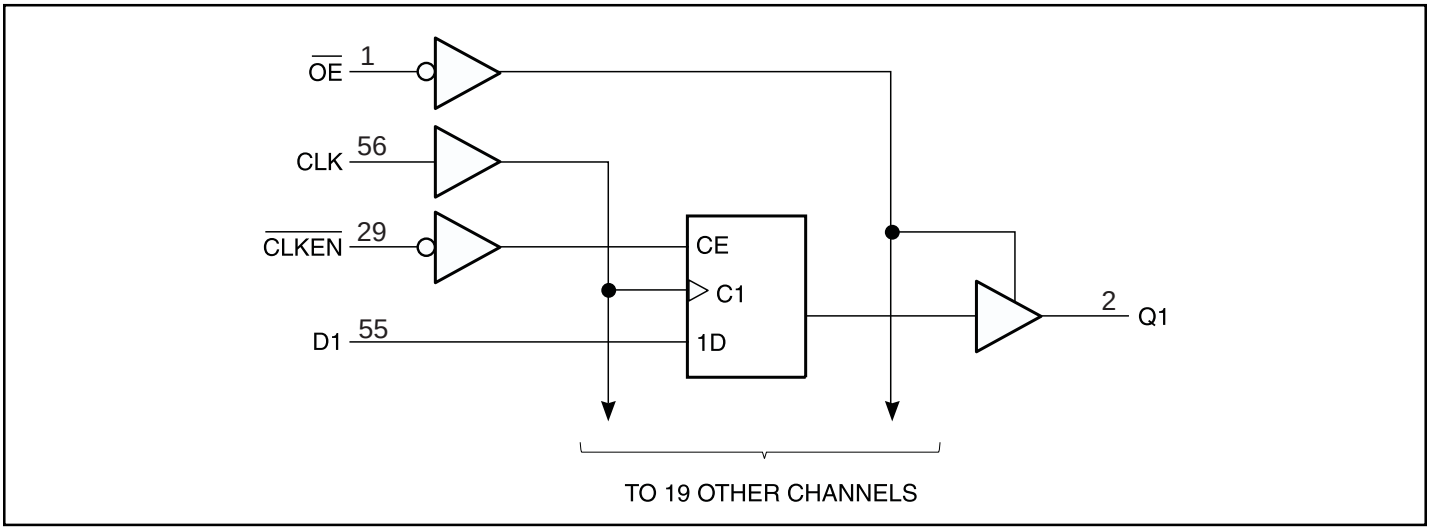
The PI74ALVCH16721 is a 20-bit flip-flop with 3-state outputs designed specifically for 2.3V to 3.6V V_{CC} operation. The PI74ALVCH16721 is designed with edge-triggered D-type flip-flops with qualified clock storage. On the positive transition of clock (CLK) input, the device provides true data at the Q outputs, provided that the clock-enable ($\overline{CLKEN}$) input is LOW. If $\overline{CLKEN}$ is HIGH, no data is stored.

A buffered output-enable ($\overline{OE}$) input can be used to place the 20 outputs in either a normal logic state (HIGH or LOW level) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capacity to drive bus lines without the need for interface or pullup components. $\overline{OE}$ does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The PI74ALVCH16721 data has "Bus Hold" which retains the data input's last state whenever the data input goes to high-impedance preventing "floating" inputs and eliminating the need for pullup/down resistors.

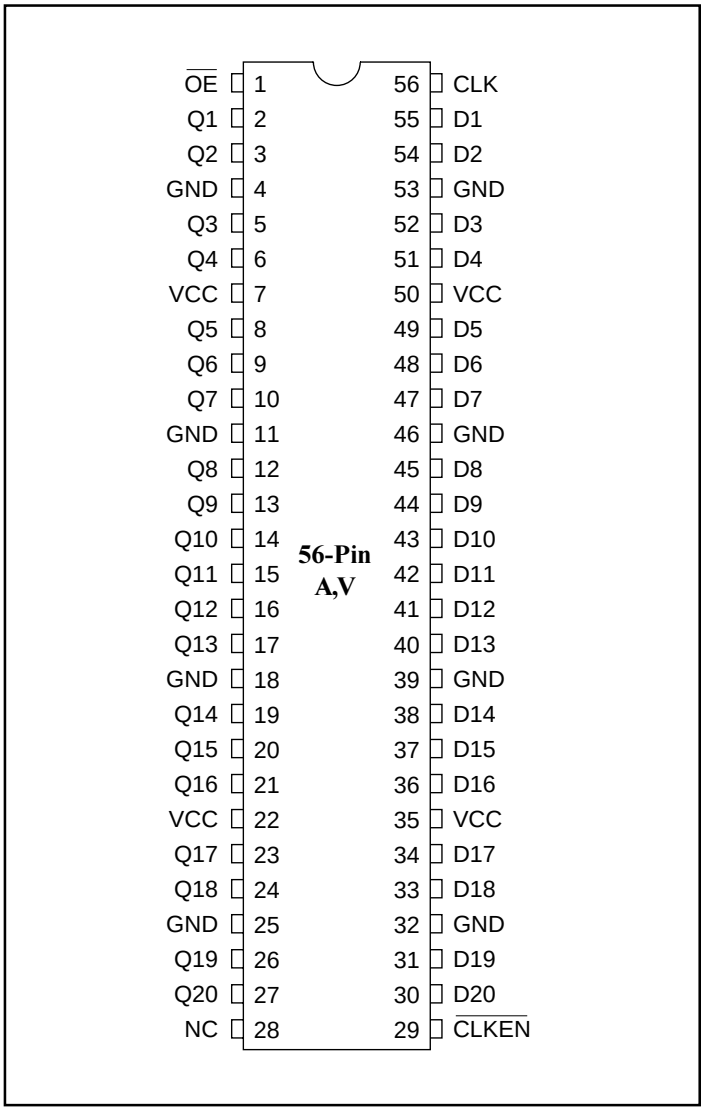
Logic Block Diagram



Product Pin Description

Pin Name	Description
$\overline{OE}$	Output Enable Input (Active LOW)
$\overline{CLKEN}$	Clock Enable Input (Active LOW)
CLK	Clock Input (Active HIGH)
Dx	Data Inputs
Qx	3-State Outputs
GND	Ground
V_{CC}	Power

Product Pin Configuration



Truth Table[1]

Inputs				Outputs
$\overline{OE}$	$\overline{CLKEN}$	CLK	Dx	Qx
L	H	X	X	Q_0
L	L	↑	H	H
L	L	↑	L	L
L	L	L or H	X	Q_0
H	X	X	X	Z

Notes:

1. H = High Signal Level
   L = Low Signal Level
   X = Don't Care or Irrelevant
   Z = High Impedance
   ↑ = LOW-to-HIGH Transition

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–40°C to +85°C
Input Voltage Range, V_{IN}	–0.5V to V_{CC} +0.5V
Output Voltage Range, V_{OUT}	–0.5V to V_{CC} +0.5V
DC Input Voltage	–0.5V to +5.0V
DC Output Current	100 mA
Power Dissipation	1.0W

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, T_A = –40°C to +85°C, V_{CC} = 3.3V ±10%)

Parameters	Description	Test Conditions[1]	Min.	Typ.[2]	Max.	Units
V_{CC}	Supply Voltage		2.3		3.6	V
V_{IH}[3]	Input HIGH Voltage	V_{CC} = 2.3V to 2.7V	1.7			
		V_{CC} = 2.7V to 3.6V	2.0			
V_{IL}[3]	Input LOW Voltage	V_{CC} = 2.3V to 2.7V			0.7	
		V_{CC} = 2.7V to 3.6V			0.8	
V_{IN}[3]	Input Voltage		0		V_{CC}	
V_{OUT}[3]	Output Voltage		0		V_{CC}	
V_{OH}	Output HIGH Voltage	I_{OH} = -100µA, V_{CC} = Min. to Max.	V_{CC} -0.2			
		V_{IH} = 1.7V, I_{OH} = -6mA, V_{CC} = 2.3V	2.0			
		V_{IH} = 1.7V, I_{OH} = -12mA, V_{CC} = 2.3V	1.7			
		V_{IH} = 2.0V, I_{OH} = -12mA, V_{CC} = 2.7V	2.2			
		V_{IH} = 2.0V, I_{OH} = -12mA, V_{CC} = 3.0V	2.4			
		V_{IH} = 2.0V, I_{OH} = -24mA, V_{CC} = 3.0V	2.0			
V_{OL}	Output LOW Voltage	I_{OL} = 100µA, V_{IL} = Min. to Max.			0.2	
		V_{IL} = 0.7V, I_{OL} = 6mA, V_{CC} = 2.3V			0.4	
		V_{IL} = 0.7V, I_{OL} = 12mA, V_{CC} = 2.3V			0.7	
		V_{IL} = 0.8V, I_{OL} = 12mA, V_{CC} = 2.7V			0.4	
		V_{IL} = 0.8V, I_{OL} = 24mA, V_{CC} = 3.0V			0.55	
I_{OH}[3]	Output HIGH Current	V_{CC} = 2.3V			-12	mA
		V_{CC} = 2.7V			-12	
		V_{CC} = 3.0V			-24	
I_{OL}[3]	Output LOW Current	V_{CC} = 2.3V			12	
		V_{CC} = 2.7V			12	
		V_{CC} = 3.0V			24	

DC Electrical Characteristics-Continued (Over the Operating Range, T_A = –40°C to +85°C, V_{CC} = 3.3V ±10%)

Parameters	Description	Test Conditions[1]	Min.	Typ.[2]	Max.	Units
I_{IN}	Input Current	V_{IN} = V_{CC} or GND, V_{CC} = 3.6V			±5	μA
I_{IN} (HOLD)	Input Hold Current	V_{IN} = 0.7V, V_{CC} = 2.3V	45			
		V_{IN} = 1.7V, V_{CC} = 2.3V	-45			
		V_{IN} = 0.8V, V_{CC} = 3.0V	75			
		V_{IN} = 2.0V, V_{CC} = 3.0V	-75			
		V_{IN} = 0 to 3.6V, V_{CC} = 3.6V			±500	
I_{OZ}	Output Current (3-STATE Outputs)	V_{OUT} = V_{CC} or GND, V_{CC} = 3.6V			±10	
I_{CC}	Supply Current	V_{CC} = 3.6V, I_{OUT} = 0μA, V_{IN} = GND or V_{CC}			40	
ΔI_{CC}	Supply Current per Input @ TTL HIGH	V_{CC} = 3.0V to 3.6V One Input at V_{CC} - 0.6V Other Inputs at V_{CC} or GND			750	
C_I	Control Inputs	V_{IN} = V_{CC} or GND, V_{CC} = 3.3V		3		pF
	Data Inputs			6		
C_O	Outputs	V_O = V_{CC} or GND, V_{CC} = 3.3V		7		

Notes:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient and maximum loading.
3. Unused Control Inputs must be held HIGH or LOW to prevent them from floating.

Switching Characteristics over Operating Range[1]

Parameters	Description	Conditions[1]	V_{CC} = 2.5V ±0.2V		V_{CC} = 2.7V		V_{CC} = 3.3V ±0.3V		Units
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
f_{CLOCK}	Clock Frequency	C_L = 50pF R_L = 500Ω	0	150	0	150	0	150	MHz
f_{MAX}	Maximum Frequency		150		150		150		
t_{PLH}, t_{PHL}	Propogation Delay CLK to Qx		1.0	5.6	1.0	5.1	1.0	4.3	ns
t_{PZH}, t_{PZL}	Output Enable Time $\overline{OE}$ to Qx			6.1		5.8		4.8	
t_{PHX}	Output Disable Time $\overline{OE}$ to Qx			5.5		4.7		4.4	
t_{SU}	Data Before CLK↑		4		3.6		3.1		
t_{SU}	$\overline{CLKEN}$ Before CLK↑		3.4		3.1		2.7		
t_H	Data After CLK↑		0		0		0		
t_H	$\overline{CLKEN}$ After CLK↑		0		0		0		
t_W	Pulse Width[3] CLK HIGH or LOW		3.3		3.3		3.3		
$\Delta t/\Delta v$[4]	Input Transition RISE or FALL		0	10	0	10	0	10	ns/V

Notes:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Recommended operating condition.

Operating Characteristics, T_A = 25°C

Parameter		Test Conditions	V_{CC} = 2.5V ±0.2V	V_{CC} = 3.3V ±0.3V	Units
			Typ.		
C_{PD} Power Dissipation Capacitance	Outputs Enabled	C_L = 50pF, f = 10 MHz	55	59	pF
	Outputs Disabled		46	49	