

PIC24FJ256DA210 Family Silicon Errata and Data Sheet Clarification

The PIC24FJ256DA210 Family devices that you have received conform functionally to the current Device Data Sheet (DS39969B), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in [Table 1](#). The silicon issues are summarized in [Table 2](#).

The errata described in this document will be addressed in future revisions of the PIC24FJ256DA210 Family silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of [Table 2](#) apply to the current silicon revision (A4).

Data Sheet clarifications and corrections start on [page 1](#), following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 2 or PICKit™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 2 programmer/debugger or PICKit™ 3.
2. From the main menu in MPLAB IDE, select *Configure>Select Device*, and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (*Debugger>Select Tool*).
4. Perform a "Connect" operation to the device (*Debugger>Connect*). Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC24FJ256DA210 Family silicon revisions are shown in [Table 1](#).

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID ⁽¹⁾	Revision ID for Silicon Revision ⁽²⁾	
		A3	A4
PIC24FJ256DA210	410Eh	03h	04h
PIC24FJ256DA206	410Ch		
PIC24FJ256DA110	410Fh		
PIC24FJ256DA106	410Dh		
PIC24FJ128DA210	410Ah		
PIC24FJ128DA206	4108h		
PIC24FJ128DA110	410Bh		
PIC24FJ128DA106	4109h		

- Note 1:** The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".
- 2:** Refer to the "*PIC24FJXXDA1/DA2/GB2 Families Flash Programming Specification*" (DS39970) for detailed information on Device and Revision IDs for your specific device.

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TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions ⁽¹⁾	
				A3	A4
Oscillator	Two-Speed Start-up	1.	Feature is not functional.	X	X
Resets	—	2.	POR flag also set on BOR and External Reset.	X	X
Enhanced PMP	—	3.	Write incompatibility with certain slave devices.	X	X
A/D Converter	—	4.	Module continues to draw current when disabled.	X	X
Interrupts	INTx	5.	External interrupts missed when writing to INTCON2.	X	X
Output Compare	Cascaded Mode	6.	Some modes are unavailable in Cascaded mode.	X	X
USB	Host Mode	7.	Low-speed devices, when connected to a hub, will not work.	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

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Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A4**).

1. Module: Oscillator (Two-Speed Start-up)

Two-Speed Start-up is not functional. Leaving the IESO Configuration bit in its default state (Two-Speed Start-up enabled) may result in unpredictable operation.

Work around

None. Always program the IESO Configuration bit to disable the feature (CW2<15> = 0).

Affected Silicon Revisions

A3	A4						
X	X						

2. Module: Resets

On Brown-out Resets and External (Master Clear) Resets, the POR bit may also become set. This may cause Brown-out and External Reset conditions to be indistinguishable from a Power-on Reset.

Work around

None.

Affected Silicon Revisions

A3	A4						
X	X						

3. Module: Enhanced PMP

The module is not write-compatible with slave devices that require data to be present before the Write strobe is asserted. The module has no configuration provision to output data before asserting the Write strobe.

Since most slave devices require valid input data to be present before the Write strobe is de-asserted, the significance of this issue is thought to be limited.

Work around

None.

Affected Silicon Revisions

A3	A4						
X	X						

4. Module: A/D Converter

Once the A/D module is enabled (AD1CON1<15> = 1), it may continue to draw extra current even if the module later is disabled (AD1CON1<15> = 0).

Work around

In addition to disabling the module through the ADON bit, set the corresponding PMD bit, ADC1MD (PMD1<0>), to power it down completely.

Affected Silicon Revisions

A3	A4						
X	X						

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5. Module: Interrupts (INTx)

Writing to the INTCON2 register may cause an external interrupt event (inputs on INT0 through INT4) to be missed. This only happens when the interrupt event and the write event occur during the same clock cycle.

Work around

If this cannot be avoided, write the data intended for INTCON2 to any other register in the interrupt block of the SFR (addresses, 0080h to 00E0h); then write the data to INTCON2.

Be certain to write the data to a register not being actively used by the application, or to any of the interrupt flag registers, in order to avoid spurious interrupts. For example, if the interrupts controlled by IEC5 are not being used in the application, the code sequence would be:

```
IEC5 = 0x1E;  
INTCON2 = 0x1E;  
IEC5 = 0;
```

It is the user's responsibility to determine an appropriate register for the particular application.

Affected Silicon Revisions

A3	A4						
X	X						

6. Module: Output Compare (Cascaded Mode)

When 32-bit Cascaded mode is enabled ($OCxCON2\langle 8 \rangle = 1$), these modes are unavailable:

- Single-Shot operations when OCM ($OCxCON1\langle 2:0 \rangle = 110$ or 111 and OCTRIG ($OCxCON2\langle 7 \rangle = 1$ and TRIGMODE ($OCxCON1\langle 3 \rangle = 1$).
- Synchronous modes when the SYNCSEL bits ($OCxCON2\langle 4:0 \rangle \neq 00000$ and OCTRIG ($OCxCON2\langle 7 \rangle = 0$).

Work around

None.

Affected Silicon Revisions

A3	A4						
X	X						

7. Module: USB

While operating in Host mode and attached to a low-speed device through a full-speed USB hub, the host may persistently drive the bus to an SE0 state (both D+/D- as 0) which would be interpreted as a bus Reset condition by the hub; or the host may persistently drive the bus to a J state, which would make the hub detach condition undetectable by the host.

Work around

Connect low-speed devices directly to the host USB port and not through a USB hub.

Affected Silicon Revisions

A3	A4						
X	X						

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Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS39969B):

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Guidelines for Getting Started with 16-Bit Microcontrollers

Section 2.4 Voltage Regulator Pins (ENVREG/DISVREG and VCAP/VDDCORE) has been replaced with a new and more detailed section. The entire text follows:

2.4 Voltage Regulator Pins (ENVREG/DISVREG and VCAP/VDDCORE)

The on-chip voltage regulator enable pin must always be connected directly to a supply voltage.

Refer to **Section 27.2 “On-Chip Voltage Regulator”** for details on connecting and using the on-chip regulator.

When the regulator is enabled, a low-ESR ($< 5\Omega$) capacitor is required on the VCAP pin to stabilize the voltage regulator output voltage. The VCAP pin must not be connected to VDD and must use a capacitor of $10\ \mu\text{F}$ connected to ground. The type can be ceramic or tantalum. Suitable examples of capacitors are shown in [Table 2-1](#). Capacitors with equivalent specifications can be used.

Designers may use [Figure 2-3](#) to evaluate ESR equivalence of candidate devices.

The placement of this capacitor should be close to VCAP. It is recommended that the trace length not exceed 0.25 inch (6 mm). Refer to **Section 30.0 “Electrical Characteristics”** for additional information.

FIGURE 2-3 FREQUENCY vs. ESR PERFORMANCE FOR SUGGESTED VCAP

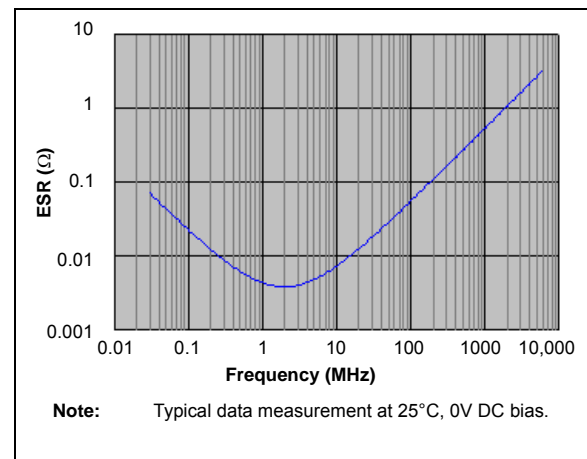


TABLE 2-1 SUITABLE CAPACITOR EQUIVALENTS

Make	Part #	Nominal Capacitance	Base Tolerance	Rated Voltage	Temp. Range
TDK	C3216X7R1C106K	10 μF	$\pm 10\%$	16V	-55 to +125°C
TDK	C3216X5R1C106K	10 μF	$\pm 10\%$	16V	-55 to +85°C
Panasonic	ECJ-3YX1C106K	10 μF	$\pm 10\%$	16V	-55 to +125°C
Panasonic	ECJ-4YB1C106K	10 μF	$\pm 10\%$	16V	-55 to +85°C
Murata	GRM32DR71C106KA01L	10 μF	$\pm 10\%$	16V	-55 to +125°C
Murata	GRM31CR61C106KC31L	10 μF	$\pm 10\%$	16V	-55 to 85°C+

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2.4.1 CONSIDERATIONS FOR CERAMIC CAPACITORS

In recent years, large value, low-voltage, surface mount ceramic capacitors have become very cost effective in sizes up to a few tens of microfarad. The low-ESR, small physical size and other properties make ceramic capacitors very attractive in many types of applications.

Ceramic capacitors are suitable for use with the internal voltage regulator of this microcontroller. However, some care is needed in selecting the capacitor to ensure that it maintains sufficient capacitance over the intended operating range of the application.

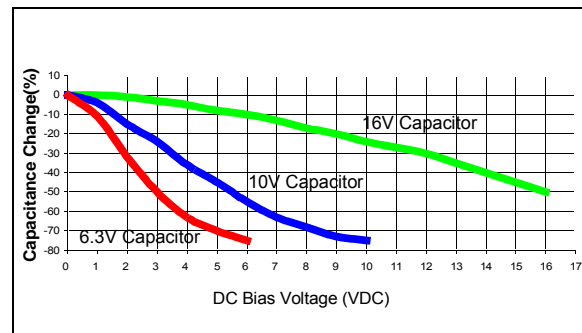
Typical low-cost, 10 μF ceramic capacitors are available in X5R, X7R and Y5V dielectric ratings (other types are also available, but are less common). The initial tolerance specifications for these types of capacitors are often specified as $\pm 10\%$ to $\pm 20\%$ (X5R and X7R), or $-20\%/+80\%$ (Y5V). However, the effective capacitance that these capacitors provide in an application circuit will also vary based on additional factors, such as the applied DC bias voltage and the temperature. The total in-circuit tolerance is, therefore, much wider than the initial tolerance specification.

The X5R and X7R capacitors typically exhibit satisfactory temperature stability (ex: $\pm 15\%$ over a wide temperature range, but consult the manufacturer's data sheets for exact specifications). However, Y5V capacitors typically have extreme temperature tolerance specifications of $+22\%/ -82\%$. Due to the extreme temperature tolerance, a 10 μF nominal rated Y5V type capacitor may not deliver enough total capacitance to meet minimum internal voltage regulator stability and transient response requirements. Therefore, Y5V capacitors are not recommended for use with the internal voltage regulator if the application must operate over a wide temperature range.

In addition to temperature tolerance, the effective capacitance of large value ceramic capacitors can vary substantially, based on the amount of DC voltage applied to the capacitor. This effect can be very significant, but is often overlooked or is not always documented.

A typical DC bias voltage vs. capacitance graph for 16V, 10V and 6.3V rated capacitors is shown in Figure 2-4.

FIGURE 2-4 DC BIAS VOLTAGE vs. CAPACITANCE CHARACTERISTICS



When selecting a ceramic capacitor to be used with the internal voltage regulator, it is suggested to select a high-voltage rating, so that the operating voltage is a small percentage of the maximum rated capacitor voltage. For example, choose a ceramic capacitor rated at 16V for the 1.8V VCAP voltage. Suggested capacitors are shown in Table 2-1.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (6/2010)

Initial release of this document; issued for revision A3. Includes silicon issues 1 (Oscillator – Two-Speed Start-up), 2 (Resets), 3 (Enhanced PMP), 4 (A/D), 5 (Interrupts – INTx), and 6 (Output Compare – Cascaded Mode).

Rev B Document (9/2010)

Revised silicon issue 4 (A/D Converter) to reflect updated definition of issues. Added data sheet clarification issue 1 (Guidelines For Getting Started with 16-Bit Microcontrollers).

Rev C Document (1/2011)

Added silicon issue 7 (USB).

Rev D Document (6/2011)

Added silicon revision A4. Adds existing silicon issues, 1 through 7, from revision A3 without changes. No new data sheet clarifications added. No issues removed.

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NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
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