PIC24FJ256GA110 Family Silicon Errata and Data Sheet Clarification

The PIC24FJ256GA110 family devices that you have received conform functionally to the current Device Data Sheet (DS39905**D**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC24FJ256GA110 family silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A5**).

Data Sheet clarifications and corrections start on page 10, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 2 or PICkit™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 2 programmer/debugger or PICkit™ 3.
2. From the main menu in MPLAB IDE, select *Configure>Select Device*, and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (*Debugger>Select Tool*).
4. Perform a "Connect" operation to the device (*Debugger>Connect*). Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC24FJ256GA110 family silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)	
		A3	A5
PIC24FJ256GA110	101Eh	01h	03h
PIC24FJ192GA110	1016h		
PIC24FJ128GA110	100Eh		
PIC24FJ256GA108	101Ah		
PIC24FF192GA108	1012h		
PIC24FJ128GA108	100Ah		
PIC24FJ256GA106	1018h		
PIC24FJ192GA106	1010h		
PIC24FJ128GA106	1008h		

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".

2: Refer to the *"PIC24FJXXXGA0XX Flash Programming Specification"* (DS39768) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)	
				A3	A5
Core	RAM Operation	1.	RAM issues in Doze mode.	X	X
Core	BOR	2.	BOR issues in enabled on-chip regulator.	X	
JTAG	Device Programming	3.	JTAG issues in device programming.	X	X
UART	—	4.	Framing errors in UART.	X	
I/O	PORTB	5.	RB5 issues in open-drain operation.	X	
SPI	Master mode	6.	Early one-half clock cycles.	X	
CTMU	—	7.	CTMU issues as a trigger source.	X	
UART	UERIF Interrupt	8.	UART error interrupt issue.	X	
UART	FIFO Error Flags	9.	Error bits settings for receive FIFO.	X	
SPI	Enhanced Buffer modes	10.	Errors in enhanced buffer interrupts.	X	
UART	IrDA®	11.	Issues in 8-bit mode using IrDA® endec.	X	
UART	IrDA	12.	Framing errors in 8-bit mode using IrDA endec.	X	
UART	IrDA	13.	Transmission errors in 9-bit mode using IrDA endec.	X	
Core	Instruction Set	14.	Read-After-Write stall conditions inside a REPEAT loop.	X	X
Memory	Program Space Visibility	15.	False error trap conditions when accessing data in the PSV.	X	
ICSP™	—	16.	Inability of the ICSP/ICD port pair to read or program.	X	
RTCC	—	17.	Unexpected decrementing of the Alarm Repeat Counter.	X	
I^2C™ Module	Master mode	18.	Acknowledgement issues in addressing slave device.	X	
I^2C™ Module	Slave mode	19.	Acknowledgement issues in Slave mode.	X	
A/D Converter	—	20.	Debugging issues on 64-pin devices.	X	
SPI	Enhanced Buffer mode	21.	FIFO transfer issues in Enhanced Master mode.	X	
Core	Code Protection	22.	Applications unable to write when General Segment Code Protection has been enabled.	X	
SPI/PPS	—	23.	ALTRP/ASCK1 functionality is not supported.	X	
Oscillator	LPRC	24.	Issues with LPRC automatic restart following BOR.	X	
CTMU	A/D Trigger	25.	Issues in the CTMU in triggering automatic A/D conversion.	X	
Output Compare	—	26.	Single missed compare events under certain conditions.	X	
Interrupts	INTx	27.	External interrupts missed when writing to INTCON2.	X	X
A/D Converter	—	28.	Module continues to draw current when disabled.	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A5**).

1. Module: Core (RAM Operation)

If a RAM read is performed on the instruction immediately prior to enabling Doze mode, an extra read event may occur when Doze mode is enabled. This has no effect on most SFRs and on user RAM space. However, this could cause registers which also perform some action on a read (such as auto-incrementing a pointer or removing data from a FIFO buffer) to repeat that action, possibly resulting in lost data or unexpected operation.

Work around

Avoid reading registers which perform a secondary action (e.g., UART and SPI FIFO buffers, and the RTCVAL registers) immediately prior to entering Doze mode.

If this cannot be avoided, execute a NOP instruction before entering Doze mode.

Affected Silicon Revisions

A3	A5						
X	X						

2. Module: Core (BOR)

When the on-chip regulator is enabled (ENVREG tied to VDD), a BOR event may spontaneously occur under the following circumstances:

- VDD is less than 2.5V, and either:
- the internal band gap reference is being used as a reference with the A/D converter (AD1PCFGH<1> or <0> = 0) or comparators (CMxCON<1:0> = 11); or
- the CTMU module is enabled.

Work around

Limit the following activities to only those times when the on-chip regulator is not in Tracking mode (LVDIF (IFS4<8>) = 0):

- enabling the CTMU module;
- selecting the internal band gap as a reference for the A/D converter or the comparators.

Affected Silicon Revisions

A3	A5						
X							

3. Module: JTAG (Device Programming)

The JTAGEN Configuration bit can be programmed to '0' while using the JTAG interface for device programming. This may cause a situation where JTAG programming can lock itself out of being able to program the device.

Work around

None.

Affected Silicon Revisions

A3	A5						
X	X						

4 Module: UART

When the UART is operating using two Stop bits (STSEL = 1), it may sample the first Stop bit instead of the second one. If the device being communicated with is one using one Stop bit in its communications, this may lead to framing errors.

Work around

None.

Affected Silicon Revisions

A3	A5						
X							

5. Module: I/O (PORTB)

When RB5 is configured as an open-drain output, it remains in a high-impedance state. The settings of LATB5 and TRISB5 have no effect on the pin's state.

Work around

If open-drain operation is not required, configure RB5 as a regular I/O (ODCB<5> = 0).

If open-drain operation is required, there are two options:

- select a different I/O pin for the open-drain function; or
- place an external transistor on the pin, and configure the pin as a regular I/O.

Affected Silicon Revisions

A3	A5						
X							

6. Module: SPI (Master Mode)

In Master mode, both the SPI Interrupt Flag (SPIxIF) and the SPIRBF bit (SPIxSTAT<0>) may become set one-half clock cycle early, instead of on the clock edge. This occurs only under the following circumstances:

- Enhanced Buffer mode is disabled (SPIBEN = 0); and
- the module is configured for serial data output changes on transition from clock active to clock Idle state (CKE = 1)

If the application is using the interrupt flag to determine when data to be transmitted is written to the transmit buffer, the data currently in the buffer may be overwritten.

Work around

Before writing to the SPI buffer, check the SCK pin to determine if the last clock edge has passed. Example 1 (below) demonstrates a method for doing this. In this example, pin RD1 functions as the SPI clock, SCK, which is configured as Idle low.

Affected Silicon Revisions

A3	A5						
X							

7. Module: CTMU

When the CTMU module is selected as the trigger source (SYNCSEL<4:0> = 11000), the input capture and/or output compare trigger may not work.

Work around

Manually trigger the input capture and/or output compare module(s) after a CTMU event is received. Be certain to compensate for any time latency that results from manually triggering the module.

Affected Silicon Revisions

A3	A5						
X							

EXAMPLE 1: CHECKING THE STATE OF SPIxIF AGAINST THE SPI CLOCK

```
while(IFS0bits.SPI1IF == 0){}     //wait for the transmission to complete
while(PORTDbits.RD1 == 1){}       //wait for the last clock to finish
SPI1BUF = 0xFF;                   //write new data to the buffer
```

8. Module: UART (UERIF Interrupt)

The UART error interrupt may not occur, or occur at an incorrect time, if multiple errors occur during a short period of time.

Work around

Read the error flags in the UxSTA register whenever a byte is received to verify the error status. In most cases, these bits will be correct, even if the UART error interrupt fails to occur. For possible exceptions, refer to Errata # 9.

Affected Silicon Revisions

A3	A5						
X							

9. Module: UART (FIFO Error Flags)

Under certain circumstances, the PERR and FERR error bits may not be correct for all bytes in the receive FIFO. This has only been observed when both of the following conditions are met:

- the UART receive interrupt is set to occur when the FIFO is full or ¾ full (UxSTA<7:6> = 1x), and
- more than 2 bytes with an error are received.

In these cases, only the first two bytes with a parity or framing error will have the corresponding bits indicate correctly. The error bits will not be set after this.

Work around

None.

Affected Silicon Revisions

A3	A5						
X							

10. Module: SPI (Enhanced Buffer Modes)

If the SPI event interrupt is configured to occur when the enhanced FIFO buffer is full (SISEL<2:0> = 111), the interrupt may actually occur when the 7th byte is written to the buffer, instead of the 8th byte. The other enhanced buffer interrupts function as previously described.

Work around

Do not use the Full Buffer Interrupt mode. The SPITBF bit (SPIxSTAT<1>) reliably indicates when the enhanced FIFO buffer is full, and can be polled instead of using the Full Buffer Interrupt mode.

Affected Silicon Revisions

A3	A5						
X							

11. Module: UART (IrDA®)

When the UART is operating in 8-bit mode (PDSEL<1:0> = 0x) and using the IrDA endec (IREN = 1), the module incorrectly transmits a data payload of 80h as 00h.

Work around:

None.

Affected Silicon Revisions

A3	A5						
X							

12. Module: UART (IrDA)

When the UART is operating in 8-bit mode (PDSEL<1:0> = 0x) and using the IrDA endec (IREN = 1), a framing error may occur when transmitting a data payload of 00h.

Work around:

None.

Affected Silicon Revisions

A3	A5						
X							

13. Module: UART (IrDA)

When the UART is operating in 9-bit mode (PDSEL<1:0> = 1x) and using the IrDA endec (IREN = 1), the module will incorrectly transmit 10 bits when transmitting data payloads of 00h or 80h.

Work around:

None.

Affected Silicon Revisions

A3	A5						
X							

14. Module: Core (Instruction Set)

If an instruction producing a read-after-write stall condition is executed inside a REPEAT loop, the instruction will be executed fewer times than was intended. For example, this loop:

```
repeat #0xf
inc [w1],[++w1]
```

will execute less than 15 times.

Work around

Avoid using REPEAT to repetitively execute instructions that create a stall condition. Instead, use a software loop using conditional branches. The MPLAB® C Compiler will not generate REPEAT loops that cause this erratum.

Affected Silicon Revisions

A3	A5						
X	X						

15. Module: Memory (Program Space Visibility)

When accessing data in the PSV area of data RAM, it is possible to generate a false address error trap condition by reading data located precisely at the lower address boundary (8000h). If data is read using an instruction with an auto-decrement, the resulting RAM address will be below the PSV boundary (i.e., at 7FFEh); this will result in an address error trap.

This false address error can also occur if a 32-bit MOV instruction is used to read the data at location 8000h.

Work around

Do not use the first location of a PSV page (address 8000h). The MPLAB® C Compiler (v3.11 or later) supports the option "-merrata=psv_trap" to prevent it from generating code that would cause this erratum.

Affected Silicon Revisions

A3	A5						
X							

16. Module: ICSP™

The ICSP/ICD port pair, PGEC3/PGED3 (RB5/RB4), cannot be used to read or program the device.

Work around

Use either PGEC2/PGED2 or PGEC1/PGED1.

Affected Silicon Revisions

A3	A5						
X							

17. Module: RTCC

Under certain circumstances, the value of the Alarm Repeat Counter (ALCFGRPT<7:0>) may be unexpectedly decremented. This happens only when a byte write to the upper byte of ALCFGRPT is performed in the interval between a device POR/BOR and the first edge from the RTCC clock source.

Work around

Do not perform byte writes on ALCFGRPT, particularly the upper byte.

Alternatively, wait until one period of the SOSC has completed before performing byte writes to ALCFGRPT.

Affected Silicon Revisions

A3	A5						
X							

18. Module: I²C™ Module (Master Mode)

Under certain circumstances, a module operating in Master mode may Acknowledge its own command addressed to a slave device. This happens when the following occurs:

- 10-Bit Addressing mode is used (A10M = 1), and:
- the I²C master has the same two upper address bits (I2CADD<9:8>) as the addressed slave module.

In these cases, the master also Acknowledges the address command and generates an erroneous I²C slave interrupt, as well as the I²C master interrupt.

Work around

Several options are available:

- When using 10-Bit Addressing mode, make certain that the master and slave devices do not share the same 2 MSBs of their addresses.

If this cannot be avoided:

- Clear the A10M bit (I2CxCON<10> = 0) prior to performing a Master mode transmit.
- Read the ADD10 bit (I2CxSTAT<8>) to check for a full 10-bit match whenever a slave I²C interrupt occurs on the master module.

Affected Silicon Revisions

A3	A5						
X							

19. Module: I²C Module (Slave Mode)

Under certain circumstances, a module operating in Slave mode may not respond correctly to some of the special addresses reserved by the I²C protocol. This happens when the following occurs:

- 10-Bit Addressing mode is used (A10M = 1), and
- bits, A<7:1>, of the Slave address (I2CADD<7:1>) fall into the range of the reserved 7-bit address ranges, '1111xxx' or '0000xxx'.

In these cases, the Slave module Acknowledges the command and triggers an I²C slave interrupt; it does not copy the data into the I2CxRCV register or set the RBF bit.

Work around

Do not set bits, A<7:1>, of the module's slave address equal to '1111xxx' or '0000xxx'.

Affected Silicon Revisions

A3	A5						
X							

20. Module: A/D Converter

When using PGEC1 and PGED1 to debug an application on any 64-pin devices in this family, all voltage references will be disabled. This includes VREF+, VREF-, AVDD and AVSS. Any A/D conversion will always equal 3FFh.

Note: This issue applies only to 64-pin devices in this family (PIC24FJ256GA106, PIC24FJ192GA106 and PIC24FJ128GA106).

Work around

Use PGEC2 and PGED2 to debug any A/D functionality.

Affected Silicon Revisions

A3	A5						
X							

21. Module: SPI (Enhanced Buffer Mode)

In Enhanced Master mode, the SRMPT bit (SPIxSTAT<7>) may erroneously become set for several clock cycles in the middle of a FIFO transfer, indicating that the shift register is empty when it is not. This happens when both SPI clock prescalers are set to values other than their maximum (SPIxCON<4:2> ≠ 000 and SPIxCON<1:0> ≠ 00).

Work around

Configure the module to generate an SPI event interrupt whenever the last bit is shifted out of the shift register (SPIxSTAT<4:2> = 101). When the SPIxIF flag becomes set, the shift register is empty.

Affected Silicon Revisions

A3	A5						
X							

22. Module: Core (Code Protection)

When General Segment Code Protection has been enabled (GCP Configuration bit is programmed), applications are unable to write to the first 512 bytes of the program memory space (0000h through 0200h). In applications that may require the interrupt vectors to be changed during run time, such as bootloaders, modifications to the interrupt vector tables will not be possible.

Work around

Create two new interrupt vector tables, one each for the IVT and AIVT, in an area of program space beyond the affected region. Map the addresses in the old vector tables to the new tables. These new tables can then be modified as needed to the actual addresses of the ISRs.

Affected Silicon Revisions

A3	A5						
X							

23. Module: SPI/PPS

The ALTRP/ASCK1 functionality is not supported by the A3 revision of this part family.

Work around

None.

Affected Silicon Revisions

A3	A5						
X							

24. Module: Oscillator (LPRC)

The LPRC may not automatically restart following BOR events (i.e., when supply voltage sags to between the BOR and POR thresholds, then returns to above the BOR level). When this happens, systems that use the LPRC clock may not work. This includes the PLL, Two-Speed Start-up, Fail-Safe Clock Monitor and the WDT.

Work around

For PLL issues: Select a non-PLL Clock mode as the initial start-up mode, using the FNOSC Configuration bits (CW2<10:8>). After the application has initialized, switch to a PLL Clock mode in software using the NOSC bits (OSCCON<10:8>). Allow 10 microseconds to elapse between application start-up and a software clock switch.

For WDT issues: Disable the WDT by programming the FWDTEN bit (CW1<7>). After the application has initialized, enable the WDT in software by setting the SWDTEN bit (RCON<5>). Allow 10 microseconds to elapse between application start-up and setting SWDTEN.

Affected Silicon Revisions

A3	A5						
X							

25. Module: CTMU (A/D Trigger)

The CTMU may not trigger an automatic A/D conversion after the current source is turned off. This happens even when the A/D trigger control bit, CTTRIG (CTMUCON<8>), has been set.

Work around

Perform a manual A/D conversion by clearing the SAMP bit (AD1CON1<1>) immediately after the CTMU current source has been stopped.

Affected Silicon Revisions

A3	A5						
X							

26. Module: Output Compare

In PWM mode, the output compare module may miss a compare event when the current duty cycle register (OCxRS) value is 0000h (0% duty cycle) and the OCxRS register is updated with a value of 0001h. The compare event is only missed the first time a value of 0001h is written to OCxRS and the PWM output remains low for one PWM period. Subsequent PWM high and low times occur as expected.

Work around

If the current OCxRS register value is 0000h, avoid writing a value of 0001h to OCxRS. Instead, write a value of 0002h. In this case, however, the duty cycle will be slightly different from the desired value.

Affected Silicon Revisions

A3	A5						
X							

27. Module: Interrupts (INTx)

Writing to the INTCON2 register may cause an external interrupt event (inputs on INT0 through INT4) to be missed. This only happens when the interrupt event and the write event occur during the same clock cycle.

Work around

If possible, do not write to INTCON2 while any of the external interrupts are enabled.

If this cannot be avoided, write the data intended for INTCON2 to any other register in the interrupt block of the SFR (addresses, 0080h to 00E0h); then write the data to INTCON2.

Be certain to write the data to a register not being actively used by the application, or to any of the interrupt flag registers, in order to avoid spurious interrupts. For example, if the interrupts controlled by IEC5 are not being used in the application, the code sequence would be:

```
IEC5 = 0x1E;
INTCON2 = 0x1E;
IEC5 = 0;
```

It is the user's responsibility to determine an appropriate register for the particular application.

Affected Silicon Revisions

A3	A5						
X	X						

28. Module: A/D Converter

Once the A/D module is enabled (AD1CON1<15> = 1), it may continue to draw extra current even if the module is later disabled (AD1CON1<15> = 0).

Work around

In addition to disabling the module through the ADON bit, set the corresponding PMD bit (ADC1MD, PMD1<0>) to power it down completely.

Disabling the A/D module through the PMD register also disables the AD1PCFG registers, which in turn, affects the state of any port pins with analog inputs. Users should consider the effect on I/O ports and other digital peripherals on those ports when ADC1MD is used for power conservation.

Affected Silicon Revisions

A3	A5						
X	X						

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS39905**D**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Guidelines for Getting Started with 16-Bit Microcontrollers

Section 2.4 Voltage Regulator Pins (ENVREG/DISVREG and VCAP/VDDCORE) has been replaced with a new and more detailed section. The entire text follows:

2.4 Voltage Regulator Pins Voltage Regulator Pins (ENVREG/DISVREG and VCAP/VDDCORE)

Note:	This section applies only to PIC24FJ devices with an on-chip voltage regulator.

The on-chip voltage regulator enable/disable pin (ENVREG or DISVREG, depending on the device family) must always be connected directly to either a supply voltage or to ground. The particular connection is determined by whether or not the regulator is to be used:

- For ENVREG, tie to VDD to enable the regulator, or to ground to disable the regulator
- For DISVREG, tie to ground to enable the regulator or to VDD to disable the regulator

Refer to **Section 25.2 "On-Chip Voltage Regulator"** for details on connecting and using the on-chip regulator.

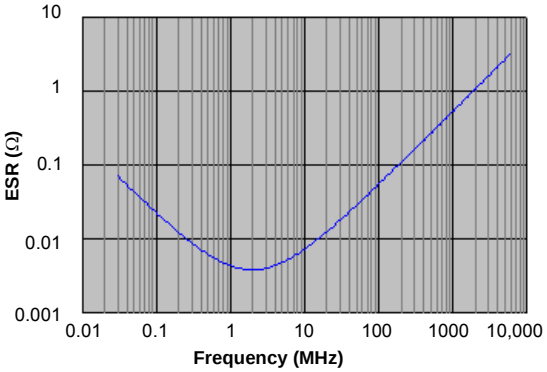
When the regulator is enabled, a low-ESR (< 5Ω) capacitor is required on the VCAP/VDDCORE pin to stabilize the voltage regulator output voltage. The VCAP/VDDCORE pin must not be connected to VDD and must use a capacitor of 10 µF connected to ground. The type can be ceramic or tantalum. Suitable examples of capacitors are shown in Table 2-1. Capacitors with equivalent specifications can be used.

Designers may use Figure 2-3 to evaluate ESR equivalence of candidate devices.

The placement of this capacitor should be close to VCAP/VDDCORE. It is recommended that the trace length not exceed 0.25 inch (6 mm). Refer to **Section 28.0 "Electrical Characteristics"** for additional information.

When the regulator is disabled, the VCAP/VDDCORE pin must be tied to a voltage supply at the VDDCORE level. Refer to **Section 28.0 "Electrical Characteristics"** for information on VDD and VDDCORE.

FIGURE 2-3 FREQUENCY vs. ESR PERFORMANCE FOR SUGGESTED VCAP



Note: Typical data measurement at 25°C, 0V DC bias.

TABLE 2-1 SUITABLE CAPACITOR EQUIVALENTS

Make	Part #	Nominal Capacitance	Base Tolerance	Rated Voltage	Temp. Range
TDK	C3216X7R1C106K	10 µF	±10%	16V	-55 to 125ºC
TDK	C3216X5R1C106K	10 µF	±10%	16V	-55 to 85ºC
Panasonic	ECJ-3YX1C106K	10 µF	±10%	16V	-55 to 125ºC
Panasonic	ECJ-4YB1C106K	10 µF	±10%	16V	-55 to 85ºC
Murata	GRM32DR71C106KA01L	10 µF	±10%	16V	-55 to 125ºC
Murata	GRM31CR61C106KC31L	10 µF	±10%	16V	-55 to 85ºC

2.4.1 CONSIDERATIONS FOR CERAMIC CAPACITORS

In recent years, large value, low-voltage, surface mount ceramic capacitors have become very cost effective in sizes up to a few tens of microfarad. The low-ESR, small physical size and other properties make ceramic capacitors very attractive in many types of applications.

Ceramic capacitors are suitable for use with the internal voltage regulator of this microcontroller. However, some care is needed in selecting the capacitor to ensure that it maintains sufficient capacitance over the intended operating range of the application.

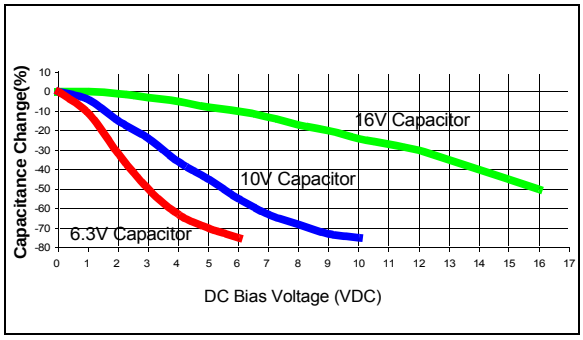
Typical low-cost, 10 µF ceramic capacitors are available in X5R, X7R and Y5V dielectric ratings (other types are also available, but are less common). The initial tolerance specifications for these types of capacitors are often specified as ±10% to ±20% (X5R and X7R), or -20%/+80% (Y5V). However, the effective capacitance that these capacitors provide in an application circuit will also vary based on additional factors, such as the applied DC bias voltage and the temperature. The total in-circuit tolerance is, therefore, much wider than the initial tolerance specification.

The X5R and X7R capacitors typically exhibit satisfactory temperature stability (ex: ±15% over a wide temperature range, but consult the manufacturer's data sheets for exact specifications). However, Y5V capacitors typically have extreme temperature tolerance specifications of +22%/-82%. Due to the extreme temperature tolerance, a 10 µF nominal rated Y5V type capacitor may not deliver enough total capacitance to meet minimum internal voltage regulator stability and transient response requirements. Therefore, Y5V capacitors are not recommended for use with the internal regulator if the application must operate over a wide temperature range.

In addition to temperature tolerance, the effective capacitance of large value ceramic capacitors can vary substantially, based on the amount of DC voltage applied to the capacitor. This effect can be very significant, but is often overlooked or is not always documented.

A typical DC bias voltage vs. capacitance graph for 16V, 10V and 6.3V rated capacitors is shown in Figure 2-4.

FIGURE 2-4 DC BIAS VOLTAGE vs. CAPACITANCE CHARACTERISTICS



When selecting a ceramic capacitor to be used with the internal voltage regulator, it is suggested to select a high-voltage rating, so that the operating voltage is a small percentage of the maximum rated capacitor voltage. For example, choose a ceramic capacitor rated at 16V for the 2.5V core voltage. Suggested capacitors are shown in Table 2-1.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (2/2008)

First revision of this document. Includes silicon issues 1 (Core, RAM Operation), 2 (Core, BOR), 3 (JTAG, Programming), 4 (UART), 5 (I/O, PORTB), 6 (SPI) and 7 (Input Capture).

Rev B Document (4/2008)

Revised silicon issues 7 to clarify the requirement for latency compensation. Added silicon issues 8 (UART – UERIF Interrupt), 9 (UART – FIFO Error Flags) and 10 (SPI – Enhanced Buffer Modes).

Rev C Document (7/2008)

Revised silicon issues 4 (UART) and 6 (SPI, Master Mode) to reflect updated definition of issues. Added silicon issues 11 through 13 (UART, IrDA), 14 (Core, Instruction Set), 15 (Memory, Program Space Visibility), 16 (ICSP), 17 (RTCC), 18 (I^2C, Master Mode), 19 (I^2C Module (Slave Mode) and 20 (A/D Converter).

Rev D Document (10/2008)

Added silicon issue 21 (SPI – Enhanced Buffer Mode).

Rev E Document (04/2009)

Added silicon issue 22 (Core – Code Protection), 23 (SPI/PPS), 24 (Oscillator – LPRC) and 25 (CTMU – A/D Trigger).

Rev F Document (07/2009)

Added silicon revision A5 to document. Includes existing silicon issues 1 (Core, RAM Operation), 3 (JTAG, Programming), 8 (UART – UERIF Interrupt) and 14 (Core – Instruction Set). No additional new issues added.

Rev G Document (06/2010)

Added silicon issues 26 (Output Compare) and 27 (Interrupts – INTx) to silicon revisions A3 and A5.

Rev H Document (07/2010)

Added silicon issue 28 (A/D Converter) to silicon revisions A3 and A5.

Rev J Document (09/2010)

Revised silicon issue 28 (A/D Converter) to reflect updated definition of issues. Added data sheet clarification issue 1 (Guidelines For Getting Started with 16-Bit Microcontrollers).

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