

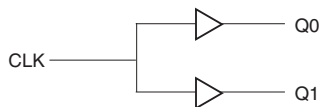
## GENERAL DESCRIPTION

The 8302 is a low skew, 1-to-2 LVCMOS/LVTTTL Fanout Buffer. The 8302 has a single ended clock input. The single ended clock input accepts LVCMOS or LVTTTL input levels. The 8302 features a pair of LVCMOS/LVTTTL outputs. The 8302 is characterized at full 3.3V for input  $V_{DD}$ , and mixed 3.3V and 2.5V for output operating supply modes ( $V_{DDO}$ ). Guaranteed output and part-to-part skew characteristics make the 8302 ideal for clock distribution applications demanding well defined performance and repeatability.

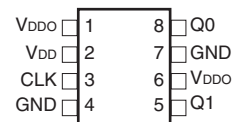
## FEATURES

- 2 LVCMOS / LVTTTL outputs
- LVCMOS / LVTTTL clock input accepts LVCMOS or LVTTTL input levels
- Maximum output frequency: 200MHz
- Output skew: 25ps (typical)
- Part-to-part skew: 250ps (typical)
- Small 8 lead SOIC package saves board space
- Full 3.3V or 3.3V core, 2.5V supply modes
- 0°C to 70°C ambient operating temperature
- Lead-Free package fully RoHS compliant

## BLOCK DIAGRAM



## PIN ASSIGNMENT



**8302**  
**8-Lead SOIC**  
 3.8mm x 4.8mm, x 1.47mm package body  
**M Package**  
 Top View

**TABLE 1. PIN DESCRIPTIONS**

Number	Name	Type		Description
1, 6	V <sub>DDO</sub>	Power		Output supply pins.
2	V <sub>DD</sub>	Power		Core supply pin.
3	CLK	Input	Pulldown	LVC MOS / LV TTL clock input.
4,7	GND	Power		Power supply ground.
5	Q1	Output		Single clock output. LVC MOS / LV TTL interface levels.
8	Q0	Output		Single clock output. LVC MOS / LV TTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**TABLE 2. PIN CHARACTERISTICS**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
C <sub>PD</sub>	Power Dissipation Capacitance (per output)	V <sub>DD</sub> , V <sub>DDO</sub> = 3.465V		22		pF
		V <sub>DD</sub> = 3.465V, V <sub>DDO</sub> = 2.625V		16		pF
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			51		kΩ
R <sub>OUT</sub>	Output Impedance		5	7	12	Ω

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage, $V_{DD}$	4.6V
Inputs, $V_I$	-0.5V to $V_{DD} + 0.5V$
Outputs, $V_O$	-0.5V to $V_{DDO} + 0.5V$
Package Thermal Impedance, $\theta_{JA}$	112.7°C/W (0 lfpm)
Storage Temperature, $T_{STG}$	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 3A. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Core Supply Voltage		3.135	3.3	3.465	V
$V_{DDO}$	Output Power Supply Voltage		3.135	3.3	3.465	V
$I_{DD}$	Power Supply Current				13	mA
$I_{DDO}$	Output Supply Current				4	mA

**TABLE 3B. LVCMOS / LVTTTL DC CHARACTERISTICS,  $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage		2		$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage		-0.3		0.8	V
$I_{IH}$	Input High Current	CLK $V_{DD} = V_{IN} = 3.465V$			150	$\mu A$
$I_{IL}$	Input Low Current	CLK $V_{DD} = 3.465V, V_{IN} = 0V$	-5			$\mu A$
$V_{OH}$	Output High Voltage	$50\Omega$ to $V_{DDO}/2$	2.6			V
		$I_{OH} = -100\mu A$	2.9			V
$V_{OL}$	Output Low Voltage	$50\Omega$ to $V_{DDO}/2$			0.5	V
		$I_{OL} = 100\mu A$			0.2	V

**TABLE 4A. AC CHARACTERISTICS,  $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Output Frequency				200	MHz
$t_{pLH}$	Propagation Delay, Low-to-High; NOTE 1	$f \leq 200MHz$	1.9	2.35	2.8	ns
$t_{sk(o)}$	Output Skew; NOTE 2, 4			25	85	ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 3, 4			250	800	ps
$t_R$	Output Rise Time	20% to 80%	300		800	ps
$t_F$	Output Fall Time	20% to 80%	300		800	ps
odc	Output Duty Cycle	$f \leq 133MHz$	45		55	%
		$133MHz < f \leq 200MHz$	40		60	%

Parameters measured at  $f_{MAX}$  unless otherwise noted.

NOTE 1: Measured from  $V_{DD}/2$  of the input to  $V_{DDO}/2$  of the output.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at  $V_{DDO}/2$ .

NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at  $V_{DDO}/2$ .

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

**TABLE 3C. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Core Supply Voltage		3.135	3.3	3.465	V
$V_{DDO}$	Output Supply Voltage		2.375	2.5	2.625	V
$I_{DD}$	Power Supply Current				13	mA
$I_{DDO}$	Output Supply Current				4	mA

**TABLE 3D. LVCMOS / LVTTTL DC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage		2		$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage		-0.3		0.8	V
$I_{IH}$	Input High Current	CLK $V_{DD} = V_{IN} = 3.465V$			150	$\mu A$
$I_{IL}$	Input Low Current	CLK $V_{DD} = 3.465V, V_{IN} = 0V$	-5			$\mu A$
$V_{OH}$	Output High Voltage	$50\Omega$ to $V_{DDO}/2$	1.8			V
		$I_{OH} = -100\mu A$	2.2			V
$V_{OL}$	Output Low Voltage	$50\Omega$ to $V_{DDO}/2$			0.5	V
		$I_{OL} = 100\mu A$			0.2	V

**TABLE 4B. AC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Output Frequency				200	MHz
$tp_{LH}$	Propagation Delay, Low-to-High; NOTE 1	$f \leq 200MHz$	2.3		3.3	ns
$tsk(o)$	Output Skew; NOTE 2, 4				85	ps
$tsk(pp)$	Part-to-Part Skew; NOTE 3, 4			250	800	ps
$t_R$	Output Rise Time	20% to 80%	250		650	ps
$t_F$	Output Fall Time	20% to 80%	250		650	ps
odc	Output Duty Cycle	$f \leq 133MHz$	45		55	%
		$133MHz < f \leq 200MHz$	40		60	%

Parameters measured at  $f_{MAX}$  unless otherwise noted.

NOTE 1: Measured from  $V_{DD}/2$  of the input to  $V_{DDO}/2$  of the output.

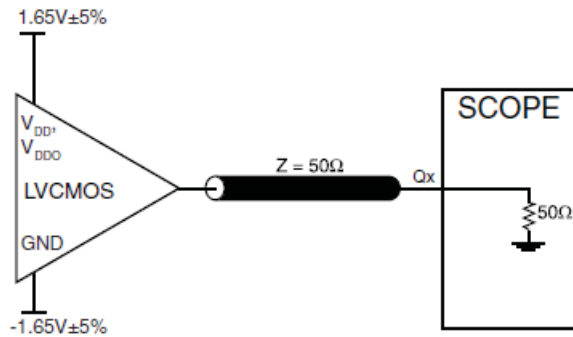
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.

Measured at  $V_{DDO}/2$ .

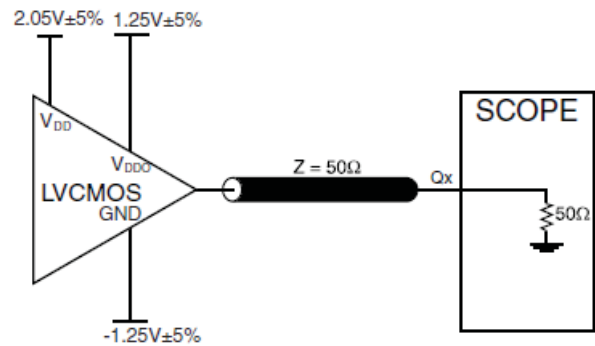
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at  $V_{DDO}/2$ .

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

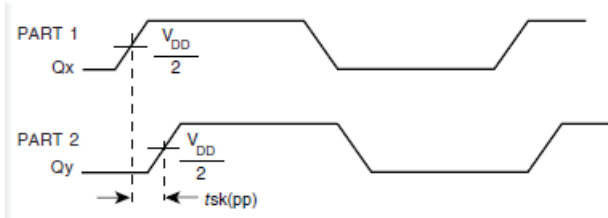
## PARAMETER MEASUREMENT INFORMATION



3.3V OUTPUT LOAD AC TEST CIRCUIT



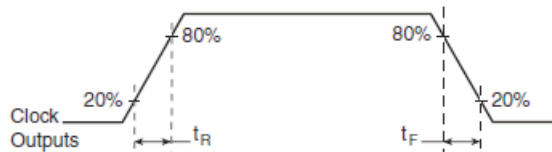
3.3V/2.5V OUTPUT LOAD AC TEST CIRCUIT



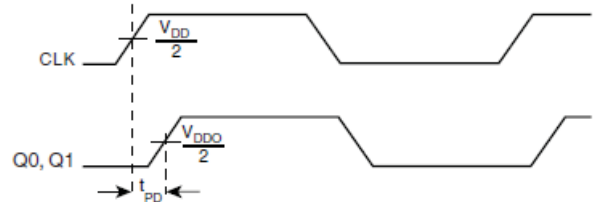
PART-TO-PART SKEW



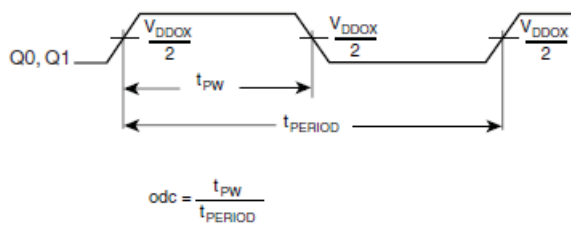
OUTPUT SKEW



OUTPUT RISE/FALL TIME



PROPAGATION DELAY



OUTPUT PULSE WIDTH/PERIOD

## RELIABILITY INFORMATION

TABLE 5.  $\theta_{JA}$  VS. AIR FLOW TABLE FOR 8 LEAD SOIC

$\theta_{JA}$ by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	153.3°C/W	128.5°C/W	115.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	112.7°C/W	103.3°C/W	97.1°C/W

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

### TRANSISTOR COUNT

The transistor count for 8302 is: 322

PACKAGE OUTLINE - SUFFIX M FOR 8 LEAD SOIC

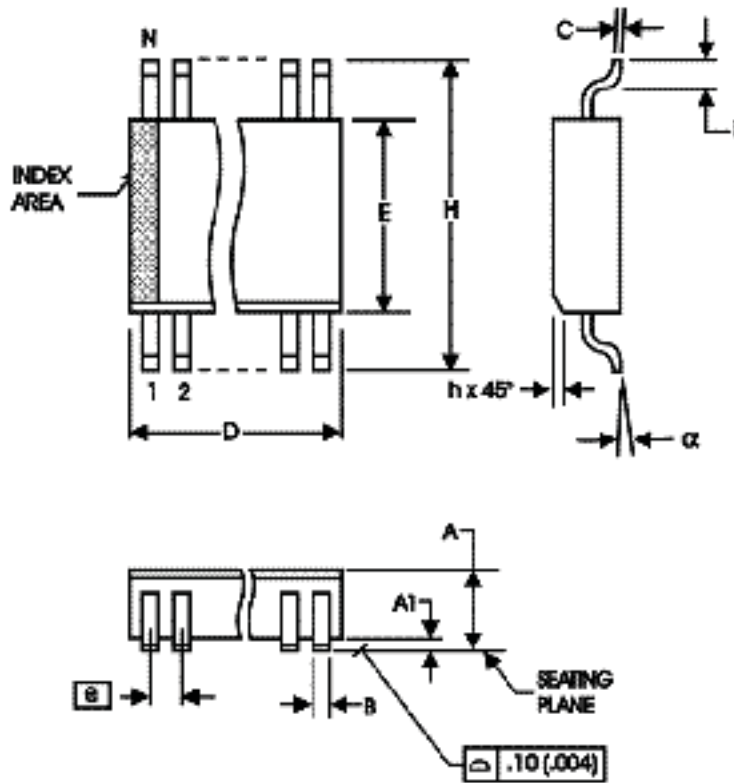


TABLE 6. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	MINIMUM	MAXIMUM
N	8	
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BASIC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
alpha	0°	8°

Reference Document: JEDEC Publication 95, MS-012

**TABLE 7. ORDERING INFORMATION**

<b>Part/Order Number</b>	<b>Marking</b>	<b>Package</b>	<b>Shipping Packaging</b>	<b>Temperature</b>
8302AMLF	8302AMLF	8 lead "Lead Free" SOIC	tube	0°C to 70°C
8302AMLFT	8302AMLF	8 lead "Lead Free" SOIC	tape & reel	0°C to 70°C



REVISION HISTORY SHEET				
Rev	Table	Page	Description of Change	Date
B	T1	2	Pin Description table, revised $V_{DD}$ description.	2/4/03
	T2	2	Pin Characteristics table, deleted $R_{PULLUP}$ row.	
	T3A & T3C	3, 4	Power Supply table, changed $V_{DD}$ parameter to correspond with description.	
	T4A & T4B	3, 4	AC Characteristics tables - added note "Parameters measured at $f_{MAX}$ unless otherwise noted." $t_{p_{LH}}$ Test Conditions, added $f \leq 200\text{MHz}$ .	
C	T2	2	Pin Characteristics table - changed $C_{IN}$ 4pF max. to 4pF typical. Added 5 $\Omega$ min. and 12 $\Omega$ max. to $R_{OUT}$ row.	6/15/04
	T7	8	Ordering Information table - added "Lead-Free" part number.	
D	T3B & T3D	3, 4	LVC MOS DC Characteristics Table - changed $V_{IL}$ max. from 1.3V to 0.8V.	5/17/05
	T7	8	Ordering Information Table - added Lead-Free note.	
D	T7	8	Updated datasheet's header/footer with IDT from ICS.	7/30/10
		10	Removed ICS prefix from Part/Order Number column. Added Contact Page.	
D	T7	8	Ordering Information - removed leaded devices. Updated data sheet format.	11/19/15
D			Updated header and footer.	3/4/16



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### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

### Contact Information

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