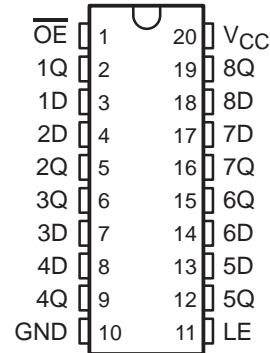


SN54HCT373, SN74HCT373 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCLS009D – MARCH 1984 – REVISED AUGUST 2003

- Operating Voltage Range of 4.5 V to 5.5 V
- High-Current 3-State True Outputs Can Drive Up To 15 LSTTL Loads
- Low Power Consumption, 80- μ A Max I_{CC}
- Typical $t_{pd} = 21$ ns
- ± 6 -mA Output Drive at 5 V
- Low Input Current of 1 μ A Max
- Inputs Are TTL-Voltage Compatible
- Eight High-Current Latches in a Single Package
- Full Parallel Access for Loading

SN54HCT373 . . . J OR W PACKAGE
SN74HCT373 . . . DB, DW, N, NS, OR PW PACKAGE
(TOP VIEW)

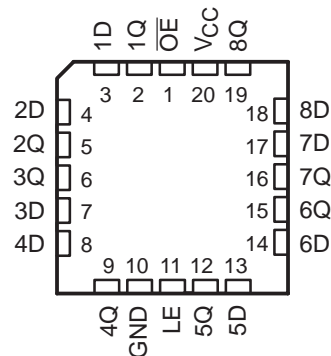


description/ordering information

These 8-bit latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'HCT373 devices are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels that were set up at the D inputs.

SN54HCT373 . . . FK PACKAGE
(TOP VIEW)



ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube of 20	SN74HCT373N	SN74HCT373N
	SOIC – DW	Tube of 25	SN74HCT373DW	HCT373
		Reel of 2000	SN74HCT373DWR	
	SOP – NS	Reel of 2000	SN74HCT373NSR	HCT373
	SSOP – DB	Reel of 2000	SN74HCT373DBR	HT373
	TSSOP – PW	Tube of 70	SN74HCT373PW	HT373
Reel of 2000		SN74HCT373PWR		
Reel of 250		SN74HCT373PWT		
-55°C to 125°C	CDIP – J	Tube of 20	SNJ54HCT373J	SNJ54HCT373J
	CFP – W	Tube of 85	SNJ54HCT373W	SNJ54HCT373W
	LCCC – FK	Tube of 55	SNJ54HCT373FK	SNJ54HCT373FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2003, Texas Instruments Incorporated
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54HCT373, SN74HCT373 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCLS009D – MARCH 1984 – REVISED AUGUST 2003

description/ordering information (continued)

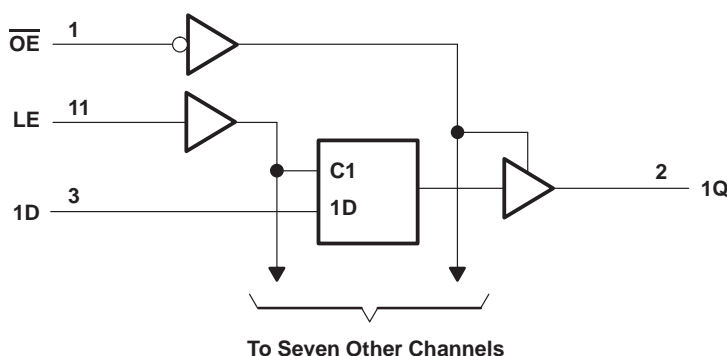
An output-enable (\overline{OE}) input places the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

\overline{OE} does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

FUNCTION TABLE
(each latch)

INPUTS			OUTPUT
\overline{OE}	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±35 mA
Continuous current through V_{CC} or GND	±70 mA
Package thermal impedance, θ_{JA} (see Note 2):	
DB package	70°C/W
DW package	58°C/W
N package	69°C/W
NS package	60°C/W
PW package	83°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

SN54HCT373, SN74HCT373 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCLS009D – MARCH 1984 – REVISED AUGUST 2003

recommended operating conditions (see Note 3)

		SN54HCT373			SN74HCT373			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 4.5 V to 5.5 V		2	2			V
V _{IL}	Low-level input voltage	V _{CC} = 4.5 V to 5.5 V		0.8			0.8	V
V _I	Input voltage	0	V _{CC}		0	V _{CC}		V
V _O	Output voltage	0	V _{CC}		0	V _{CC}		V
Δt/Δv	Input transition rise/fall time	500			500			ns
T _A	Operating free-air temperature	-55	125		-40	85		°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54HCT373		SN74HCT373		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	V _I = V _{IH} or V _{IL}	4.5 V	I _{OH} = -20 μA		4.4	4.499	4.4	4.4	V	
			I _{OH} = -6 mA		3.98	4.3	3.7	3.84		
V _{OL}	V _I = V _{IH} or V _{IL}	4.5 V	I _{OL} = 20 μA		0.001		0.1	0.1	V	
			I _{OL} = 6 mA		0.17	0.26	0.4	0.33		
I _I	V _I = V _{CC} or 0	5.5 V	±0.1	±100	±1000		±1000		nA	
I _{OZ}	V _O = V _{CC} or 0	5.5 V	±0.01	±0.5	±10		±5		μA	
I _{CC}	V _I = V _{CC} or 0, I _O = 0	5.5 V	8		160		80		μA	
ΔI _{CC} [†]	One input at 0.5 V or 2.4 V, Other inputs at 0 or V _{CC}	5.5 V	1.4	2.4	3		2.9		mA	
C _i		4.5 V to 5.5 V	3	10	10		10		pF	

[†] This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V _{CC}	T _A = 25°C		SN54HCT373		SN74HCT373		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration, LE high	4.5 V	20		30		25		ns
		5.5 V	17		27		23		
t _{su}	Setup time, data before LE↓	4.5 V	10		15		13		ns
		5.5 V	9		14		12		
t _h	Hold time, data after LE↓	4.5 V	10		10		10		ns
		5.5 V	10		10		10		



SN54HCT373, SN74HCT373
OCTAL TRANSPARENT D-TYPE LATCHES
WITH 3-STATE OUTPUTS

SCLS009D – MARCH 1984 – REVISED AUGUST 2003

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HCT373		SN74HCT373		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	Q	4.5 V	25	35	53	44	ns			
			5.5 V	21	32	48	40				
	LE	Any Q	4.5 V	28	35	53	44				
			5.5 V	25	32	48	40				
t_{en}	\overline{OE}	Any Q	4.5 V	26	35	53	44	ns			
			5.5 V	23	32	48	40				
t_{dis}	\overline{OE}	Any Q	4.5 V	23	35	53	44	ns			
			5.5 V	22	32	48	40				
t_t		Any Q	4.5 V	10	12	18	15	ns			
			5.5 V	9	11	16	14				

switching characteristics over recommended operating free-air temperature range, $C_L = 150 \text{ pF}$ (unless otherwise noted) (see Figure 1)

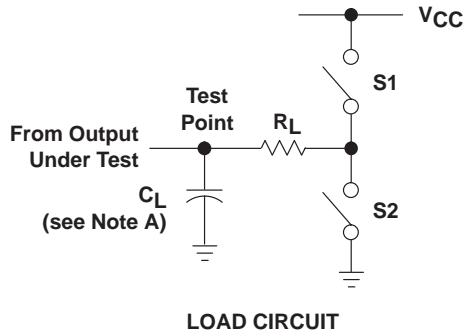
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HCT373		SN74HCT373		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	Q	4.5 V	32	52	79	65	ns			
			5.5 V	27	47	71	59				
	LE	Any Q	4.5 V	38	52	79	65				
			5.5 V	36	47	71	59				
t_{en}	\overline{OE}	Any Q	4.5 V	33	52	79	65	ns			
			5.5 V	28	47	71	59				
t_t		Any Q	4.5 V	18	42	63	53	ns			
			5.5 V	16	38	57	48				

operating characteristics, $T_A = 25^\circ\text{C}$

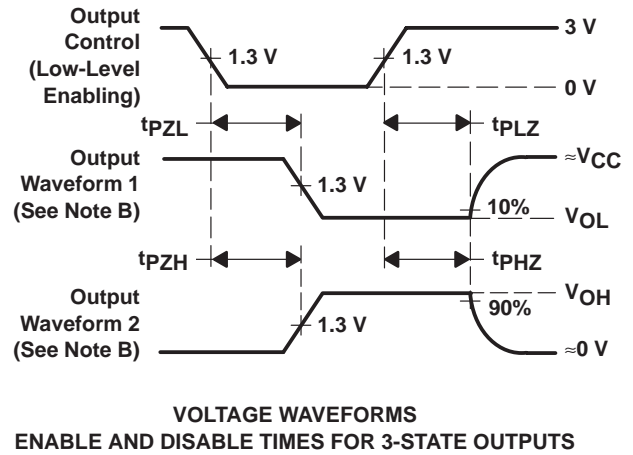
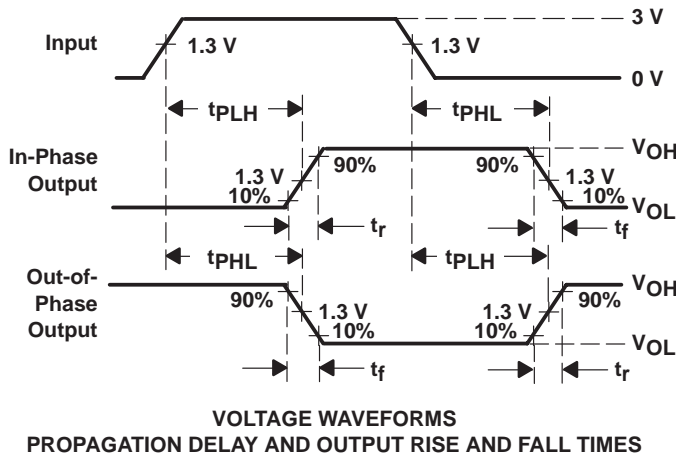
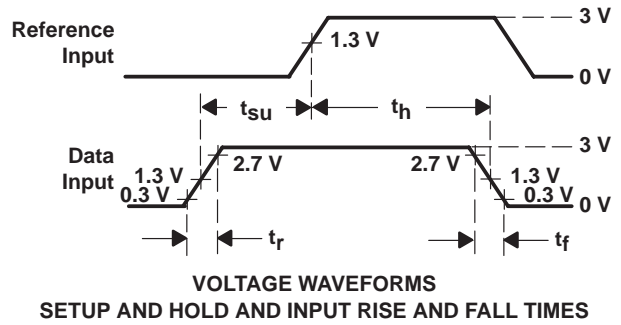
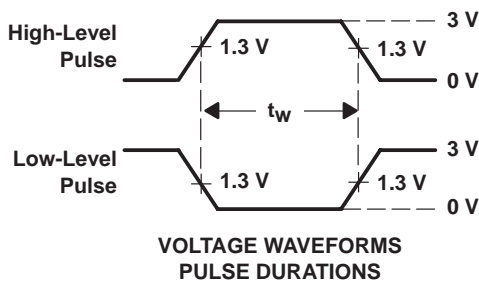
PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance per latch	No load	50	pF



PARAMETER MEASUREMENT INFORMATION



PARAMETER	R_L	C_L	S1	S2	
t_{en}	t_{PZH}	1 k Ω	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 k Ω	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t	—	50 pF or 150 pF	Open	Open	



- NOTES: A. C_L includes probe and test-fixture capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
 D. The outputs are measured one at a time with one input transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-86867012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-8686701RA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type
5962-8686701VRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type
5962-8686701VSA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type
JM38510/65453BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type
JM38510/65453BSA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type
SN54HCT373J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type
SN74HCT373DBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT373DBRE4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT373DBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT373DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT373DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT373DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT373DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT373DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT373DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT373N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74HCT373N3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI
SN74HCT373NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74HCT373NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT373NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT373NSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT373PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT373PWE4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT373PWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT373PWLE	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI
SN74HCT373PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT373PWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT373PWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
						no Sb/Br)		
SN74HCT373PWT	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT373PWTE4	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT373PWTG4	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54HCT373FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54HCT373J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type
SNJ54HCT373W	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HCT373DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74HCT373DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74HCT373NSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1
SN74HCT373PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74HCT373PWT	TSSOP	PW	20	250	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HCT373DBR	SSOP	DB	20	2000	346.0	346.0	33.0
SN74HCT373DWR	SOIC	DW	20	2000	346.0	346.0	41.0
SN74HCT373NSR	SO	NS	20	2000	346.0	346.0	41.0
SN74HCT373PWR	TSSOP	PW	20	2000	346.0	346.0	33.0
SN74HCT373PWT	TSSOP	PW	20	250	346.0	346.0	33.0

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

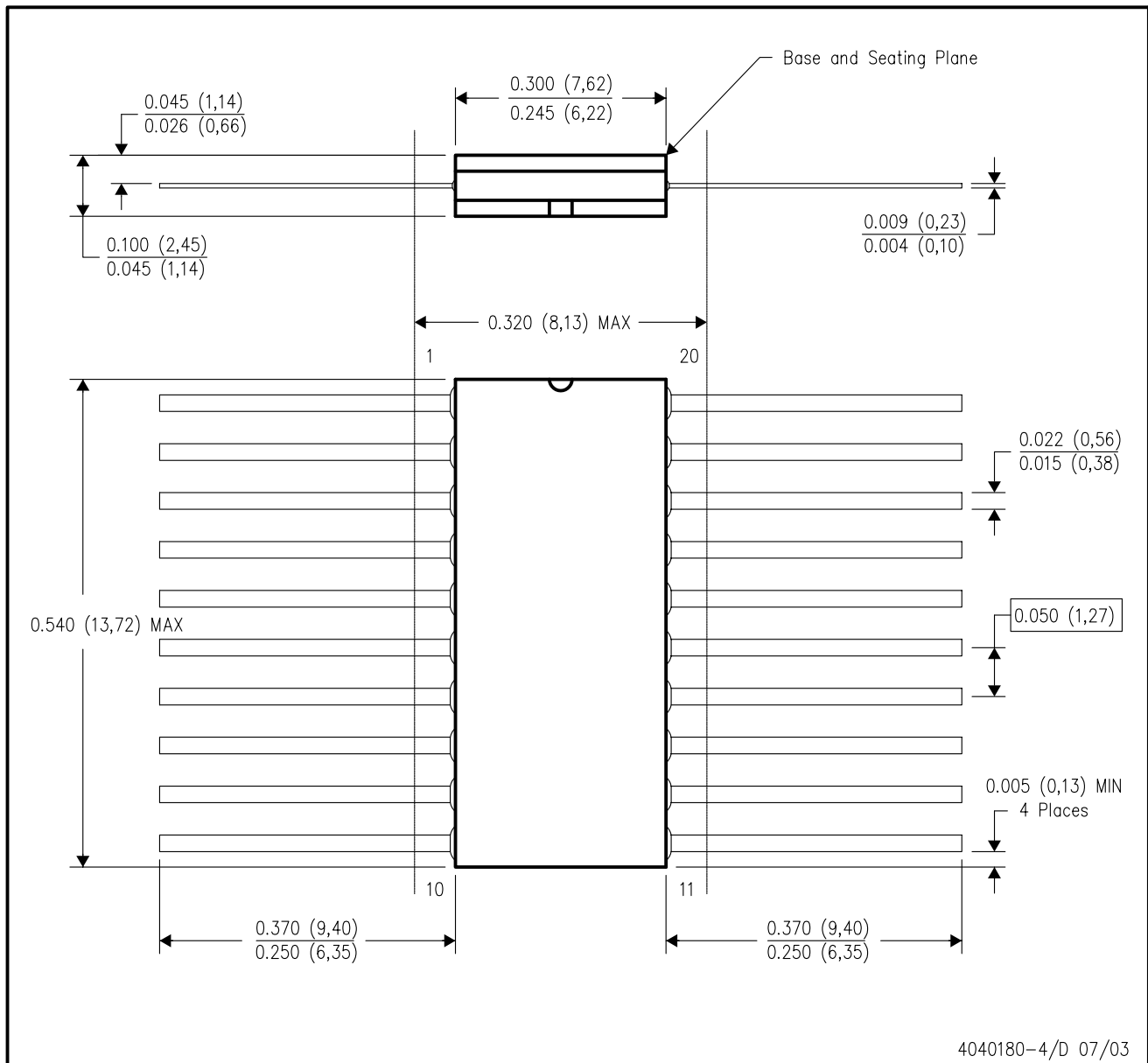


4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within Mil-Std 1835 GDFP2-F20

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



4040140/D 10/96

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 D The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

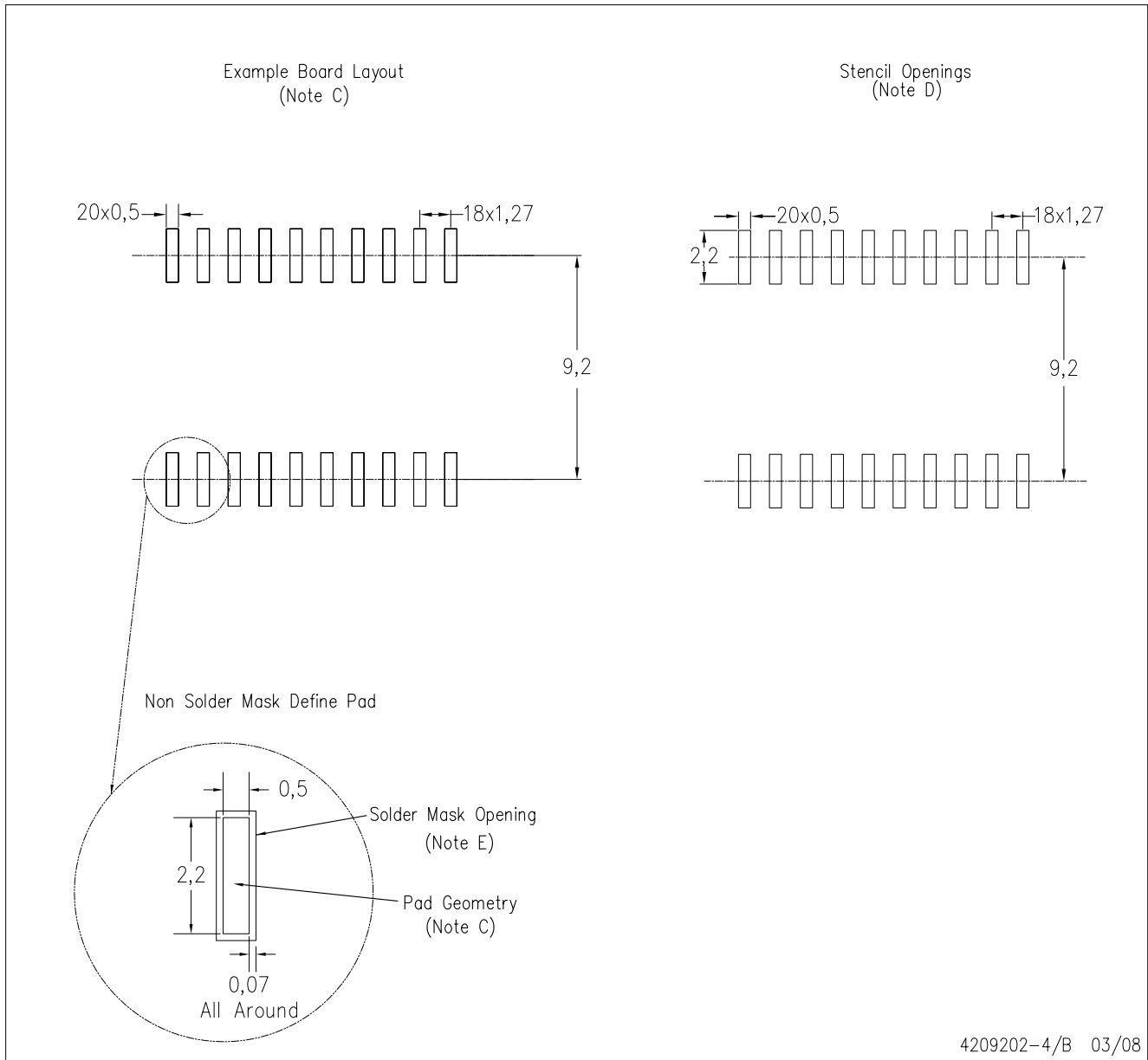
DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-013 variation AC.

DW (R-PDSO-G20)



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN

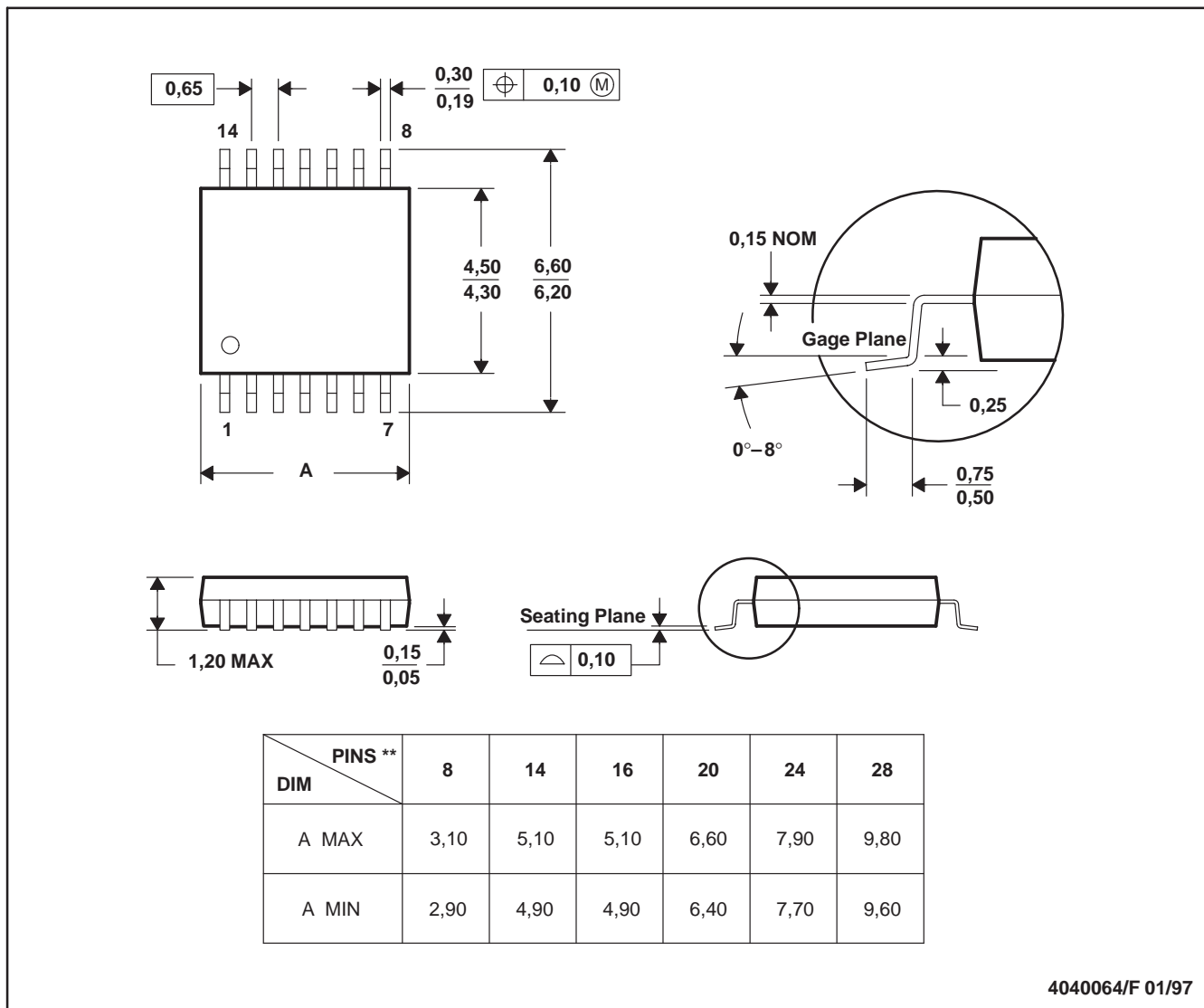


- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
RF/IF and ZigBee® Solutions	www.ti.com/lprf

Applications

Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Transportation and Automotive	www.ti.com/automotive
Video and Imaging	www.ti.com/video
Wireless	www.ti.com/wireless-apps

TI E2E Community Home Page

e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2011, Texas Instruments Incorporated