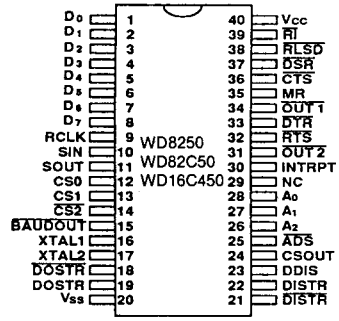
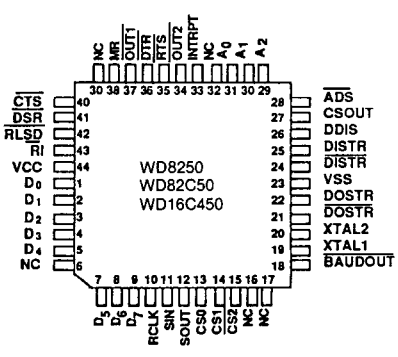
WD8250/82C50/16C450 Asynchronous Communications Element (ACE)

FEATURES

- Designed to be Easily Interfaced to Most Microprocessors (Z-80, 8080A, 8088, 68000, etc.)
- Generating and Stripping of Serial Asynchronous Data Control Bits (Start, Stop, Parity)
- Full Double Buffering Allows Imprecise Synchronization
- Independently Controlled Transmit, Receive, Line Status, and Data Set Interrupts
- Programmable Baud Rate Generator Allows Division of Any Input Clock by 1 to $(2^{16}-1)$ and Generates the Internal 16x Clock
- Independent Receiver Clock Input
- MODEM Interface Capabilities
- Fully Programmable Serial-Interface Characteristics
  - 5-, 6-, 7-, or 8-Bit Characters
  - Even, Odd, or No-Parity Bit Generation and Detection
  - 1-, 1 1/2-, or 2-Stop Bit Generation
  - Baud Rate Generation (DC to 56K Baud)**
- False Start Bit Detector
- Complete Status Reporting Capabilities
- THREE-STATE TTL Drive Capabilities for Bi-directional Data Bus and Control Bus
- Line Break Generation and Detection
- Internal Diagnostic Capabilities
  - Loopback Controls for Communications Link Fault Isolation
- Break, Parity, Overrun, Framing Error Simulation
- Full Prioritized Interrupt System Controls
- Single +5-Volt Power Supply
- Low CMOS Power Dissipation (WD82C50, WD16C450)
- Available in 40-Pin Dual-in-Line and 44-Pin QCM Packages



PIN DESIGNATION (DIP)



QUAD PIN DESIGNATION (QUAD)*

DESCRIPTION

The WD8250/82C50/16C450 is a programmable Asynchronous Communication Element (ACE). The device is fabricated in N/MOS (WD8250) and CMOS (WD82C50 and WD16C450) silicon gate technology.

The ACE is a software-oriented device using a three-state, 8-bit, bi-directional data bus.

The ACE is used to convert parallel data to a serial format on the transmit side, and convert serial data to parallel on the receiver side. The serial format, in order of transmission and reception, is a start bit, followed by 5 to 8 data bits, a parity bit (if programmed) and 1-, 1 1/2- (5-bit format only) or 2-stop bits. The maximum recommended data rate is 56K baud.**

Internal registers enable the user to program various types of interrupts, modem controls, and character formats. The user can read the status of the ACE at any time monitoring word conditions, interrupts and modem status.

An additional feature of the ACE is a programmable baud rate generator capable of dividing an internal XTAL or TTL signal clock by a division of 1 to $(2^{16}-1)$.

The ACE is designed to work in either a polling or interrupt driven system, which is programmable by user's software controlling an internal register.

*Consult Western Digital Sales Office for other pinouts.

**Contact Western Digital Sales Office for information regarding exceeding this recommended maximum baud rate.

PIN DESCRIPTION

PIN NUMBERS DIP	PIN NUMBERS QUAD	MNEMONIC	SIGNAL NAME	FUNCTION
1 thru 8	1thru5 and 7thru9	D0 thru D7	DATA BUS	3-state, bi-directional communication lines between the ACE and Data Bus. All prepared TX and assembled REC data, Control characters, and Status information are transferred via the data bus (D0-D7).
—	6	NC	NO CONNECT	No Connect.
9	10	RCLK	RECEIVE CLK	This input is the 16X baud rate clock for the receiver section of the chip, may be tied to $\overline{\text{BAUDOUT}}$ (pin 15 for DIP package and/or pin 18 for QUAD package).
10	11	SIN	SERIAL INPUT	Received Serial Data In from the communications link (Peripheral device, modem or data set).
11	12	SOUT	SERIAL OUTPUT	Transmitted Serial Data Out to the communication link. The SOUT signal is set to a (logic1) marking condition upon a MASTER RESET.
12	13	CS0	CHIP SELECT	When CS0 and CS1 are high, and $\overline{\text{CS2}}$ is low, chip is selected. Selection is complete when the address strobe $\overline{\text{ADS}}$ latches the chip select signals.
13	14	CS1	CHIP SELECT	
14	15	$\overline{\text{CS2}}$	CHIP SELECT	
—	16	NC	NO CONNECT	No Connect.
—	17	NC	NO CONNECT	No Connect.
15	18	$\overline{\text{BAUDOUT}}$	$\overline{\text{BAUDOUT}}$	16X clock signal for the transmitter section of the ACE. The clock rate is equal to the oscillator frequency divided by the divisor loaded into the divisor latches. The $\overline{\text{BAUDOUT}}$ signal may be used to clock the receiver by tying to RCLK (pin 9 for DIP package and/or pin 10 for QUAD package).
16	19	XTAL 1	EXTERNAL CLOCK IN	These pins connect the crystal or signal clock to the ACE baud rate divisor circut. See Fig. 5 and 6 for circuit connection diagrams.
17	20	XTAL 2	EXTERNAL CLOCK OUT	
18	21	$\overline{\text{DOSTR}}$	$\overline{\text{DATA OUT STROBE}}$	When the chip has been selected, a low $\overline{\text{DOSTR}}$ or high DOSTR will latch data into the selected WD8250/82C50/16C450 register (a CPU write). Only one of these lines need be used. Tie unused line to its inactive state, $\overline{\text{DOSTR}}$-high or DOSTR-low.
19	22	DOSTR	DATA OUT STROBE	
20	23	V_{SS}	GROUND	System signal ground.
21	24	$\overline{\text{DISTR}}$	$\overline{\text{DATA IN STROBE}}$	When chip has been selected, a low $\overline{\text{DISTR}}$ or high DISTR will allow a read of the selected WD8250/82C50/16C450 register (a CPU read). Only one of these lines need be used. Tie unused line to its inactive state, $\overline{\text{DISTR}}$-high or DISTR-low.
22	25	DISTR	DATA IN STROBE	
23	26	DDIS	DRIVER DISABLE	Output goes low whenever data is being read from the ACE. Can be used to reverse data direction of external transceiver.
24	27	CSOUT	CHIP SELECT OUT	Output goes high when chip is selected. No data transfer can be initiated until CSOUT is high.
25	28	$\overline{\text{ADS}}$	$\overline{\text{ADDRESS STROBE}}$	When low, provides latching for Register Select (A0, A1, A2) and Chip Select (CS0, CS1, $\overline{\text{CS2}}$). NOTE: The rising edge (↑) of the $\overline{\text{ADS}}$ signal is required when the Register Select (A0, A1, A2) and the Chip Select (CS0, CS1, $\overline{\text{CS2}}$) signals are not stable for the duration of a read or write operation. If not required, the $\overline{\text{ADS}}$ input can be tied permanently low.
26	29	A2	REGISTER SELECT A2	These three inputs are used to select an internal register of the ACE during a read or a write. See Table 1.
27	30	A1	REGISTER SELECT A1	
28	31	A0	REGISTER SELECT A0	

PIN NUMBERS DIP	PIN NUMBERS QUAD	MNEMONIC	SIGNAL NAME	FUNCTION
29	32	NC	NO CONNECT	No Connect.
30	33	INTRPT	INTERRUPT	Output goes high whenever an enabled interrupt is pending.
31	34	$\overline{OUT2}$	$\overline{OUTPUT\ 2}$	User-designated output that can be programmed by Bit 3 of the Modem Control Register ($\overline{OUT2}$ goes low when Bit 3 = 1).
32	35	$\overline{RTS}$	$\overline{REQUEST\ TO\ SEND}$	Output when low informs the modem or data set that the ACE is ready to transmit data. See Modem Control Register.
33	36	$\overline{DTR}$	$\overline{DATA\ TERMINAL\ READY}$	Output when low informs the modem or data set that the ACE is ready to receive.
34	37	$\overline{OUT1}$	$\overline{OUTPUT\ 1}$	User-designated output that can be programmed by Bit 2 of Modem Control Register ($\overline{OUT1}$ goes low when Bit 2 = 1).
35	38	MR	MASTER RESET	When high clears the registers to the states as indicated in Table 2.
—	39	NC	NO CONNECT	No Connect.
36	40	$\overline{CTS}$	$\overline{CLEAR\ TO\ SEND}$	Input from DCE indicating remote device is ready to transmit. See Modem Status Register.
37	41	$\overline{DSR}$	$\overline{DATA\ SET\ READY}$	Input from DCE used to indicate the status of the local data set. See Modem Status Register.
38	42	$\overline{RSLD}$	$\overline{RECEIVER\ LINE\ SIGNAL\ DETECT}$	Input from DCE indicating that it is receiving a signal which meets its signal quality conditions. See Modem Status Register.
39	43	$\overline{RI}$	$\overline{RING\ INDICATOR}$	Input when low indicates that a ringing signal is being received by the modem or data set. See Modem Status Register.
40	44	V_{CC}	+5V	+5 Volt Supply.

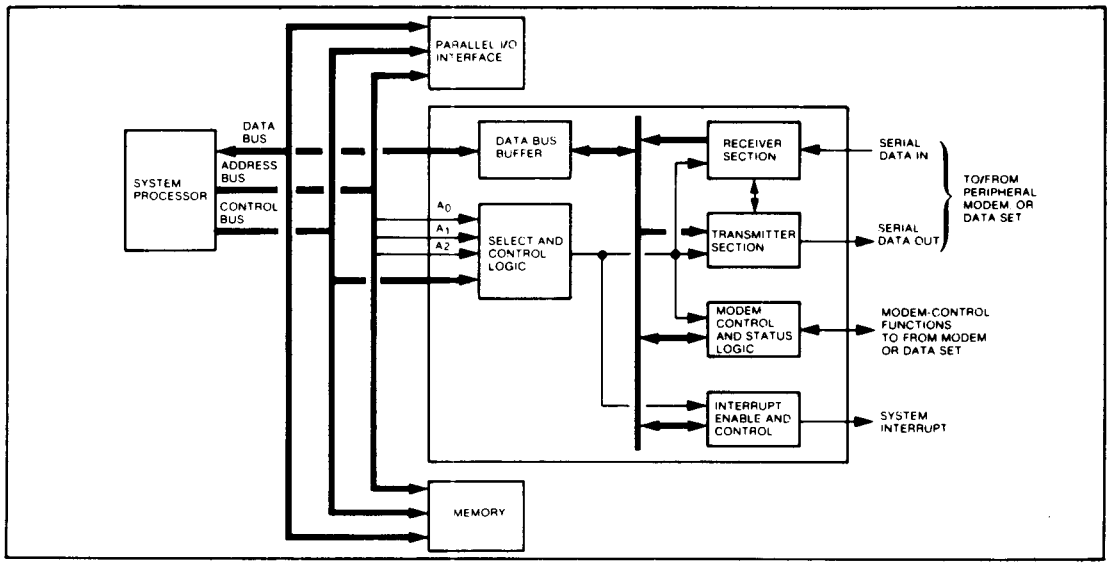


FIGURE 1. WD8250/82C50/16C450 GENERAL SYSTEM CONFIGURATION

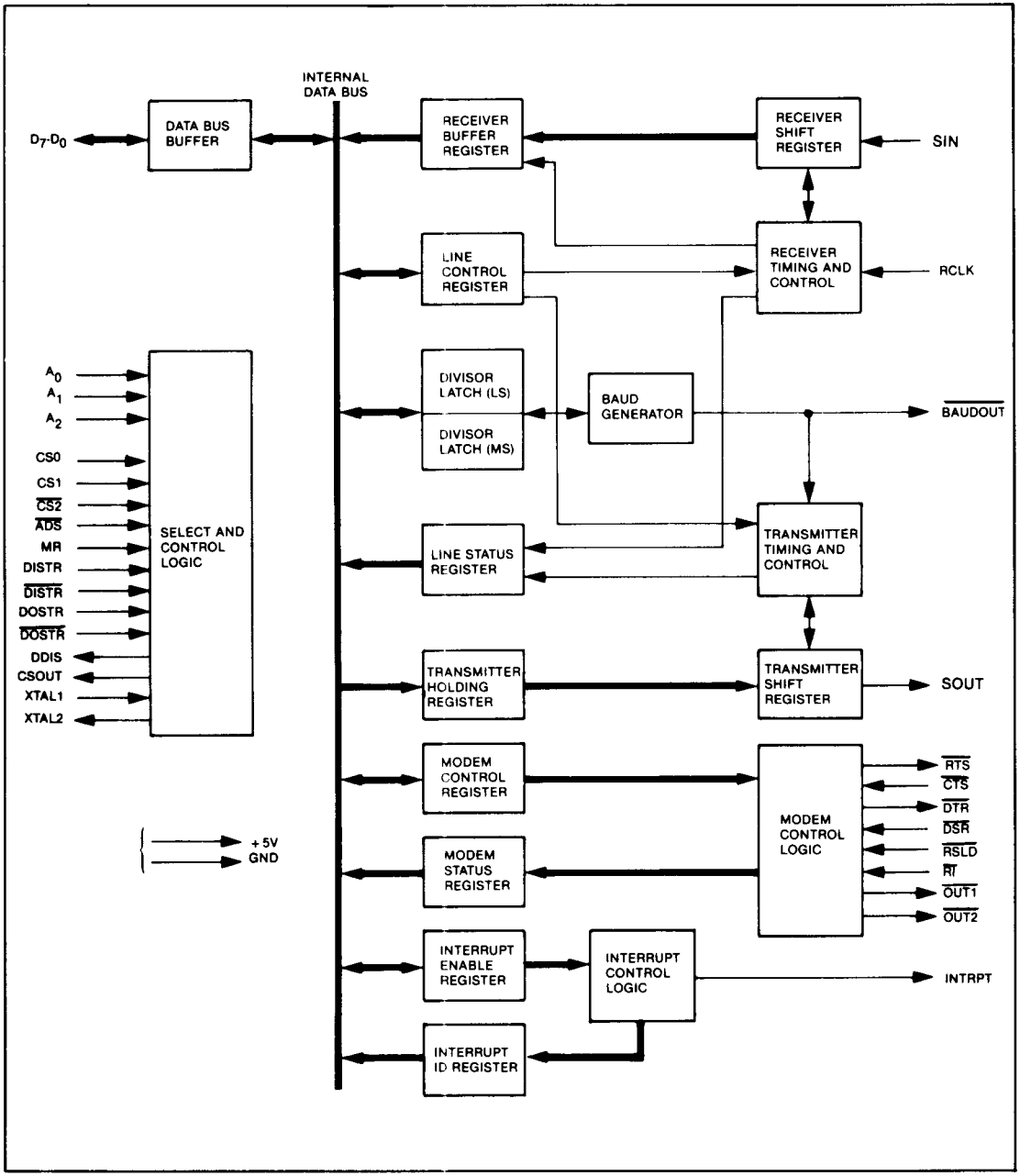


FIGURE 2. WD8250/82C50/16C450 BLOCK DIAGRAM

CHIP SELECTION AND REGISTER ADDRESSING

Address Strobe ($\overline{ADS}$): When low, provides latching for register select (A0, A1, A2) and chip select (CS0, CS1, $\overline{CS2}$).

NOTE: The rising edge (↑) of the $\overline{ADS}$ input is required when Register Select (A0, A1, A2) and Chip Select (CS0, CS1, $\overline{CS2}$) signals are not stable for the duration of a read or write operation. If $\overline{ADS}$ is not required for latching, this input can be tied permanently low.

Chip Select (CS0, CS1, $\overline{CS2}$): The definition of a chip selected is CS0, CS1 both high and $\overline{CS2}$ low. Chip selection is complete when latched by $\overline{ADS}$ or $\overline{ADS}$ is tied low.

Register Select (A0, A1, A2): To select a register for read or write operation, see Table 1.

NOTE: (DLAB) Divisor Latch Access Bit is the MSB of the Line Control Register. DLAB must be programmed high (logic 1) by the system software to access the Baud Rate Generator Divisor Latches.

TABLE 1. REGISTER ADDRESSING

DLAB	A2	A1	A0	Register
0	0	0	0	Receiver Buffer (read), Transmitter Holding Register (write)
0	0	0	1	Interrupt Enable
X	0	1	0	Interrupt Identification (read only)
X	0	1	1	Line Control
X	1	0	0	MODEM Control
X	1	0	1	Line Status
X	1	1	0	MODEM Status
X	1	1	1	See Note 1
1	0	0	0	Divisor Latch (least significant byte)
1	0	0	1	Divisor Latch (most significant byte)

NOTE 1: For this address, WD8250/82C50 = NOT ACCESSIBLE
WD16C450 = SCRATCH PAD

ACE OPERATIONAL DESCRIPTION

Master Reset A high-level input on this pin causes the ACE to reset to the condition listed in Table 2.

ACE Accessible Registers The system programmer has access to any of the registers as summarized in Table 3. For individual register descriptions, refer to the following pages under register heading.

TABLE 2. RESET CONTROL OF REGISTERS AND PINOUT SIGNALS

Register/Signal	Reset Control	Reset State
Receiver Buffer Register	First Word Received	Data
Transmitter Holding Register	Writing into the Transmitter Holding Register	Data
Interrupt Enable Register	Master Reset	All Bits Low (0-3 forced and 4-7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is High and Bits 1-7 Are Permanently Low
Line Control Register	Master Reset	All Bits Low
MODEM Control Register	Master Reset	All Bits Low
Line Status Register	Master Reset	All Bits Low, Except Bits 5 and 6 Are High
Modem Status Register	Master Reset MODEM Signal Inputs	Bits 0-3 Low Bits 4-7 — Input Signal
Divisor Latch (low order bits)	Writing into the Latch	Data
Divisor Latch (high order bits)	Writing into the Latch	Data
SOUT	Master Reset	High
$\overline{BAUDOUT}$	Writing into either Divisor Latch	Low
CSOUT	$\overline{ADS}$ Strobe Signal and State of Chip Select Lines	High/Low
DDIS	DDIS = $\overline{CSOUT} \cdot RCLK \cdot \overline{DISTR}$ (At Master Reset, the CPU sets RCLK and DISTR low.)	High
INTRPT	Master Reset	Low
$\overline{OUT\ 2}$	Master Reset	High
$\overline{RTS}$	Master Reset	High
$\overline{DTR}$	Master Reset	High
$\overline{OUT\ 1}$	Master Reset	High
D7-D0 Data Bus Lines	In THREE-STATE Mode. Unless CSOUT • DISTR = High or CSOUT • DOSTR = High	THREE-STATE Data (ACE to CPU) Data (CPU to ACE)

TABLE 3. ACCESSIBLE WD8250/82C50/16C450 REGISTERS

	Register Address**									
	0 DLAB=0	0 DLAB=0	1DLAB=0	2	3	4	5	6	0DLAB=1	1DLAB=1
Bit No.	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Identification Register	Line Control Register	MODEM Control Register	Line Status Register	MODEM Status Register	Divisor Latch (LS)	Divisor Latch (MS)
0	Data Bit 0*	Data Bit 0*	Enable Received Data Available Interrupt (ERBFI)	"0" if Interrupt Pending	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit (0)	Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OR)	Delta Data Set Ready (DDSR)	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit (1)	Number of Stop Bits (STB)	Out 1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	Enable MODEM Status Interrupt (EDSSI)	0	Parity Enable (PEN)	Out 2	Framing Error (FE)	Delta Receive Line Signal Detect (DRLSD)	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Stick Parity	0	Transmitter Holding Register Empty (THRE)	Data Set Ready (DSR)	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	0	Set Break	0	Transmitter Shift Register Empty (TSRE)	Ring Indicator (RI)	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	0	Divisor Latch Access Bit (DLAB)	0	0	Received Line Signal Detect (RLSD)	Bit 7	Bit 15

**Address 7 is a Scratch Pad Register on WD16C450; it is not accessible on WD8250 and WD82C50.

Line Control Register

Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 are as follows:

Bit 1	Bit 0	Word Length
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

Bit 2: This bit specifies the number of stop bits in each transmitted or received serial character. If bit 2 is logic 0, 1 Stop bit is generated or checked in the transmit or receive data, respectively. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, 1-1/2 Stop bits are generated or checked. If bit 2 is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, 2 Stop bits are generated or checked.

Bit 3: This bit is the Parity Enable bit. When bit 3 is a logic 1, a Parity bit is generated (Transmit data) or checked (Receive data) between the last data word bit and Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1s when the data word bits and the Parity bit are summed.)

Bit 4: This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of bits is transmitted or checked.

Bit 5: This bit is the Stick Parity bit. When bit 3 is a logic 1 and bit 5 is a logic 1, the Parity bit is transmitted and then detected by the receiver in the opposite state indicated by bit 4.

Bit 6: This bit is the Set Break Control bit. When bit 6 is a logic 1, the serial output (SOUT) is forced to the Spacing (logic 0) state and remains there (until reset by a low-level bit 6) regardless of other transmitter activity. The feature enables the CPU to alert a terminal in a computer communications system.

Bit 7: This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Rate Generator duirng a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

ACE Programmable Baud Rate Generator

The ACE contains a programmable Baud Rate Generator capable of taking any clock input (DC to 3.1 MHz) and dividing it by any divisor from 1 to ($2^{16}-1$). The output frequency of the Baud Generator is 16x the Baud rate. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization in order to insure desired operation of the Baud Rate Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded. This prevents long counts on initial load.

Tables 4 and 5 illustrate the use of the Baud Generator with two different driving frequencies. One is referenced to a 1.8432 MHz crystal. The other is a 3.072 MHz crystal. (See following note.)

NOTE: The maximum operating frequency of the Baud Generator is 3.1 MHz.

A divisor of 1 is not allowed when using a 1.8432 MHz crystal.

A divisor of 1 or 2 is not allowed when using a 3.072 MHz crystal.

In no case should the data rate be greater than 56K Baud.

See Crystal Specifications on Page 12.

TABLE 4. BAUD RATES USING 1.8432 MHz CRYSTAL

Desired Baud Rate	Divisor Used to Generate 16x Clock	Percent Error Difference Between Desired and Actual
50	2304	—
75	1536	—
110	1047	0.026
134.5	857	0.058
150	768	—
300	384	—
600	192	—
1200	96	—
1800	64	—
2000	58	0.69
2400	48	—
3600	32	—
4800	24	—
7200	16	—
9600	12	—
19200	6	—
38400	3	—
56000	2	2.86

TABLE 5. BAUD RATES USING 3.072 MHz CRYSTAL

Desired Baud Rate	Divisor Used to Generate 16x Clock	Percent Error Difference Between Desired and Actual
50	3840	—
75	2560	—
110	1745	0.026
134.5	1428	0.034
150	1280	—
300	640	—
600	320	—
1200	160	—
1800	107	—
2000	96	—
2400	80	—
3600	53	0.628
4800	40	—
7200	27	1.23
9600	20	—
19200	10	—
38400	5	—
56000	3	14.285

Line Status Register

This 8-bit register provides status information to the CPU concerning the data transfer. Its contents are indicated in Table 3 and are described below.

Bit 0: This bit is the Receiver Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. Bit 0 will be reset to a logic 0 either by the CPU reading the data in the Receiver Buffer Register or by writing a logic 0 into it from the CPU.

Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

Bit 2: This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. The PE bit is set to a logic 1 upon detection of a parity error and is reset to a logic 0 whenever the CPU reads the contents of the Line Status Register.

Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop bit. Bit 3 is set to a logic 1 whenever the Stop bit following the last data bit or parity bit is detected as a zero bit (Spacing level).

Bit 4: This bit is the Break Interrupt (BI) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the Spacing (Logic 0) state for longer than a full word transmission time (that is, the total time of Start bit + data bits + Parity + Stop bits).

NOTE: Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected.

Bit 5: This bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the ACE is ready to accept a new character for transmission. In addition, this bit causes the ACE to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic 0 concurrently with the loading of the Transmitter Holding Register by the CPU.

Bit 6: This bit is the Transmitter Shift Register Empty (TSRE) indicator and is a read-only bit. For WD8250 and WD82C50, bit 6 is set to a logic 1 whenever the Transmitter Shift Register is idle (empty). It is reset to a logic 0 upon a data transfer from the Transmitter Holding Register to the Transmitter Shift Register. It toggles between a logic 0 and a logic 1 during multiple data transfer.

For WD16C450, bit 6 is set to a logic 1 when both transmitter registers (Transmitter Holding Register and Transmitter Shift Register) are idle (empty). It is reset to a logic 0 upon loading of data into the Transmitter Holding Register. During a multiple data transfer, it remains in a logic 0 state (will not toggle) until the transfer is complete and both transmitter registers are empty.

Bit 7: This bit is permanently set to logic 0.

Interrupt Identification Register

The ACE has an interrupt capability that allows for complete flexibility in interfacing to all popular microprocessors presently available. In order to provide minimum software overhead during data character transfers, the ACE prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows: Receiver Line Status (priority 1); Received Data Ready (priority 2); Transmitter Holding Register Empty (priority 3); and MODEM Status (priority 4).

Information indicating that a prioritized interrupt is pending and source of that interrupt is stored in the Interrupt Identification Register (refer to Table 6). This register (IIR), when addressed during chip-select time, freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU. Its contents are indicated in Table 3 and are described below.

Bit 0: This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending and polling (if used) continues.

Bits 1 and 2: These two bits are used to identify the highest priority interrupt pending (see Table 6).

Bits 3 through 7: These five bits are always logic 0.

Interrupt Enable Register

This 8-bit register enables the four interrupt sources of the ACE to separately activate the chip Interrupt (INTRPT) output signal. Its contents are indicated in Table 3 and are described below. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output from the chip. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Registers.

Bit 0: This bit enables the Received Data Available Interrupt when set to logic 1.

Bit 1: This bit enables the Transmitter Holding Register Empty Interrupt when set to logic 1.

Bit 2: This bit enables the Receiver Line Status Interrupt when set to logic 1.

Bit 3: This bit enables the MODEM Status Interrupt when set to logic 1.

Bits 4 through 7: These four bits are always logic 0.

TABLE 6. INTERRUPT CONTROL FUNCTIONS

Interrupt Identification Register			Interrupt Set and Reset Functions			
Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Flag	Interrupt Source	Interrupt Reset Control
0	0	1	—	None	None	—
1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
1	0	0	Second	Received Data Available	Receiver Data Available	Reading the Receiver Buffer Register
0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Received Line Signal Detect	Reading the MODEM Status Register

MODEM Control Register

This 8-bit register controls the interface either with the MODEM or data set (or a peripheral device emulating a MODEM). The contents of the MODEM Control Register are indicated in Table 3.

Bit 0: This bit controls the Data Terminal Ready ($\overline{DTR}$) output. When bit 0 is set to a logic 1, the $\overline{DTR}$ output is forced to a logic 0. When bit 0 is reset to a logic 0, the $\overline{DTR}$ output is forced to a logic 1.

NOTE: The $\overline{DTR}$ output of the ACE may be applied to an EIA inverting line driver (such as the DS1488) to obtain the proper polarity input at the succeeding MODEM or data set.

Bit 1: This bit controls the Request to Send ($\overline{RTS}$) output. Bit 1 affects the $\overline{RTS}$ output in a manner identical to that described above for bit 0.

Bit 2: This bit controls the Output 1 ($\overline{OUT\ 1}$) signal, which is an auxiliary user-designated output. Bit 2 affects the $\overline{OUT\ 1}$ output in a manner identical to that described above for bit 0.

Bit 3: This bit controls the Output 2 ($\overline{OUT\ 2}$) signal, which is an auxiliary user-designated output. Bit 3 affects the $\overline{OUT\ 2}$ output in a manner identical to that described above for bit 0.

Bit 4: This bit provides a loopback feature for diagnostic testing of the ACE. When bit 4 is set to logic 1, the following occur: the transmitter Serial Output (SOUT) is set to a logic 1 (high) state; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input; the four MODEM Control Inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{RLSD}$, and $\overline{RI}$) are disconnected; and the four MODEM Control outputs ($\overline{RTS}$, $\overline{DTR}$, $\overline{OUT2}$, $\overline{OUT1}$) are internally connected to the four MODEM Control inputs. In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit- and receive-data paths of the ACE.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the four MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

The ACE interrupt system can be tested by writing into the lower six bits of the Line Status Register and the lower four bits of the MODEM Status Register. Setting any of these bits to a logic 1 generates the appropriate interrupt (if enabled). The resetting of these interrupts is the same as in normal ACE operation. To return to this operation, the registers must be reprogrammed for normal operation and then bit 4 must be reset to a logic 0.

Bits 5 through 7: These bits are permanently set to a logic 0.

MODEM Status Register

This 8-bit register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. In addition to this current-state information, four bits of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

The contents of the MODEM Status Register are indicated in Table 3 and are described below.

Bit 0: This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the $\overline{CTS}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 1: This bit is the Delta Data Set Ready (DDSR) indicator. Bit 1 indicates that the $\overline{DSR}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 2: This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the $\overline{RI}$ input to the chip has changed from an On (logic 1) to an Off (logic 0) condition.

Bit 3: This bit is the Delta Received Line Signal Detector (DRLSD) indicator. Bit 3 indicates that the $\overline{RLSD}$ input to the chip has changed state.

NOTE: Whenever bit 0, 1, 2, or 3 is set to logic 1, a MODEM Status Interrupt is generated.

Bit 4: This bit is the complement of the Clear to Send ($\overline{CTS}$) input. This bit becomes equivalent to $\overline{RTS}$ of the MODEM contol register, if Bit 4 of the MODEM control register is set to 1.

Bit 5: This bit is the complement of the Data Set Ready ($\overline{DSR}$) input. This bit becomes equivalent to $\overline{DTR}$ of the MODEM control register, if Bit 4 of the MODEM control register is set to 1.

Bit 6: This bit is the complement of the Ring Indicator ($\overline{RI}$) input. This bit becomes equivalent to $\overline{OUT1}$ of the MODEM control register, if Bit 4 of the MODEM control register is set to 1.

Bit 7: This bit is the complement of the Received Line Signal Detect ($\overline{RLSD}$) input. This bit becomes equivalent to $\overline{OUT2}$ of the MODEM control register, if Bit 4 of the MODEM control register is set to 1.

Typical Applications

Figures 3 and 4 show how to use the ACE chip in an 8080A system and in a microcomputer system with a high-capacity data bus.

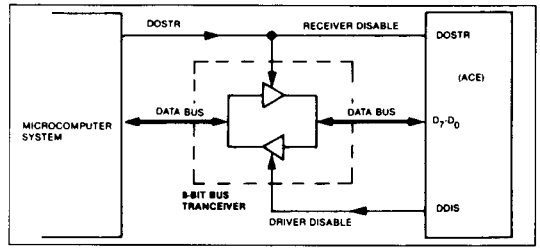


FIGURE 3. TYPICAL INTERFACE FOR A HIGH-CAPACITY DATA BUS

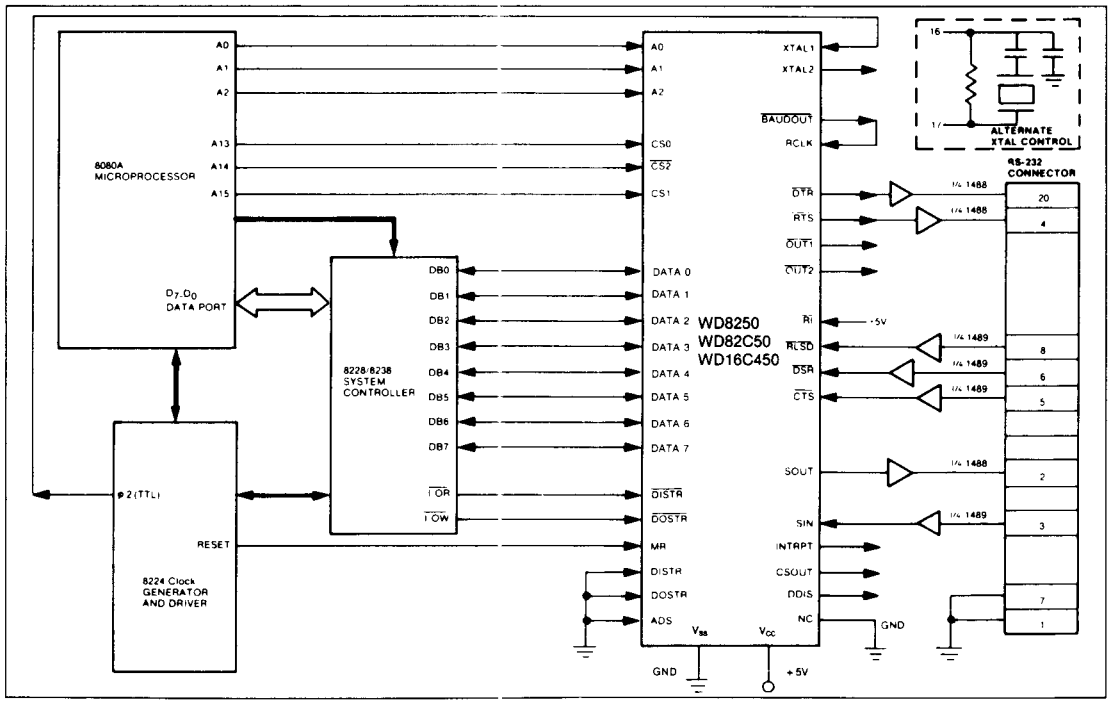


FIGURE 4. TYPICAL 8-BIT MICROPROCESSOR/RS-232 TERMINAL INTERFACE USING THE ACE

ABSOLUTE MAXIMUM RATINGS

Temperature
Under Bias ..... 0°C (32°F) to 70°C (158°F)
Storage Temperature
Ceramic .... −65°C (−85°F) to +150°C (302°F)
Plastic ..... −50°C (−58°F) to +125°C (257°F)
All Input or Output Voltages
with respect to V_{SS} ..... -0.5 v to +7.0 V

Power Dissipation WD8250 ..... 750 mW
WD82C50 ..... 110 mW
WD16C450 ..... 110 mW

Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under DC Operating Characteristics.

TABLE 7. DC OPERATING CHARACTERISTICS

T_A = 0°C (32°F) to + 70°C (158°F), V_{CC} = +5V ±5%, V_{SS} = 0V, unless otherwise specified

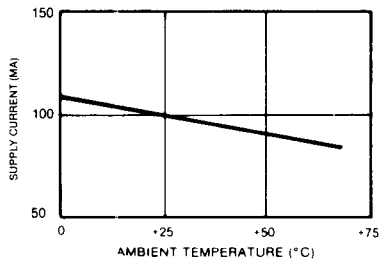
SYMBOL	CHARACTERISTIC	WD8250 MIN	WD8250 MAX	WD82C50 MIN	WD82C50 MAX	WD16C450 MIN	WD16C450 MAX	UNITS	TEST CONDITIONS
V_{ILX}	Clock Input Low Voltage	-0.5	0.8	-0.5	0.8	-0.5	0.8	V	
V_{IHX}	Clock Input High Voltage	2.4	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	V	
V_{IL}	Input Low Voltage	-0.5	0.8	-0.5	0.8	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.2	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	V	
V_{OL}	Output Low Voltage		0.45		0.4		0.4	V	I_{OL} = 1.6mA on all outputs
V_{OH}	Output High Voltage	2.4		2.4		2.4		V	I_{OH} = -100μA
I_{CC}	(AV) Average Power Supply Current (V_{CC})		150		20		20	mA	V_{CC} = 5.25V. No loads on SIN, DSR, RLSD, CTS. RI = 2.0V. All other inputs = 0.8V. Baud rate generator at 4MHz. Baud rate at 56K.
I_{IL}	Input Leakage		± 10		± 10		± 10	μA	V_{CC} = 5.25V. V_{SS} = 0V. All other pins floating.
I_{CL}	Clock Leakage		± 10		± 10		± 10	μA	V_{IN} = 0V. 5.25V.
I_{DL}	Data Bus Leakage		± 10		± 10		± 10	μA	V_{OUT} = 0.4V V_{OUT} = 4.6V Data Bus is at High-Impedance State
V_{ILMR}	MR Schmitt V_{IL}		N/A		N/A		0.8	V	
V_{IHMR}	MR Schmitt V_{IH}	N/A		N/A		2.0		V	

TABLE 8. CAPACITANCE

T_A = 25°C (77°F), f = 1.0MHz, V_{CC} = V_{SS} = OV

SYMBOL	CHARACTERISTIC	WD8250 TYP	WD8250 MAX	WD82C50 WD16C450 TYP	WD82C50 WD16C450 MAX	UNITS	TEST CONDITIONS
C_{XIN}	Clock Input Capacitance	10	15	15	20	pF	fc = 1 MHz
C_{XOUT}	Clock Output Capacitance	20	30	20	30	pF	
C_{IN}	Input Capacitance	6	10	6	10	pF	Unmeasured pins
C_{OUT}	Output Capacitance	10	20	10	20	pF	returned to V_{SS}

Typical Supply Current vs. Temperature, Normalized



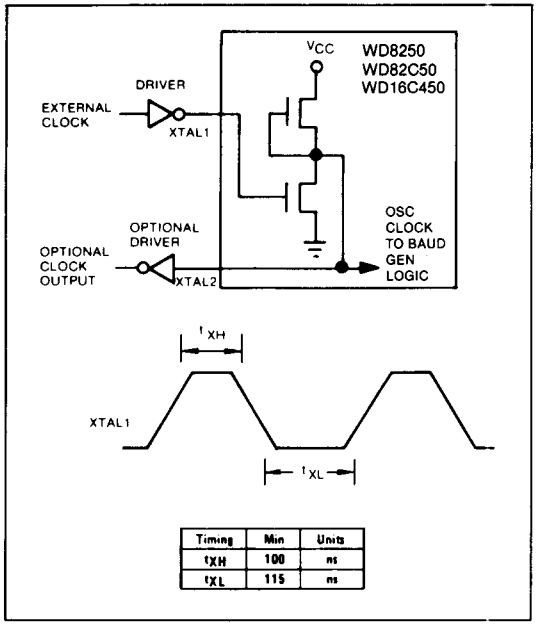


FIGURE 5. EXTERNAL CLOCK INPUT (3.1 MHz MAX.)

CRYSTAL MANUFACTURERS (Partial List)

American Time Products Division
Frequency Control Products, Inc.
Woodwide, New York 11377

Bliley Electric Company
Erie, Pennsylvania 16508

Erie Frequency Control
Calisle, Pennsylvania 17013

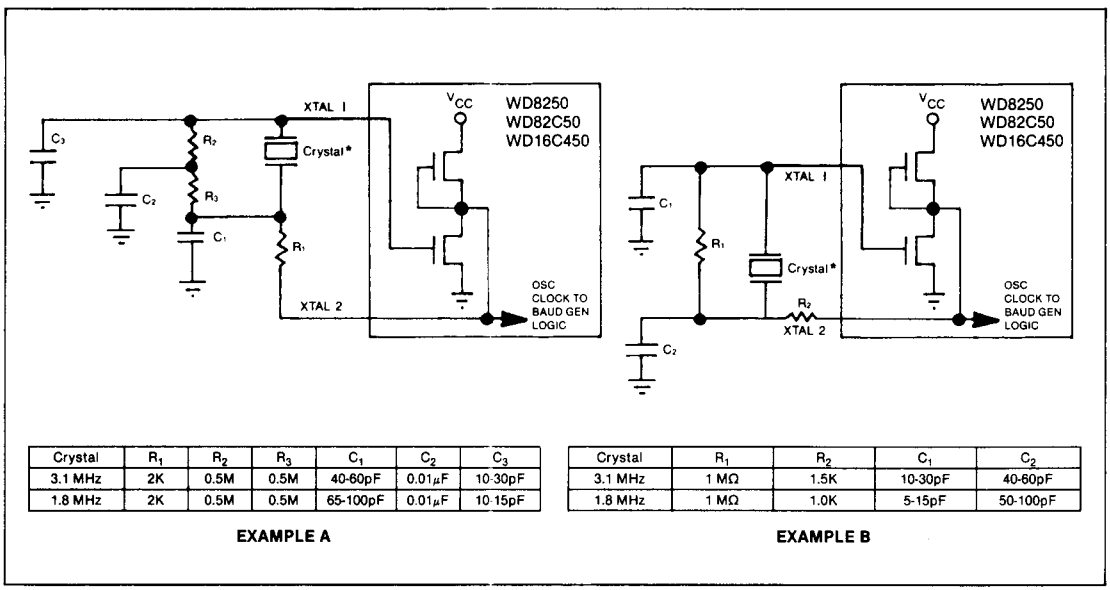
Q-Matic Corporation
Costa Mesa, California 92626

CRYSTAL SPECIFICATIONS

Frequency: 1.8432 MHz and 3.072 MHz
Type: Microprocessor Crystal

Temperature range: 0°C to +70°C
Series resistance: 200Ω to 500Ω (1.8432 MHz)
100Ω to 200Ω (3.072 MHz)

Series resonant
Overall tolerance ±0.01%



Crystal	R_1	R_2	R_3	C_1	C_2	C_3
3.1 MHz	2K	0.5M	0.5M	40-60pF	0.01μF	10-30pF
1.8 MHz	2K	0.5M	0.5M	65-100pF	0.01μF	10-15pF

EXAMPLE A

Crystal	R_1	R_2	C_1	C_2
3.1 MHz	1 MΩ	1.5K	10-30pF	40-60pF
1.8 MHz	1 MΩ	1.0K	5-15pF	50-100pF

EXAMPLE B

FIGURE 6. TYPICAL CRYSTAL OSCILLATOR NETWORKS
*See Crystal Specifications

AC OPERATING CHARACTERISTIC

T_A = 0°C (32°F) to +70°C (158°F), V_{SS} = +5V ±5%

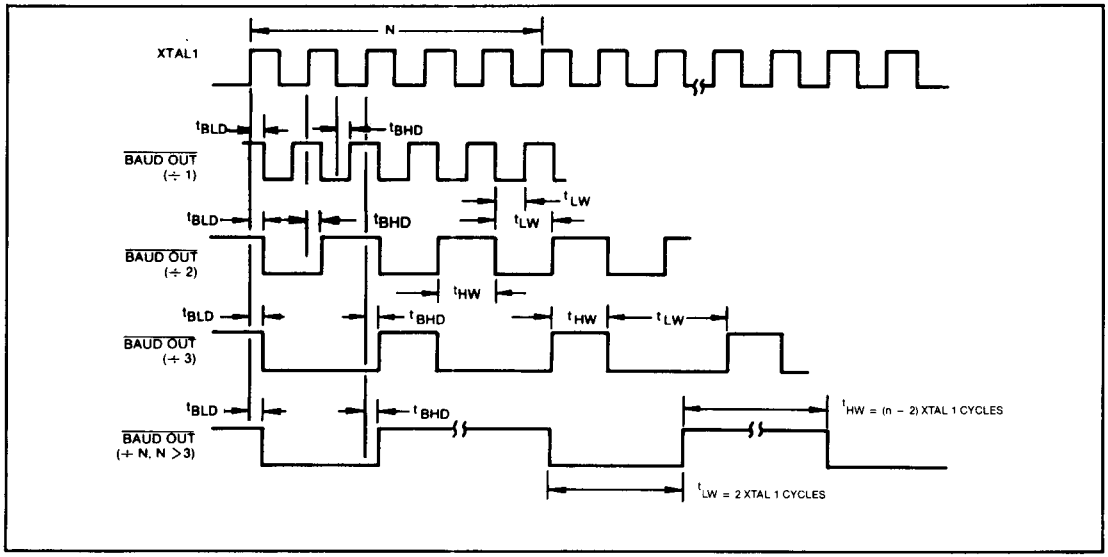
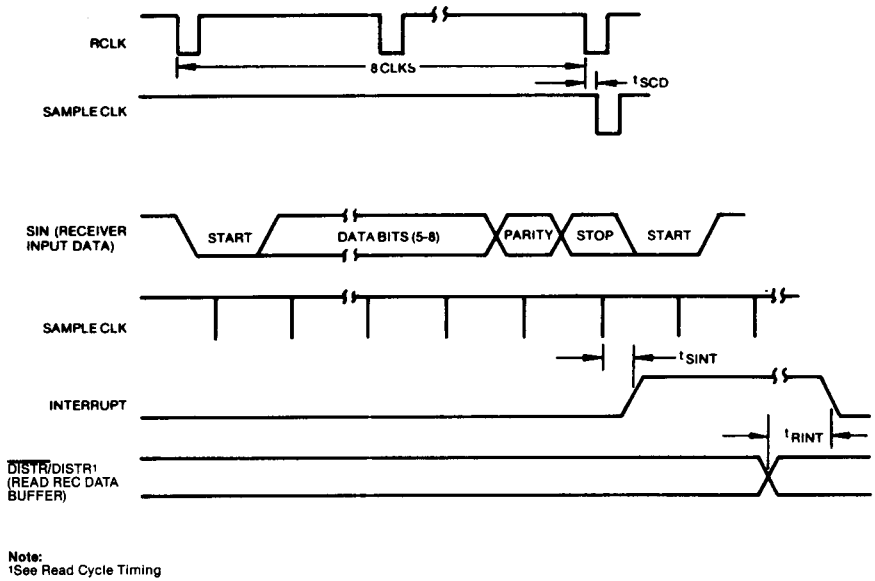


FIGURE 7. BAUD RATE GENERATOR TIMING

TABLE 9. BAUD RATE GENERATOR

SYMBOL	CHARACTERISTIC	WD8250 MIN	WD8250 MAX	WD82C50 MIN	WD82C50 TYP	WD16C450 MIN	WD16C450 MAX	UNITS	TEST CONDITIONS
N	Baud Rate Divisor	1	$(2^{16}-1)$	1	$(2^{16}-1)$	1	$(2^{16}-1)$		
t_{BLD}	Baud Output Negative Edge Delay		250		250		125	ns	100pF Load
t_{BHD}	Baud Output Positive Edge Delay		250		250		125	ns	100pF Load
t_{LW}	Baud Output Low Time	450		425		425		ns	100pF Load
t_{HW}	Baud Output High Time	330		330		330		ns	100pF Load



Note:
[1]See Read Cycle Timing

FIGURE 8. RECEIVER TIMING

TABLE 10. RECEIVER TIMING

SYMBOL	CHARACTERISTIC	WD8250 MIN	WD8250 MAX	WD82C50 MIN	WD82C50 MAX	WD16C450 MIN	WD16C450 MAX	UNITS	TEST CONDITIONS
t_{SCD}	Delay from RCLK to Sample Time		2		2		2	μs	
t_{SINT}	Delay from Sample CLK to Set Interrupt		2		2	1	1	RCLK Cycles	100pF Load
t_{RINT}	Delay from $\overline{DISTR}$/DISTR (RD RBR) Reset Interrupt	.250	1	.250	1	.250	1	μs	100pF Load

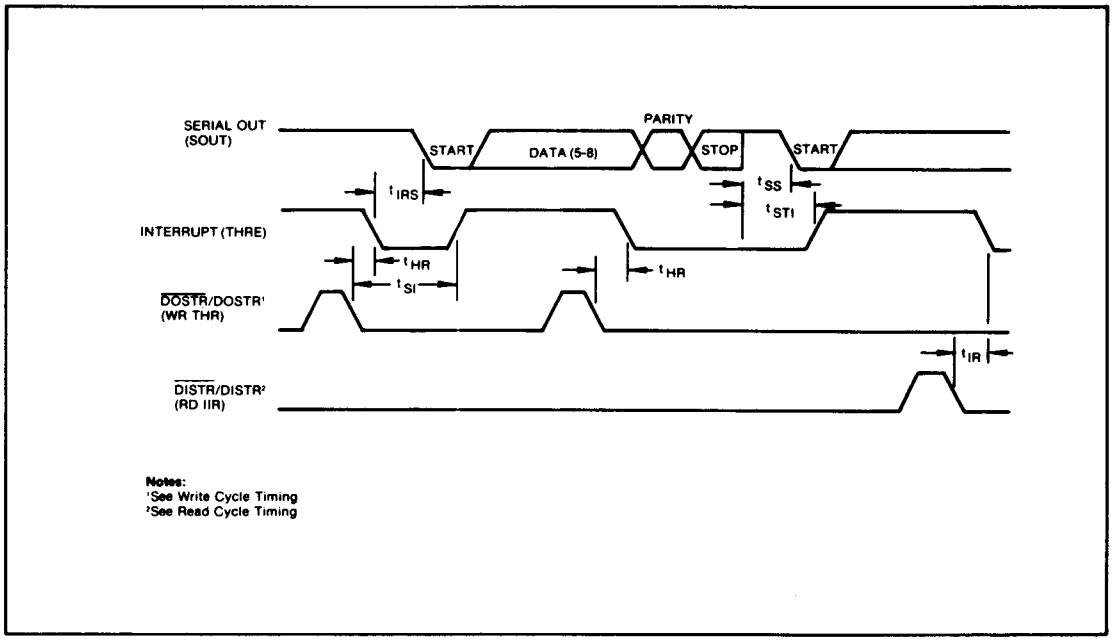


FIGURE 9. TRANSMITTER TIMING

TABLE 11. TRANSMITTER TIMING

SYMBOL	CHARACTERISTIC	WD8250 MIN	WD8250 MAX	WD82C50 MIN	WD82C50 MAX	WD16C450 MIN	WD16C450 MAX	UNITS	TEST CONDITIONS
t_{HR}	Delay from $\overline{DOSTR}$/DOSTR (WR THR) to Reset Interrupt	.250	1.0	.250	1.0		.175	μs	100pF Load
t_{IRS}	Delay from Initial INTR Reset to Transmit Start		16		16	8	24	$\overline{BAUDOUT}$ Cycles	
t_{SI}	Delay from Initial Write to Interrupt		24		24	16	32	$\overline{BAUDOUT}$ Cycles	
t_{SS}	Delay from Stop to Next Start	.250	1	.250	1	.250	1	μs	
t_{STI}	Delay from Stop to Interrupt ($\overline{THRE}$)		8		8		8	$\overline{BAUDOUT}$ Cycles	
t_{IR}	Delay from $\overline{DISTR}$/DISTR (RD IIR) to Reset Interrupt ($\overline{THRE}$)	.250	1	.250	1		.250	μs	100pF Load

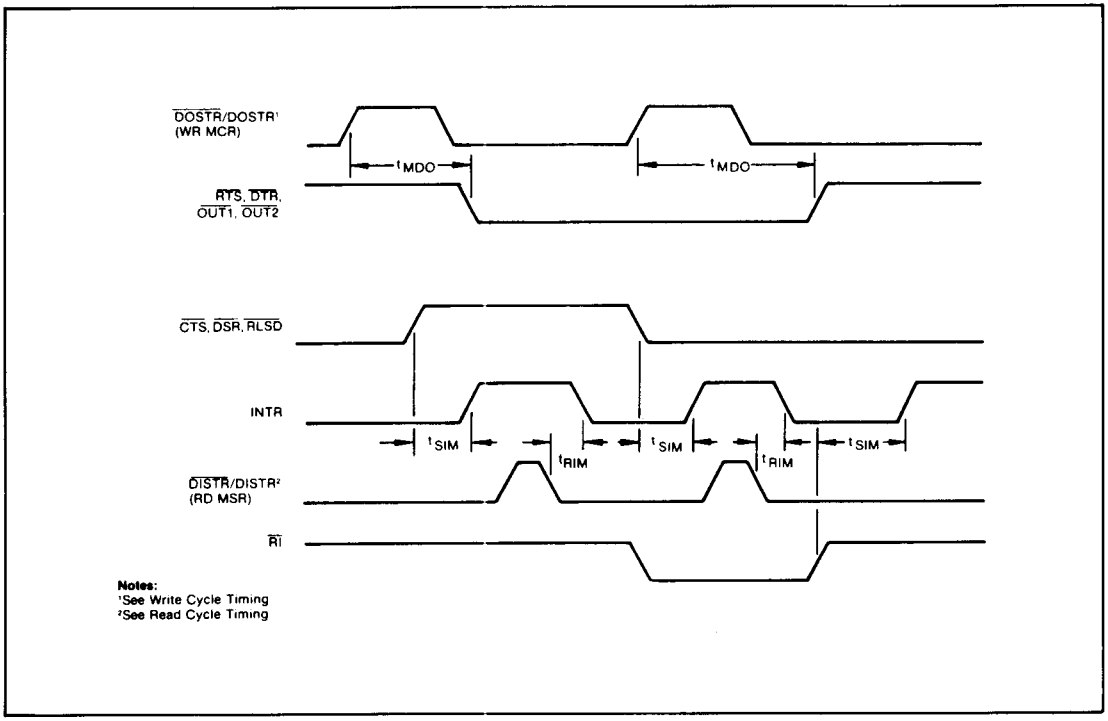


FIGURE 10. MODEM CONTROL TIMING

TABLE 12. MODEM CONTROL TIMING

SYMBOL	CHARACTERISTIC	WD8250 MIN	WD8250 MAX	WD82C50 MIN	WD82C50 MAX	WD16C450 MIN	WD16C450 MAX	UNITS	TEST CONDITIONS
t_{MDO}	Delay from DOSTR/DOSTR (WR MCR) to Output	.250	1	.250	1		.200	μs	100 pF Load
t_{SIM}	Delay to Set Interrupt from MODEM Input	.250	1	.250	1	.250	1	μs	100 pF Load
t_{RIM}	Delay to Reset Interrupt from DISTR/DISTR (RD MSR)	.250	1	.250	1		.250	μs	100 pF Load

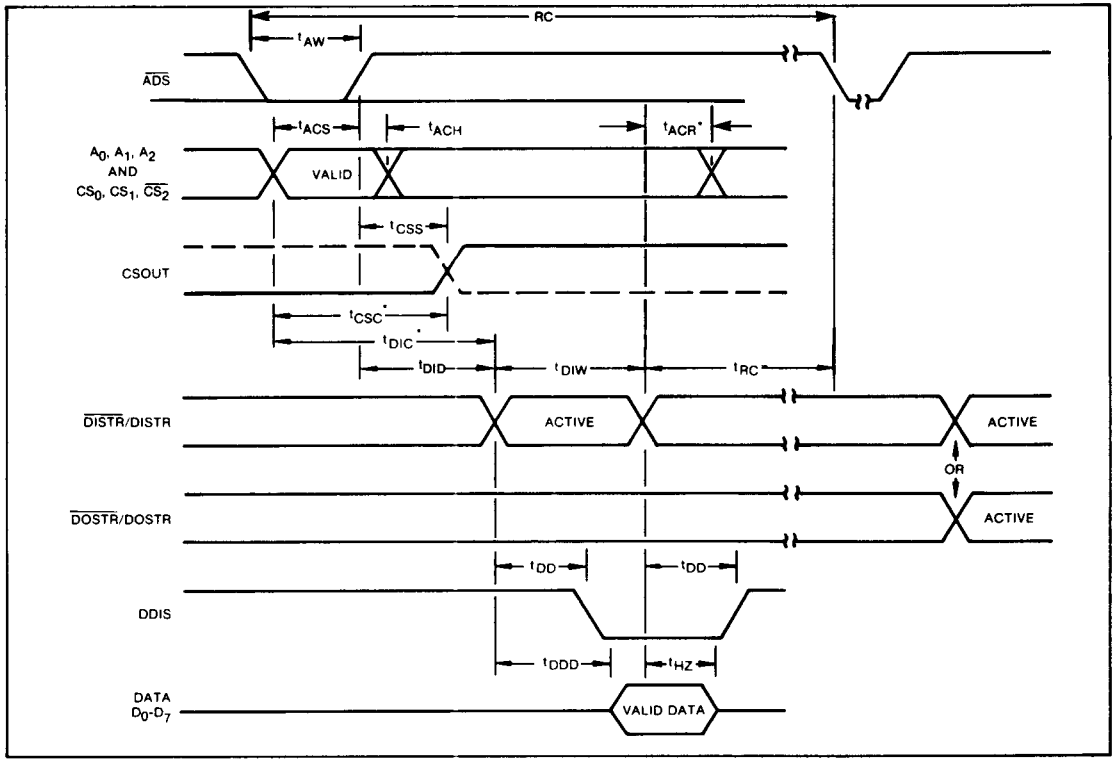


FIGURE 11. READ CYCLE TIMING

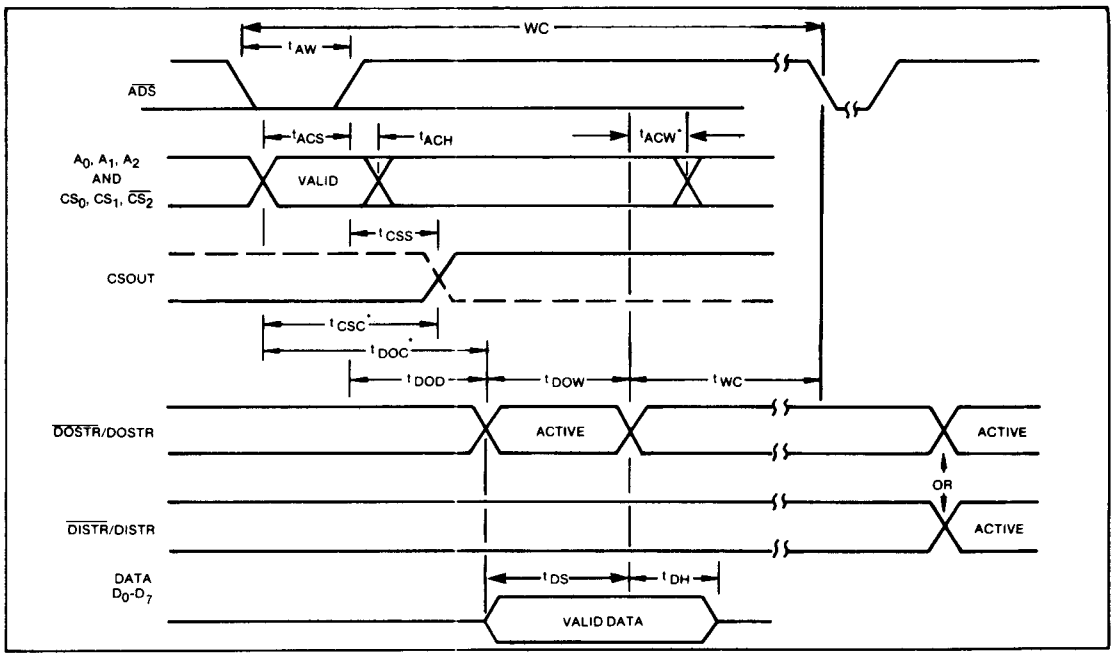


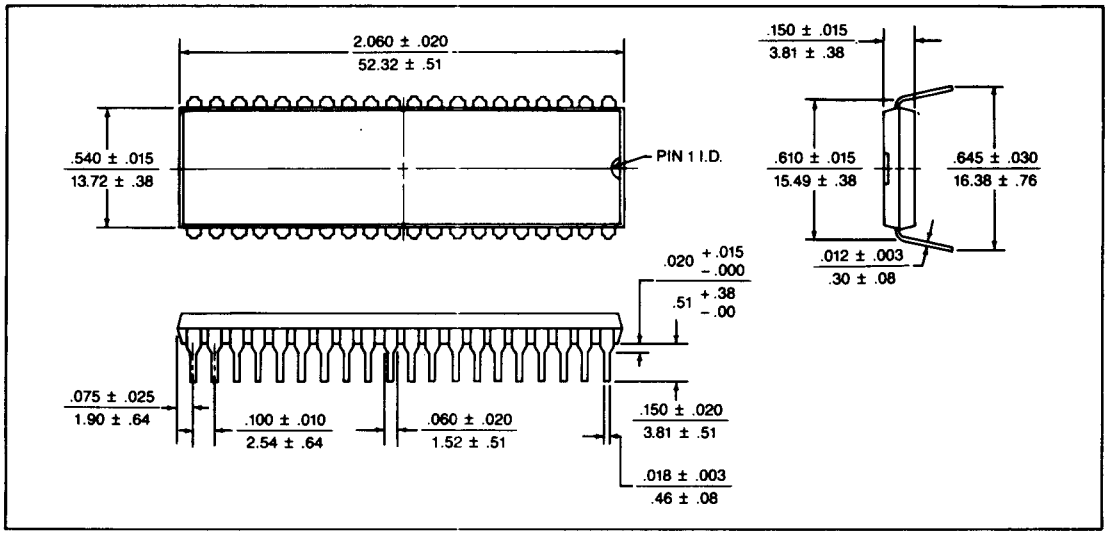
FIGURE 12. WRITE CYCLE TIMING

TABLE 13. READ/WRITE CYCLE TIMING

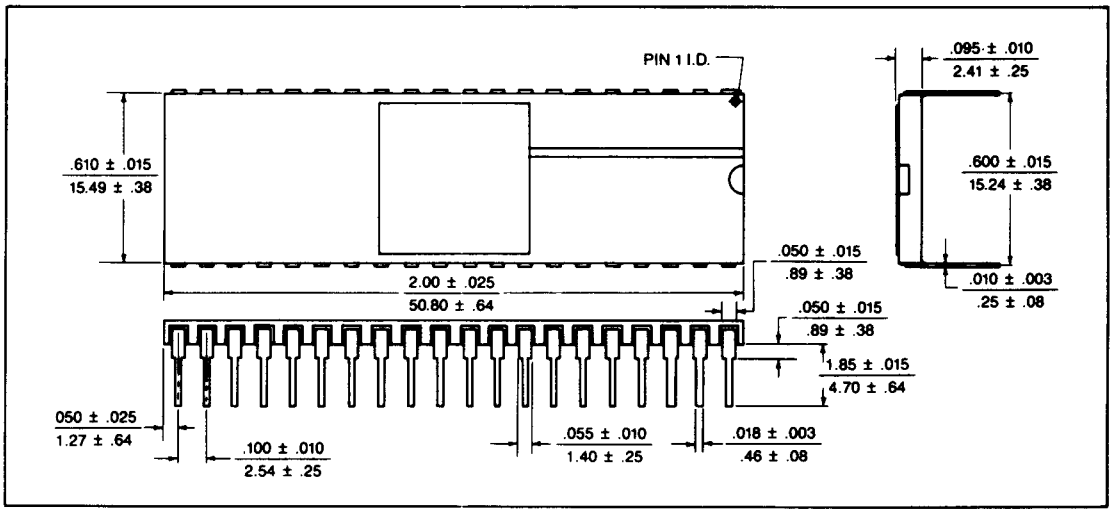
SYMBOL	CHARACTERISTIC	WD8250 MIN	WD8250 MAX	WD82C50 MIN	WD82C50 MAX	WD16C450 MIN	WD16C450 MAX	UNITS	TEST CONDITIONS
t_{AW}	Address Strobe Width	120		90		60		ns	1TTL Load
t_{ACS}	Address and Chip Select Setup Time	100		110		60		ns	1TTL Load
t_{ACH}	Address and Chip Select Hold Time	10		0		0		ns	1TTL Load
t_{CSS}	CSOUT Delay from Latch		160		90			ns	1TTL Load
t_{DID}	$\overline{DISTR}$/DISTR Delay from Latch	50		0				ns	1TTL Load
t_{DIW}	$\overline{DISTR}$/DISTR Strobe Width	300		175		125		ns	1TTL Load
t_{RC}	Read Cycle Delay	655		1735		175		ns	1TTL Load
RC	Read Cycle = $t_{ACS} + t_{DID} + t_{DIW} + t_{RC} + 20$ ns	1125		2050		360		ns	1TTL Load
t_{DD}	$\overline{DISTR}$/DISTR to Driver Disable Delay		200		150		60	ns	1TTL Load
t_{DDD}	Delay from $\overline{DISTR}$/DISTR to Data		300		250		125	ns	1TTL Load
t_{HZ}	$\overline{DISTR}$/DISTR to Floating Data Delay	60		100		0	100	ns	1TTL Load
t_{DOD}	$\overline{DOSTR}$/DOSTR Delay from Latch	20		50				ns	1TTL Load
t_{DOW}	$\overline{DOSTR}$/DOSTR Strobe Width	175		175		100		ns	1TTL Load
t_{WC}	Write Cycle Delay	685		1785		200		ns	1TTL Load
WC	Write Cycle = $t_{ACS} + t_{DOD} + t_{DOW} + t_{WC} + 20$ ns	1000		2150		360		ns	1TTL Load
t_{DS}	Data Setup Time	t_{DOW}		t_{DOW}		40		ns	1TTL Load
t_{DH}	Data Hold Time	60		60		40		ns	1TTL Load
t_{CSC}*	CSOUT Delay from Select		260		200		100	ns	1TTL Load
t_{DIC}*	$\overline{DISTR}$/DISTR Delay from Select or Address	70		70		50		ns	1TTL Load
t_{DOC}*	$\overline{DOSTR}$/DOSTR Delay from Select or Address	70		70		50		ns	1TTL Load
t_{ACR}*	Address and Chip Select Hold Time from $\overline{DISTR}$/DISTR	10		50		20		ns	1TTL Load
t_{ACW}*	Address and Chip Select Hold Time from $\overline{DOSTR}$/DOSTR	10		50		20		ns	1TTL Load
t_{MR}	Master Reset Pulse Width	1 0		25		5.0		μs	1TTL Load
t_{XH}	Duration of Clock HIGH Pulse			140		140		ns	
t_{XL}	Duration of Clock LOW Pulse			140		140		ns	External Clock (3.1 MHz Max.)

*Only applicable when $\overline{ADS}$ is permanently low.

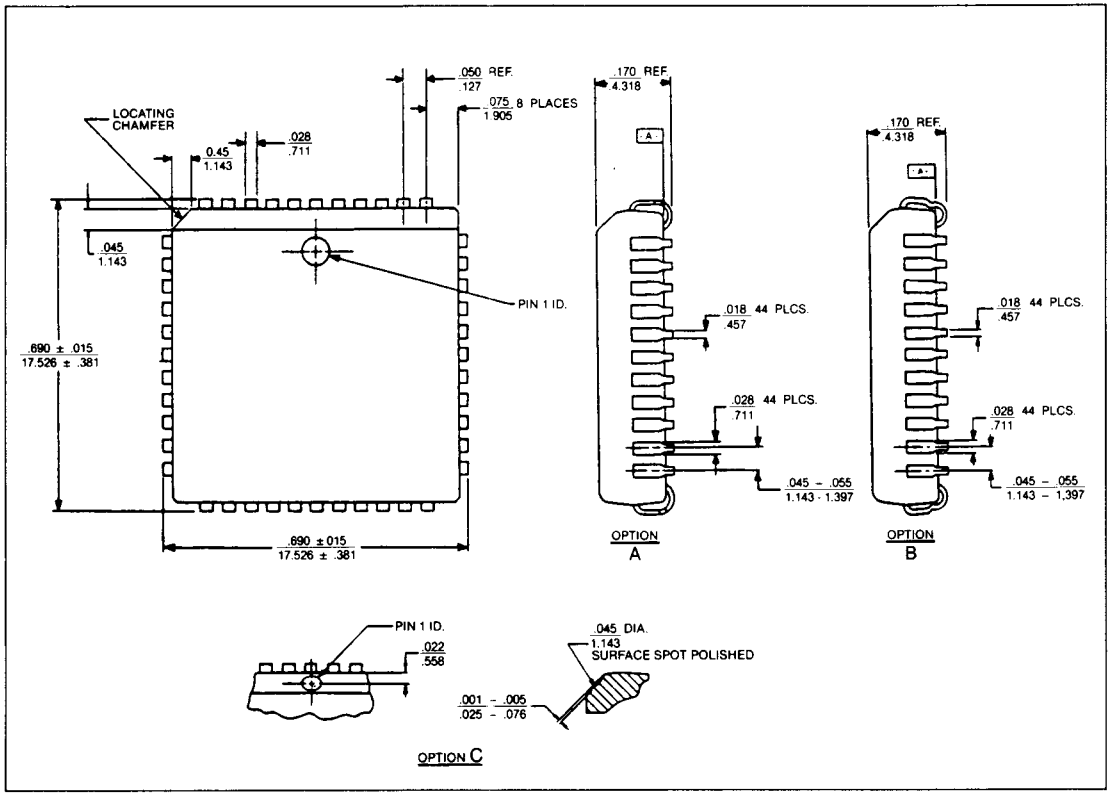
PACKAGE DIAGRAMS



40 LEAD PLASTIC "PL"



40 LEAD CERAMIC "AL"



44 LEAD PLASTIC "JM"

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