HOLT INTEGRATED CIRCUITS INC.

HI-8592, HI-8593, HI-8594

Single-Rail ARINC 429 Differential Line Driver

July, 2022

GENERAL DESCRIPTION

The HI-8592 bus interface product is a silicon gate CMOS device designed as a line driver in accordance with the ARINC 429 bus specifications. The part includes a negative voltage converter allowing it to operate from a single +5V supply using only two external capacitors. The part also features high-impedance outputs (tri-state) when both data inputs are taken high, allowing multiple line drivers to be connected to a common bus.

The HI-8593 and HI-8594 are reduced pin count versions of HI-8592 which do not incorporate the negative voltage converter. These devices are compatible with Holt's existing HI-8570 and HI-8571 respectively, with the added advantage of the tri-state outputs. For even smaller board footprint, versions are also available in leadless, surface mount QFN-style packages.

Logic inputs feature built-in 2,000V minimum ESD input protection as well as 5V or 3.3V logic level compatibility.

Products with 5 Ohm or 37.5 Ohm resistors in series with each ARINC output are available to allow the use of external resistors for lightning protection.

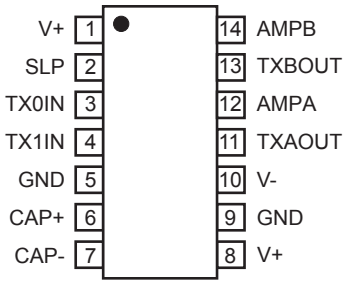
The HI-859x series of line drivers are intended for use where logic signals must be converted to ARINC 429 levels such as when using an FPGA or the HI-3584 ARINC 429 Serial Transmitter/Dual Receiver.

The family of parts are available in Industrial -40°C to +85°C, or Extended, -55°C to +125°C temperature ranges. Optional burn-in is available on the extended temperature range.

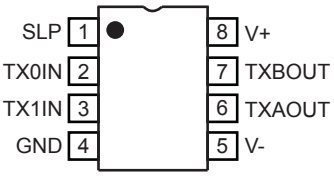
FEATURES

- Single +5V supply
- Negative voltage generated on-chip (HI-8592)
- Digitally selectable rise and fall times
- Tri-state Outputs
- Plastic 8 & 14-pin thermally enhanced SOIC packages available
- 5 Ohm or 37.5 Ohm output resistance
- Industrial and Extended temperature ranges
- Burn-in available

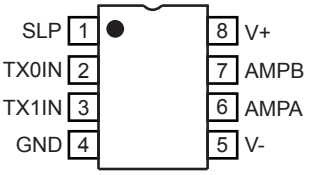
PIN CONFIGURATION (TOP VIEW)



HI-8592PS
14-PIN PLASTIC SMALL OUTLINE (ESOIC) NB



HI-8593PS
8-PIN PLASTIC SMALL OUTLINE (ESOIC) NB



HI-8594PS
8-PIN PLASTIC SMALL OUTLINE (ESOIC) NB

(*See page 10 for additional package pin configurations*)

Table 1. Function Table

TX1IN	TX0IN	SLP	TXAOUT	TXBOUT	SLOPE
0	0	X	0V	0V	N/A
0	1	0	-5V	5V	10µs
0	1	1	-5V	5V	1.5µs
1	0	0	5V	-5V	10µs
1	0	1	5V	-5V	1.5µs
1	1	X	Hi-Z	Hi-Z	N/A

BLOCK DIAGRAM

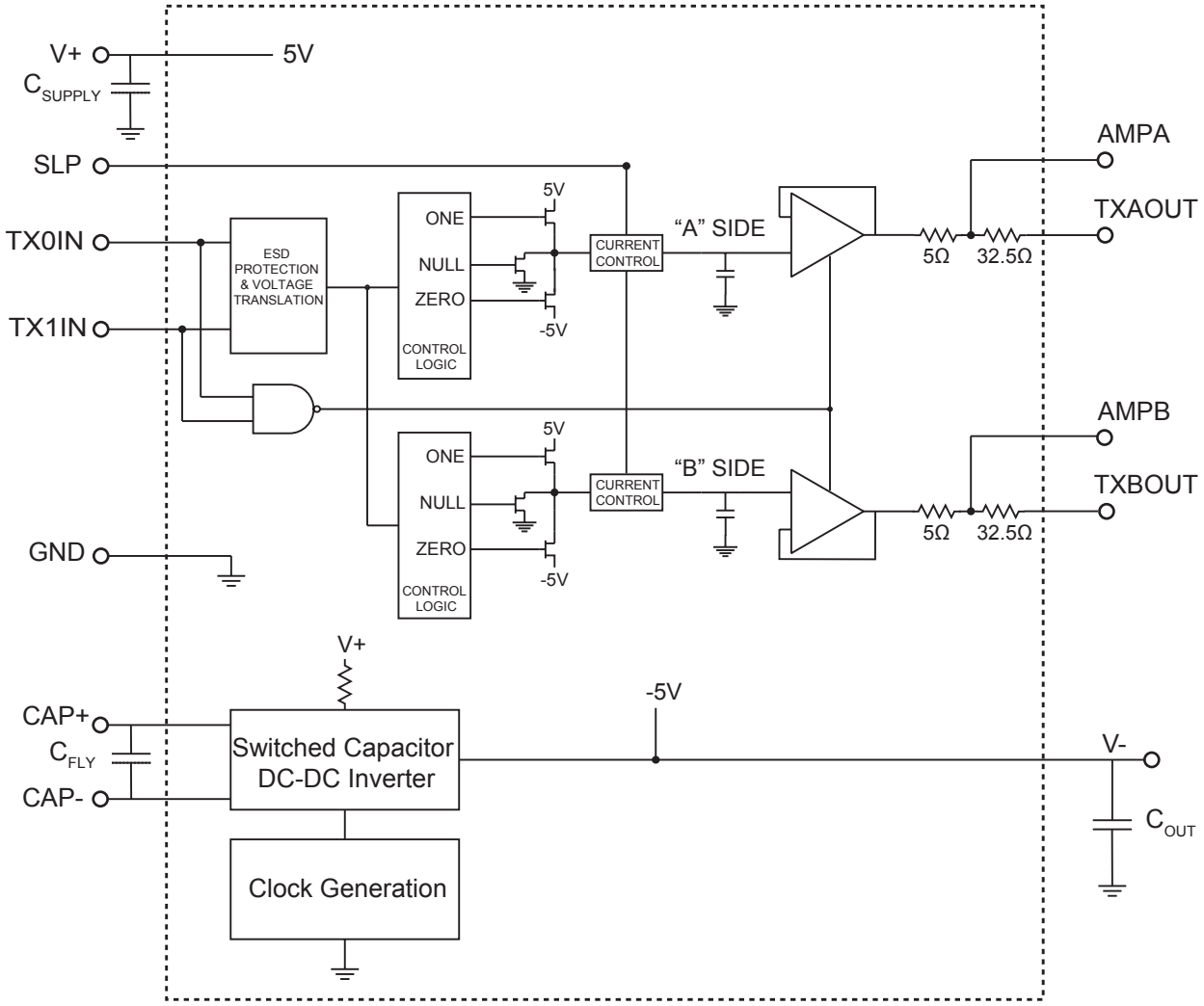


Figure 1. HI-8592 Block Diagram

PIN DESCRIPTIONS

Table 2. Pin Descriptions

Pin	Function	Description
V+	POWER	+5V power supply
SLP	INPUT	Output slew rate control. High selects ARINC 429 high-speed. Low selects ARINC 429 low-speed.
TX0IN	INPUT	Data input zero
TX1IN	INPUT	Data input one
GND	POWER	Ground supply
CAP+	ANALOG	Positive connection for external capacitor, C_{FLY}. See “Table 4. Converter Characteristics” for recommended capacitor type.
CAP-	ANALOG	Negative connection for external capacitor, C_{FLY}. See “Table 4. Converter Characteristics” for recommended capacitor type.
V-	POWER	-5V supply, may be connected to supply or used with on-chip negative supply converter. See “Table 4. Converter Characteristics” for recommended value of C_{OUT}..
TXAOUT	OUTPUT	ARINC high output with 37.5 Ohms series resistance
AMPA	OUTPUT	ARINC high output with 5 Ohms series resistance
TXBOUT	OUTPUT	ARINC low output with 37.5 Ohms series resistance
AMPB	OUTPUT	ARINC low output with 5 Ohms series resistance

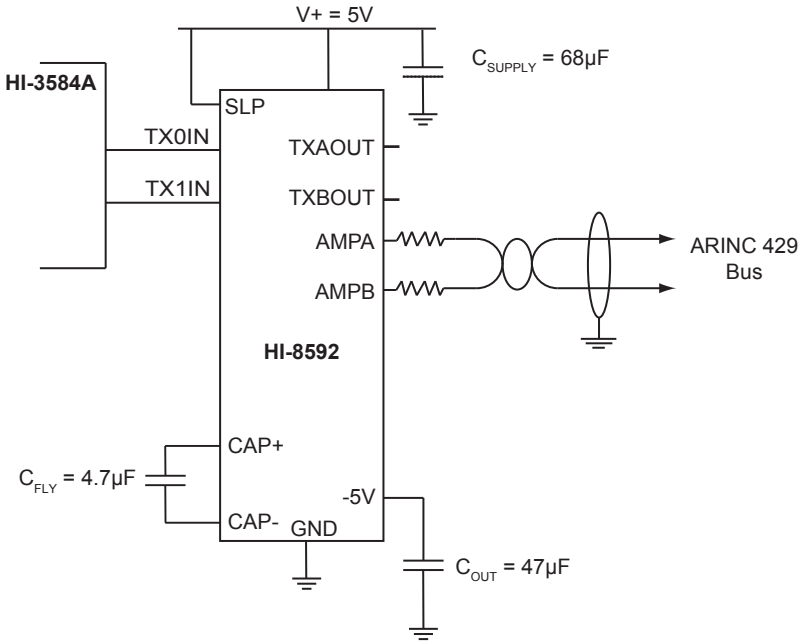


Figure 2. Application Example

FUNCTIONAL DESCRIPTION

Figure 1 is a block diagram of the line driver. The chip requires a positive 5V supply at V+. The negative 5V supply at V- may be from an external source or may be provided using the on-chip negative rail generator by connecting the two external capacitors, C_{FLY} and C_{OUT}. See "Table 4. Converter Characteristics" for recommended capacitor type.

Currents for slope control are set by on-chip resistors.

The TX0IN and TX1IN inputs receive logic signals from a control transmitter chip such as the HI-3584. TXAOUT and TXBOUT hold each side of the ARINC bus at Ground until one of the inputs becomes a One. If for example TX1IN goes high, a charging path is enabled to 5V on an "A" side internal capacitor while the "B" side is enabled to -5V. The charging current is selected by the SLP pin. If the SLP pin is high, the capacitor is nominally charged from 10% to 90% in 1.5µs. If SLP is low, the rise and fall times are 10µs.

The reduced pin-count HI-8593 and HI-8594 require an external -5V supply.

A unity gain buffer receives the internally generated slopes and differentially drives the ARINC line. Current is limited by the series output resistors at each pin. There are no fuses at the outputs of the HI-859x family.

The HI-8593 has 37.5 ohms in series with each TXOUT output and the HI-8594 has 5 ohms in series with each AMP output. The AMP outputs are for applications where external series resistance is required, typically for lightning protection devices. Both output types are available on the HI-8592. Holt Application Note AN-300 describes suitable lightning protection schemes.

All devices feature tri-stateable outputs to allow multiple line drivers to be connected to the same ARINC 429 bus. Setting TX1IN and TX0IN both to a logic "1" puts the outputs in the high-impedance state.

The HI-8592 family of line drivers are built using high-speed CMOS technology. Care should be taken to ensure the V+ and V- supplies are locally decoupled to reduce noise. An application example is shown in Figure 2.

ABSOLUTE MAXIMUM RATINGS

Supply Voltages	
V+	+7V
V-	-7V
DC Current per input pin	+10mA
Power Dissipation at 25°C	
plastic SOIC	1.0W, derate 10mW/°C
ceramic DIP	0.5W, derate 7mW/°C
Solder Temperature (reflow)	260°C
Storage Temperature	-65°C to +150°C

Note: *The HI-8592 family of drivers are available in small-footprint, thermally enhanced SOIC and QFN (chip-scale) packages. These packages include a metal heat sink located on the bottom surface of the device. This heat sink should be soldered down to the printed circuit board for optimum thermal dissipation.*

The heat sink is electrically isolated from the chip and can be soldered to any ground or power plane.

RECOMMENDED OPERATING CONDITIONS

Supply Voltages	
V+	+4.75V to +5.25V
V-	-5.25V to -4.75V
Temperature Range	
Industrial	-40°C to +85°C
Extended	-55°C to +125°C

NOTE: *Stresses above absolute maximum ratings or outside recommended operating conditions may cause permanent damage to the device. These are stress ratings only. Operation at the limits is not recommended.*

ELECTRICAL CHARACTERISTICS

Table 3. DC Electrical Characteristics

V+ = +5V, V- = -5V (HI-8593/4 only), T_A = Operating Temperature Range (unless otherwise stated)

Parameters	Symbol	Test Conditions	Min	Typ	Max	Units
Input Voltage (TX1IN, TX0IN, SLP)						
High	V_{IH}		2.1	-	V+	V
Low	V_{IL}		-	-	0.5	V
Input Current (TX1IN, TX0IN, SLP)						
Source	I_{IH}	V_{IN} = 5V	-	-	0.1	µA
Sink	I_{IL}	V_{IN} = 0V	-	-	0.1	µA
ARINC Output Voltage (Differential)						
one	V_{DIFF1}	no load; TXAOUT - TXBOUT	9	10	11	V
zero	V_{DIFF0}	no load; TXAOUT - TXBOUT	-11	-10	-9	V
null	V_{DIFFN}	no load; TXAOUT - TXBOUT	-0.5	0	0.5	V
ARINC Output Voltage (Ref. to GND)						
one or zero	V_{DOUT}	no load & magnitude at pin	4.5	5.0	5.5	V
null	V_{NOUT}	no load	-0.25	0	0.25	V
Operating Supply Current		SLP = V+				
V+	I_{DD}	TX1IN & TX0IN = 0V: no load	-	22	28	mA
GND	I_{GND}	TX1IN & TX0IN = 0V: no load	-	10	16	mA
V-	I_{EE}	TX1IN & TX0IN = 0V: no load	-16	-10	-	mA
ARINC Outputs Shorted	I_{DDS}	See Note 1	-	165	-	mA
ARINC Output Impedance	Z_{OUT}					
TXOUT pins				37.5		Ohms
AMP pins				5		Ohms
ARINC Output Tri-State Current	I_{OZ}	V- < V_{OUT} < V+, T_A = 125°C TX0IN = TX1IN = V+	-1.0	0	+1.0	µA

Note 1: TXAOUT and/or TXBOUT shorted to each other or ground. AMPA and/or AMPB shorted to each other or ground (assumes external resistors are connected to AMPA and AMPB to comply with ARINC 429 37.5 Ohm output resistance requirement).

Table 4. Converter Characteristics

V+ = +5V, V- = -5V (HI-8593/4 only), T_A = Operating Temperature Range (unless otherwise stated)

Parameters	Symbol	Test Conditions	Min	Typ	Max	Units
Start-up transient (V+, V-)	t_{START}		-	-	10	ms
Operating Switching Frequency	f_{sw}		-	650	-	kHz
Worst case maximum voltage doubler output	$V_{DD2+(max)}$	V_{DD} = 3.6V. T = -55ºC. Open load.			6.93	V
DC/DC convertor capacitor recommendations. **For optimum performance use typical (not min.) values. For EMC compliance, see AN-135. C_{FLY} and C_{OUT} caps are Ceramic, preferably multilayer, non polarized dielectric XR7, 10V min.**						
Ratio of bulk storage to fly-back capacitors	C_{OUT} / C_{FLY}		2.2	10		
Fly-back capacitor (Recommend ceramic, preferably multilayer, dielectric XR7 caps, 10V min.).	C_{FLY} $C_{FLY(ESR)}$	C_{OUT} / C_{FLY} >= 10 [0.5, 1.0]Mhz	1.0	4.7	- 500	µF mΩ
Bulk storage capacitor (Recommend ceramic, preferably multilayer, dielectric XR7 caps, 10V min.).	C_{OUT} $C_{OUT(ESR)}$	C_{OUT} / C_{FLY} >= 10 [0.5, 1.0]Mhz	2.2	47	- 300	µF mΩ
By-pass capacitor (Recommend ceramic cap, 10V min.).	C_{SUPPLY}	C_{SUPPLY} >= C_{OUT} (connect from V_{DD} to GND)				

Table 5. AC Electrical Characteristics

V+ = +5V, V- = -5V (HI-8593/4 only), T_A = Operating Temperature Range (unless otherwise stated)

Parameters	Symbol	Test Conditions	Min	Typ	Max	Units
Line Driver Propogation Delay		defined in Figure 3, no load				
Output high to low	t_{phlx}		-	500	-	ns
Output low to high	t_{plhx}		-	500	-	ns
Line Driver Transition Times						
High Speed		SLP = V+				
Output high to low	t_{fx}		1.0	1.5	2.0	µs
Output low to high	t_{rx}		1.0	1.5	2.0	µs
Low Speed		SLP = GND				
Output high to low	t_{fx}		5.0	10.0	15.0	µs
Output low to high	t_{rx}		5.0	10.0	15.0	µs
Input Capacitance (Logic)[1]	C_{IN}		-	-	10	pF
Output Capacitance (Tri-state)[1]	C_{OUT}	TX0IN = TX1IN = V+	-	-	1.5	pF

Notes:
1. Guaranteed but not tested

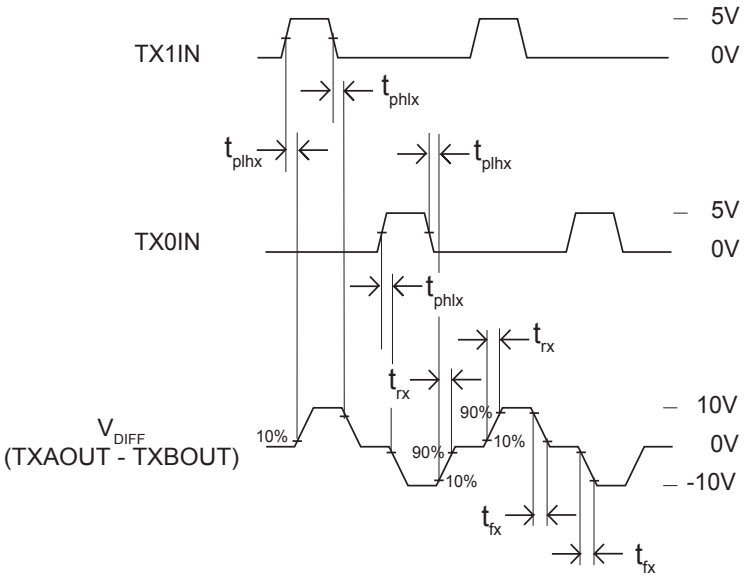


Figure 3. Line Driver Timing

PACKAGE THERMAL CHARACTERISTICS

Maximum ARINC LOAD

Package Style[1]	ARINC 429 Data Rate	Supply Current (mA)[2]			Junction Temp, T_j (°C)		
		T_A = 25°C	T_A = 85°C	T_A = 125°C	T_A = 25°C	T_A = 85°C	T_A = 125°C
14-Lead Plastic ESOIC[5]	Low Speed[3]	44	45	45	31	91	131
	High Speed[4]	58	57	55	33	93	132

TXAOUT and TXBOUT Shorted to Ground[6,7,8]

Package Style[1]	ARINC 429 Data Rate	Supply Current (mA)[2]			Junction Temp, T_j (°C)		
		T_A = 25°C	T_A = 85°C	T_A = 125°C	T_A = 25°C	T_A = 85°C	T_A = 125°C
14-Lead Plastic ESOIC[5]	Low Speed[3]	118	108	98	44	102	140
	High Speed[4]	120	106	92	44	102	140

Maximum ARINC LOAD

Package Style[1]	ARINC 429 Data Rate	Supply Current (mA)[2]			Junction Temp, T_j (°C)		
		T_A = 25°C	T_A = 85°C	T_A = 125°C	T_A = 25°C	T_A = 85°C	T_A = 125°C
8-Lead Plastic ESOIC[5]	Low Speed[3]	26	27	28	42	103	144
	High Speed[4]	34	35	35	50	111	151

TXAOUT and TXBOUT Shorted to Ground[6,7,8]

Package Style[1]	ARINC 429 Data Rate	Supply Current (mA)[2]			Junction Temp, T_j (°C)		
		T_A = 25°C	T_A = 85°C	T_A = 125°C	T_A = 25°C	T_A = 85°C	T_A = 125°C
8-Lead Plastic ESOIC[5]	Low Speed[3]	64	62	60	79	137	176
	High Speed[4]	68	66	64	83	141	179

Notes:

1. All data taken in still air.
2. At 100% duty cycle, 5V power supplies.
3. Low Speed: Data Rate = 12.5 Kbps, Load: R = 400 Ohms, C = 30 nF.
4. High Speed: Data Rate = 100 Kbps, Load: R = 400 Ohms, C = 10 nF. Data not presented for C = 30 nF as this is considered unrealistic for high speed operation.
5. 14 Lead Plastic ESOIC (Thermally enhanced SOIC with built in heat sink). Heat sink not soldered.
6. Similar results would be obtained with TXAOUT shorted to TXBOUT.
7. For applications requiring survival with continuous short circuit, operation above Tj = 175°C is not recommended.
8. Data will vary depending on air flow and the method of heat sinking employed.

ORDERING INFORMATION

HI - 8592xx x x

PART NUMBER	LEAD FINISH
Blank	Tin / Lead (Sn / Pb) Solder
F	Pb-free, RoHS compliant

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C to +85°C	I	No
T	-55°C to +125°C	T	No
M	-55°C to +125°C	M	Yes

PART NUMBER	PACKAGE DESCRIPTION
PS	14 PIN PLASTIC SMALL OUTLINE - NB ESOIC (14HNE)
PC	24 PIN PLASTIC QFN (24PCS). **NOTE: Pb-Free only, RoHS Compliant, NiPdAu**
CR	14 PIN CERDIP (14D). **NOTE: Not Available Pb-Free**

HI - 859x xx x x

PART NUMBER	LEAD FINISH
Blank	Tin / Lead (Sn / Pb) Solder
F	100% Matte Tin (Pb-free, RoHS compliant)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C to +85°C	I	No
T	-55°C to +125°C	T	No
M	-55°C to +125°C	M	Yes

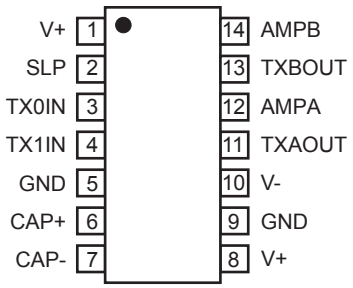
PART NUMBER	PACKAGE DESCRIPTION
PS	8 PIN PLASTIC SMALL OUTLINE - NB ESOIC (8HNE)
CR	8 PIN CERDIP (8D). **NOTE: Not Available Pb-Free**

PART NUMBER	OUTPUT RESISTANCE
8593	37.5 Ohms
8594	5 Ohms

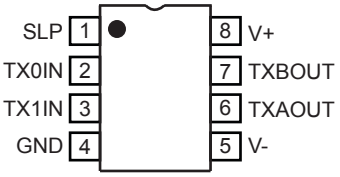
Legend: ESOIC - Thermally enhanced Small Outline Package (SOIC with built-in heat sink)
NB - Narrow Body

ADDITIONAL PIN CONFIGURATIONS

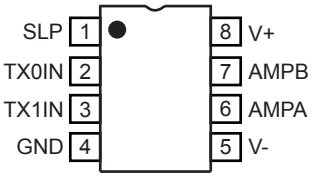
NOTE: All power and ground pins must be connected.



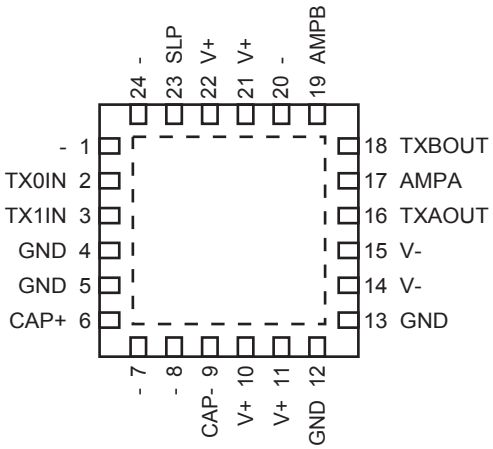
HI-8592CR
14-PIN CERDIP



HI-8593CR
8-PIN CERDIP



HI-8594CR
8-PIN CERDIP



HI-8592PC
24-LEAD 5mm x 5mm QFN

REVISION HISTORY

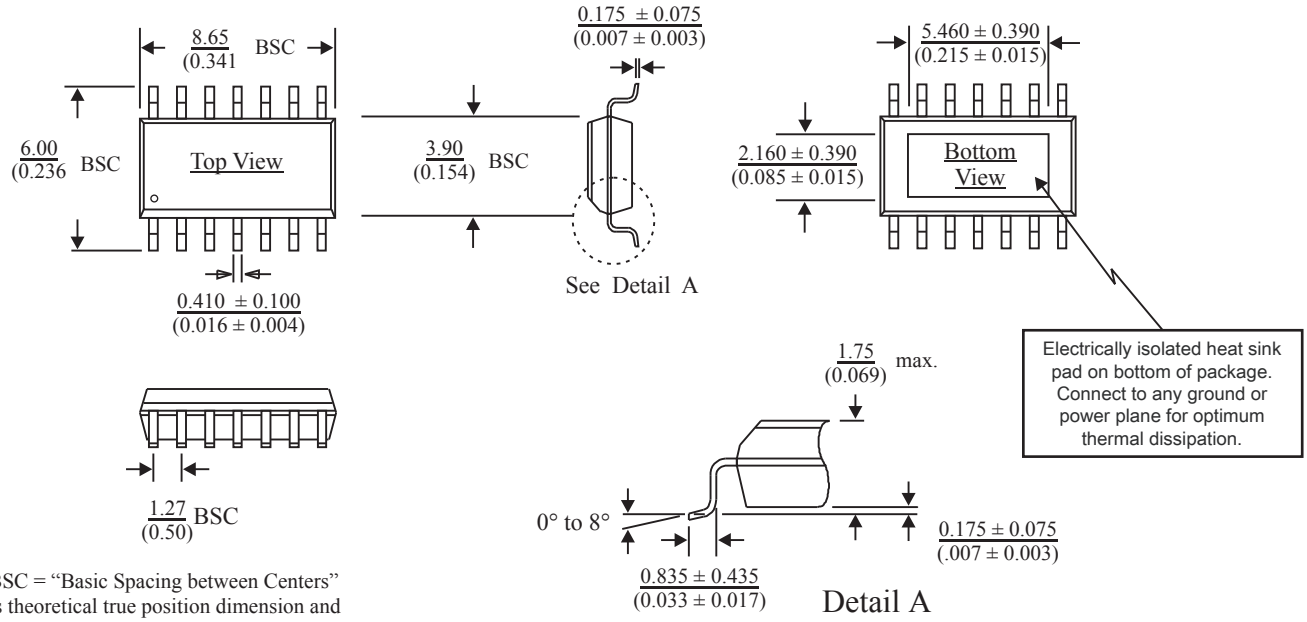
Revision		Date	Description of Change
DS8592,	Rev. NEW	6/21/10	Initial Release
	Rev. A	7/1/10	Corrected typo in features (no “fixed” rise and fall time)
	Rev. B	10/28/10	Rev. A had incorrect package drawing (SOIC-8). Replaced with correct ESOIC-8.
	Rev. C	02/03/11	Updated Package Thermal Characteristics Data for 14-Lead Plastic ESOIC. Added Package Thermal Characteristics Data for 8-Lead Plastic ESOIC.
	Rev. D	11/28/12	Updated Solder Temperature (reflow) to 260^{o}C. Added operating supply current for shorted ARINC outputs. Updated ESOIC-14, ESOIC-8 and QFN-24 package dimensions.
	Rev. E	7/3/13	Updated “Table 4. Converter Characteristics” with recommended capacitor types.
	Rev. F	9/10/13	Clarified QFN-24 package leadfree option.
	Rev. G	10/02/14	Update Converter Characteristics table. Update 14HNE and 8HNE package drawings. Clarify dimensions on 8D package drawing.
	Rev. H	07/27/16	Fix missing cross references to “Table 4. Converter Characteristics”. Updated recommended capacitor types.
	Rev. J	05/18/17	Update the supply voltages in “Recommended Operating Conditions” from ±4.85V to ±4.75V.
	Rev. K	09/02/2021	Correct typo on SLP pin polarity for High Speed / Low Speed in “Table 5. AC Electrical Characteristics”.
	Rev. L	07/07/2022	Clarify test conditions for I_{IH} and I_{IL} parameters.

PACKAGE DIMENSIONS

14-PIN PLASTIC SMALL OUTLINE (ESOIC) - NB
(Narrow Body, Thermally Enhanced)

millimeters (inches)

Package Type: 14HNE

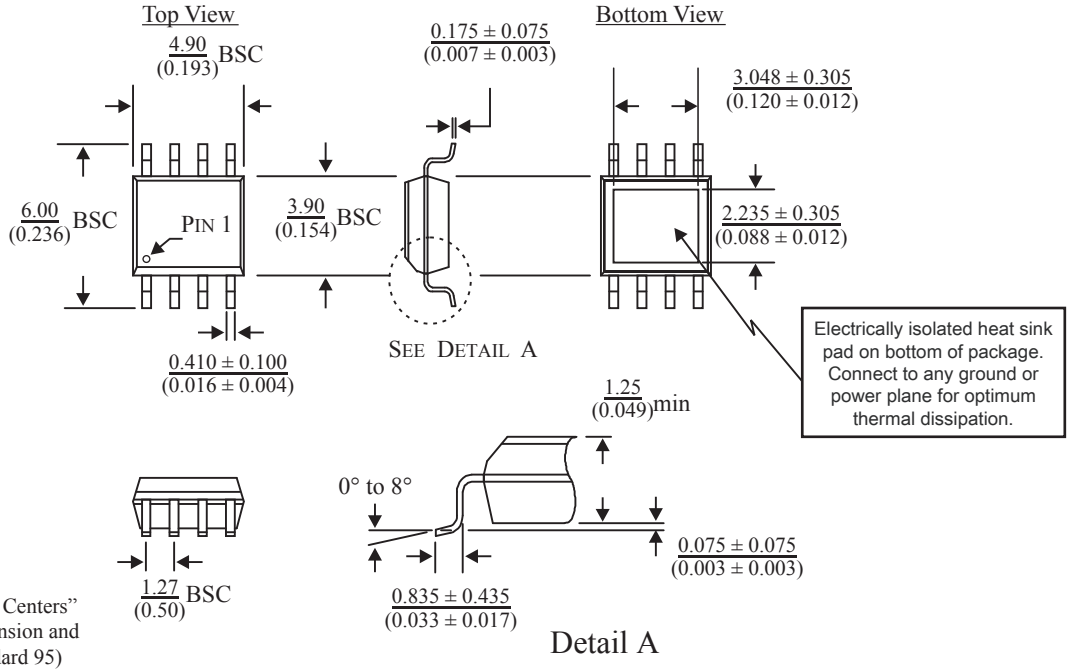


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

8-PIN PLASTIC SMALL OUTLINE (ESOIC) - NB
(Narrow Body, Thermally Enhanced)

millimeters (inches)

Package Type: 8HNE

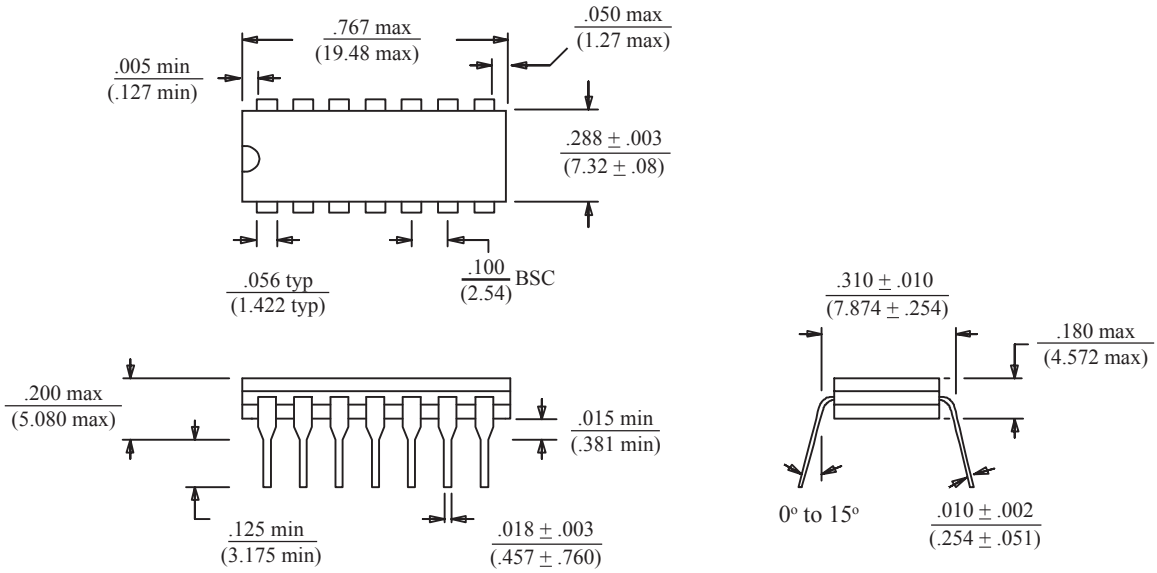


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

14-PIN CERDIP

inches (millimeters)

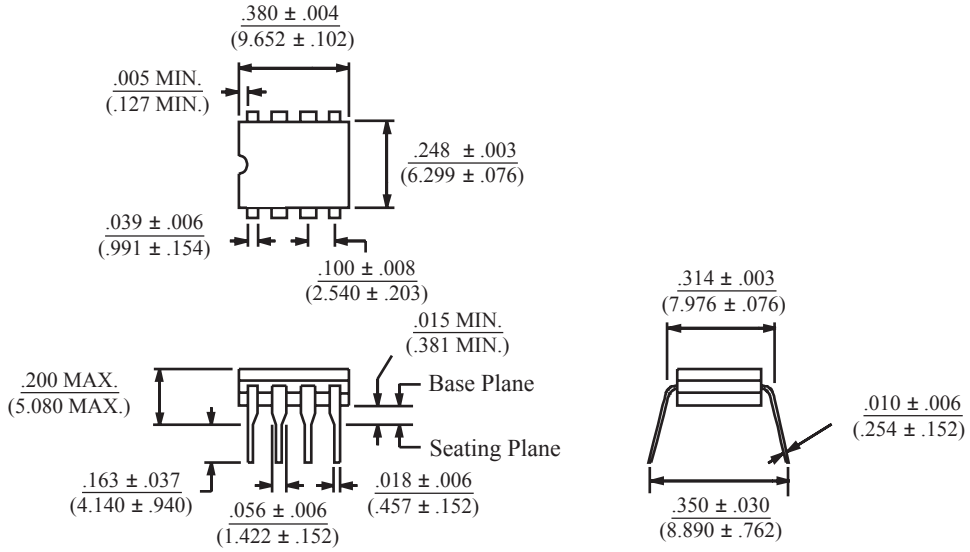
Package Type: 14D



8-PIN CERDIP

inches (millimeters)

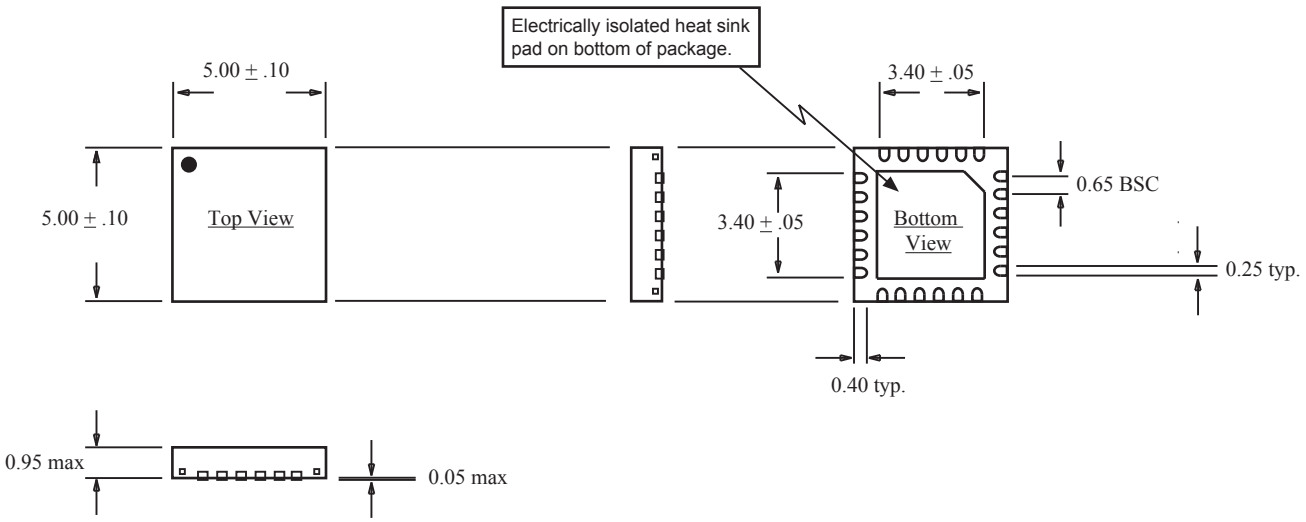
Package Type: 8D



24-PIN PLASTIC CHIP-SCALE PACKAGE (QFN)

millimeters

Package Type: 24PCS



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